CECS eNEWS

Volume 3, Issue 2, April 2003

Center for Embedded Computer Systems, University of California, Irvine

Highlights:

- Amelio Visitation
- Cassen Joins Staff
- 2 Best Paper Awards
- Professor Gajski
- Graduate Student Mishra
- Publications

Inside this issue:

Amelio Visits CECS

On January 8, 2003, Dr. Gilbert F. Amelio visited the Center for Embedded Computer Systems (CECS) at the University of California, Irvine. Gil serves on our CECS Research Advisory Board and we were delighted to host him for a review of our research programs and tour our laboratory facilities.

Professor Nik Dutt discussing memory and architecture exploration issues with Gil and Graduate Students Mehrdad Reshadi, Sudeep Pasricha, Srikanth Srinvasan, and Prabhat Mishra.

Professor Dan Gajski, Gil, and Bob Larsen at main entrance to CECS building.

Professor Fadi Kurdahi discussing reconfiguable computing architecture with Gil.

Professor Tony Givargis discussing power-aware adaptive systems with Gil and Graduate Student Andre Nacul.

Gil emphasizing a technical point.

Gil looking like an avid CECS supporter wearing a CECS baseball cap!

CECS DAC Open House

On Friday afternoon, June 6, 2003, *CECS* will host an Open House to showcase our Center for DAC attendees. Project demonstrations and laboratory tours are planned with refreshments available. Please plan your DAC schedule to include a pleasant visit with us.

Staff Introduction

The Center for Embedded Computer Systems (CECS) is pleased to announce that Quentin C. (Quent) Cassen has joined the CECS staff as a Research Relations Officer. As such, he will be responsible for developing corporate research relations related to research programs and projects at CECS.

Quent recently retired from Rockwell International Corporation (now Conexant Systems, Inc.) where he held a variety of engineering and management positions over the past thirty years. His involvement in integrated circuit design began in the late 1960's, when Rockwell established its first silicon design and manufacturing capability. In recent years, his focus has been on wireless standards, with particular emphasis on the second-generation GSM and third-generation WCDMA wireless technologies. He is a Senior Member of the IEEE and has served as chairman of the IEEE Orange County Section. Quent has been a licensed amateur radio operator since 1952 and holds the call sign W6RI. He received his BE from Vanderbilt University in 1963 and an MSEE from Purdue University in 1965.

Quent resides in Orange, CA with his wife Jan. They have two daughters and four grandchildren.

CECS is delighted to have Quent as a staff member and we look forward to his contributions in improving our collaborative research programs. His technical and managerial experience will be extremely valuable as he strives to develop new collaborative research paradigms and platforms for enabling embedded systems research. Please feel free to contact Quent at 949/824-9638 or cassen@cecs.uci.edu to explore and pursue new relationships with CECS or to expand present relationships.

SRC Review

CECS was present at the Semiconductor Research Corporation's Integrated Circuits and System Sciences (ICSS) Review on February 26-27, 2003 held at the University of California, San Diego. The following presentations were made by three of our Research Affiliates; out of a total of 25 presenters scheduled in the ICSS Review:

Task 781.001 "*A Parallelizing Compiler Framework for Integrated Systems*", Professor Rajesh Gupta

Task 1046.001 "*Self-Improving Configurable IC Platforms*", Professor Frank Vahid

Task 832.001 "*System-Level Refinement and Transformation*", Professor Daniel Gajski

Task 832.002 "*System-Level Modeling*", Professor Daniel Gajski

Also attending the SRC Review from CECS were Professor Nikil Dutt and Professor Alex Orailoglu. CECS is pleased to have these research activities within the framework of the SRC research program.

Visitation

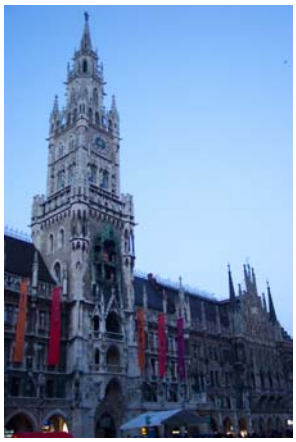
On March 15, 2003 Professor Daniel Gajski and Dr. Rainer Doemer hosted three distinguished Japanese visitors: Professor Masahiro Fujita, Department of Electrical and Computer Engineering, University of Tokyo, Tokyo, Japan, Setsuo Yamamoto, President & CEO, InterDesign Technologies, Inc., Tokyo, Japan, and Keizo Nakagawa, Senior Engineer, Innovative Information Technology Research Group, National Space Development Agency of Japan, located in Ibaraki, Japan. They met to discussion technology issues associated with heterogeneous embedded systems and explore research relationships.

Emulex Intern Event

Graduate students from the Center for Embedded Computer Systems (CECS) at the University of California, Irvine were hosted by the Emulex Corporation, 3535 Harbor Boulevard, Costa Mesa, CA. on March 24, 2003 for student summer intern interviews. Charles Nogales, Vice President, Hardware Development presented a technology and product overview. Art Martinez, Director of R&D Test and Customer Support conducted the students on a tour of the extensive testing laboratory which resulted in a lot of student questions and interest. Student interviews were conducted by Mark Karnowski, Vice President Engineering Software Development, Bill Bostick, Manager Engineering, Anthony Chung, Manager Engineering, and Dennis Dryden, Manager Engineering. Also attending the event were Bob Larsen, CECS Associate Director, Quent Cassen, CECS Research Relations Officer, Dick Koebler, Emulex Director Employment/Staffing, and Bob Wilczynski, Emulex Director Employment/Staffing. Emulex provided lunch and presented each graduate student with an Emulex "goodies" bag in appreciation of their visit.

The CECS graduate students attending the Emulex event were: Yuvraj Agarwal, Nikhil Bansai, Binayak Bhattacharyya, Bita Gorji-ara, Arun Kejariwal, Mukesh Rajan, Mehrdad Reshadi, Bo Tran, and Pei Zhang.

CECS at DATE



The Center for Embedded Computer Systems (CECS) continued its technical dominance at the Design, Automation, and Test in Europe (DATE '03) Conference held in Munich, Germany on March 3-7, 2003.

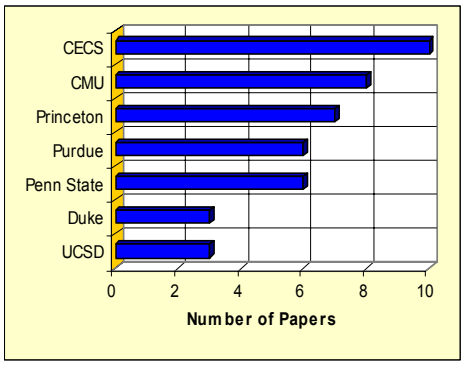
Professor Alex Orailoglu was honored by making a presentation entitled "Reducing Test Application Time Through Test Data Mutation Encoding" at the opening plenary session.

The following technical presentations were made by CECS faculty affiliates and their graduate students at DATE '03. The technical papers can be found in the conference proceedings at the cited pages:

- "*Power Efficiency Through Application-Specific Instruction Memory Transformations*", P. Petrov and A. Orailoglu, pp 30-35
- "*Low Energy Data Management for Different On-Chip Memory Levels in Multi-Context Reconfigurable Architectures*", M. Sanchez-Elez,M. Fernandez, M. Anido, H. Du, N. Bagherzadeh and R. Hermida, pp 36-41
- "*Virtual Compression Through Test Vector Switching for Scan Based Design*", W. Roa and A. Orailoglu, pp 104-109
- "*RTOS Modeling for System Level Design*", A. Gerstlauer, H. Yu and D. Gajski, pp 130-135
- "*Dynamic Conditional Branch Balancing During the High-Level Synthesis of Control-Intensive Designs*", S. Gupta, N. Dutt, R. Gupta and A. Nicolau, pp 270-275
- "*Introspection in System-Level Language Frameworks: Meta-Level or Integrated*", F. Doucet, R. Gupta and S. Shukla, pp 382-387
- "*Design and Analysis of a Programmable Single-Chip Architecture for DVB-T Base-Band Receiver*", C. Pan, N. Bagherzadeh, A. Kamalizad and A. Koohi, pp 468-473
- "*Analytical Design Space Exploration of Caches for Embedded Systems*", A. Ghosh and T. Givargis, pp 650-655
- "*Reducing Power Consumption for High-Associativity Data Caches in Embedded Processors*", D. Nicolaescu, A. Veidenbaum and A. Nicolau, pp 1064-1068
- "*On-Chip Stack Based Memory Organization for Low Power Embedded Architectures*", M. Mamidipaka and N. Dutt, pp 1082-1087

Professor Daniel Gajski served as a member of a panel discussing "*Transaction Based Design: Another Buzzword or the Solution to a Design Problem*".

The following bar chart displays the technical dominance of CECS at DATE '03.



Dutt, Gupta, Nicolau Best Paper Award

At the 16th International Conference on VLSI Design and the 2nd International Conference on Embedded Systems Design held in New Delhi, India on January 4-8, 2003, Professors Nikil Dutt, Rajesh Gupta, and Alex Nicolau and Graduate Student Sumit Gupta were conferred with the Professor A. K. Choudhary Best Paper Award by Program CoChairs M. Balakrishnan and Srimat T. Chakradhar for the paper titled "*SPARK: A High Level Synthesis Framework for Applying Parallelizing Compiler Transformations.*" Congratulations to these authors on this outstanding technical paper and the resulting international recognition which accompanies this award!

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WWW.CECS.UCI.EDU

Orailoglu Best Paper Award

At the Design, Automation, and Test in Europe (DATE '03) Conference held in Munich, Germany on March 3-7, 2003 Professor Alex Orailoglu and Graduate Student Sherief Reda received the Best Paper Award in Test for the paper at last year's DATE '02 Conference entitled "*Reducing Test Application Time Through Test Data Mutation Encoding.*" Congratulations Alex and Sherief on this outstanding technical paper in the test field and your continuing contributions to the DATE conference community!

Gajski Quoted

In an article titled "Transaction-Level Models Eyed as SOC Enabler" written by Nicolas Mokhoff that appeared in the March 17, 2003 issue of EE Times, Professor Daniel Gajski is quoted twice. The quotes originated at the Design, Automation, and Test in Europe (DATE '03) Conference held in Munich, Germany on March 3-7, 2003 in a panel discussion titled "*Transaction Based Design: Another Buzzword or the Solution to a Design Problem.*" Transaction-Level Modeling is presently undergoing refinement but is generally considered to be employing function calls to model communication protocols while VHDL/ Verilog models at the bit level. The two quotes extracted from this article follows in their entirety.

The problem is the lack of a good definition of transaction-based modeling, said panelist Dan Gajski, a University of California, Irvine professor. "Everybody has their own idea of TLM, and one EDA vendor's idea is not in synch with another's."

Ultimately, "semantics matters," said Gajski of UC Irvine. "It's not important so much what language you use to define your models. But you'd better develop them so that all understand what you mean and all can use that knowledge to develop their own models."

Dutt Appointment

The IEEE Computer Society recently selected Professor Nikil D. Dutt to participate in their Distinguished Visitors Program (DVP) for a three year term commencing January 2003. As such, he will be available to Computer Society chapters for tutorial presentations on state-of-the-art research areas aimed at benefiting the practitioners of the profession. Congratulations Nik on this noted IEEE recognition!

DAC Open House

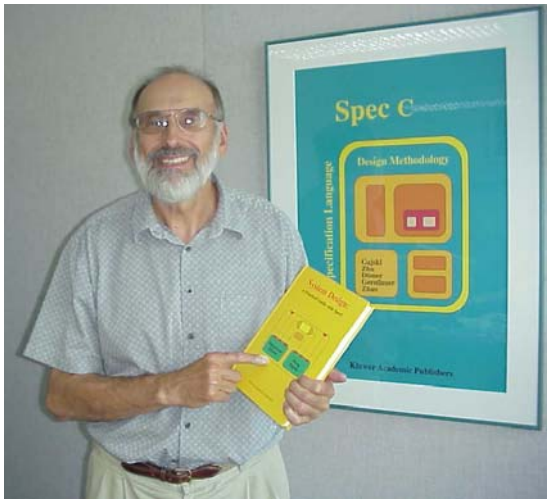
On Friday afternoon, June 6, 2003, from 2:00 PM to 5:00 PM, CECS will host an Open House to showcase our research programs. We cordially invite all interested DAC attendees to visit us. Our faculty affiliates and their graduate students will be available for exploratory discussion concerning their project activities. Light refreshments will be available so the visitation will be most enjoyable. Please plan to visit CECS while at DAC!

CECS Research Facility

Publications continued from page 6:

Focus	Title, Authors, Publication
Frequency Inheritance Algorithm	"*Dual-Mode Frequency Inheritance Algorithm for Energy Aware Task Scheduling with Task Synchronization*", R. Jejurikar, C. Periera, and R. Gupta, UCI CECS Technical Report 03-07, February 24, 2003
Communication Refinement	"*Automatic Communication Refinement for System Level Design*", S. Abdi and D. Gajski, UCI CECS Technical Report 03-08, March 8, 2003
G.729E Algorithm	"*G.729E Algorithm Optimization for ARM926EJ-S Processor*", A. Tripathi, S. Verma, and D. Gajski, UCI CECS Technical Report 03-09, March 20, 2003
Power Evaluation	"*Instruction-Based System-Level Power Evaluation of System-on-a-Chip Peripheral Cores*", T. Givargis, F. Vahid, and J. Henkel, IEEE Proceedings on Very Large Scale Integrated (VLSI) Systems, Volume 10, Number 6, December 2002, pp 856-863

Professor Profile



CECS is proud to profile Professor Daniel D. Gajski of the Department of Electrical Engineering and Computer Science in the Henry Samueli School of Engineering, University of California, Irvine (UCI), as an outstanding research affiliate. He was recently appointed as the Henry Samueli Endowed Chair in Computer System Design. He received the Dipl. Ing. in 1962 and a MS in Electrical Engineering in 1967 from the University of Zagreb, Croatia, and the PhD degree in Computer and Information Sciences from the University of Pennsylvania, Philadelphia, PA in 1974. From 1977 to 1987 he was a professor in the Department of Computer Science at the University of Illinois at Urbana-Champaign, and from 1987 to 2003 he was a professor in the School of Information and Computer Science at the University of California, Irvine. He was elected a Fellow in the Institute of Electrical and Electronic Engineers (IEEE) in 1994.

He currently serves as Director of the Center for Embedded Computer Systems (CECS) which has a research mission to embedded heterogeneous computer systems into automotive, communications, and medical applications. CECS has 15 faculty affiliates and 70 graduate students with last year's annual research budget of approximately $4,400,000.

He is the editor of the book *Silicon Compilation* (Addison-Wesley, Reading, MA, 1988), a coauthor of the books *High Level Synthesis: An Introduction to Chip and System Design* (Kluwer Academic Publishers, Norwell, MA, 1992), *Specification and Design of Embedded Systems* (Prentice Hall, Englewood Cliffs, NJ, 1994), *SpecC: Specification Language and Methodology* (Kluwer Academic Publishers, Norwell, MA, 2000) and *System-Level Design: A Practical Guide with SpecC* (Kluwer Academic Publishers, Norwell, MA, 2001), and the author of *Principles of Digital Design* (Prentice Hall, Englewood Cliffs, 1995).

Professor Gajski has published over 300 technical papers and has been awarded 5 Best Paper Awards. He has been granted 5 US patents. He has served on numerous editorial boards, program committees, conference tutorials and panels. He has delivered several invited lectures and keynote addresses.

Professor Gajski lives in University Hills with his wife Ana.

Graduate Student Profile

CECS is honored to profile Prabhat Mishra as an outstanding graduate student. He was born in Kharagpur, India, in 1973. He received a B.E. in Computer Science and Engineering from Jadavpur University, India in 1994. In 1996, he received a M.Tech. In Computer and Information Technology from the Indian Institute of Technology, Kharagpur, India. Following graduation, he worked for several years in three VLSI/EDA companies—Texas Instruments, Silicon Automation, and Synopsys. Currently, he is a fourth year PhD student and research assistant at CECS. During the summer of 2000, he was an intern at Intel, Santa Clara, CA and was a summer intern at Motorola, Austin TX in 2001 and 2002.

His research is focused on developing and implementing a top-down validation methodology for embedded systems under the supervision of Professor Nikil Dutt. His thesis topic is titled "*Architecture Description Language Driven Validation of Programmable Embedded Systems*". His research interests are in the areas of design space exploration of architectures, validation of embedded systems, and test program generation for microprocessors.

Some of Prabhat's selected publications are:

- "*Instruction Set Compiled Simulation: A Technique for Fast and Flexible Instruction Set Simulation*", Mehrdad Reshadi, Prabhat Mishra, and Nikil Dutt, Proceedings of the 40th Design Automation Conference, June 2-6, 2003

- "*Automatic Functional Test Program Generation for Pipelined Processors Using Model Checking*", Prabhat Mishra and Nikil Dutt, High Level Design Validation and Test (HLDVT), October 2002

- "*Automatic Verification of In-Order Execution in Microprocessors with Fragmented Pipelines and Multicycle Functional Units*", Prabhat Mishra, Hiroyuki Tomiyama, Nikil Dutt and Alex Nicolau, Proceedings of Design Automation and Test in Europe, March 2002, pp 36-43

- "*Automatic Modeling and Validation of Pipeline Specifications Driven by an Architecture Description Language*", Prabhat Mishra, Hiroyuki Tomiyama, Ashok Halambi, Peter Grun, Nikil Dutt and Alex Nicolau, Proceedings of the Asia and South Pacific Design Automation Conference (ASPDAC) and the International Conference on VLSI Design, January 2002, pp 458-463

- "*Functional Abstraction Driven Design Space Exploration of Heterogeneous Programmable Architectures*", Prabhat Mishra, Nikil Dutt and Alex Nicolau, Proceedings of the International Symposium on System Synthesis (ISSS), October 2001

PUBLICATIONS

The following were published by CECS faculty affiliates during the period of January 1, 2003 to March 31, 2003:

Focus	Title, Authors, Publication
Power Efficiency	"*Power Efficiency Through Application-Specific Instruction Memory Transformations*", P. Petrov and A. Orailoglu, Proceedings of the Design, Automation, and Test in Europe Conference (DATE '03), March 3-7, 2003, pp 30-35
Data Management	"*Low Energy Data Management for Different On-Chip Memory Levels in Multi-Context Reconfigurable Architectures*", M. Sanchez-Elez,M. Fernandez, M. Anido, H. Du, N. Bagherzadeh and R. Hermida, Proceedings of the Design, Automation, and Test in Europe Conference (DATE '03), March 3-7, 2003, pp 36-41
Virtual Compression	"*Virtual Compression Through Test Vector Switching for Scan Based Design*", W. Roa and A. Orailoglu, Proceedings of the Design, Automation, and Test in Europe Conference (DATE '03), March 3-7, 2003, pp 104-109
RTOS Modeling	"*RTOS Modeling for System Level Design*", A. Gerstlauer, H. Yu and D. Gajski, Proceedings of the Design, Automation, and Test in Europe Conference (DATE '03), March 3-7, 2003, pp 130-135
Branch Balancing	"*Dynamic Conditional Branch Balancing During the High-Level Synthesis of Control-Intensive Designs*", S. Gupta, N. Dutt, R. Gupta and A. Nicolau, Proceedings of the Design, Automation, and Test in Europe Conference (DATE '03), March 3-7, 2003, pp 270-275
Language Frameworks	"*Introspection in System-Level Language Frameworks: Meta-Level or Integrated*", F. Doucet, R. Gupta and S. Shukla, Proceedings of the Design, Automation, and Test in Europe Conference (DATE '03), March 3-7, 2003, pp 382-387
Single-Chip Architecture	"*Design and Analysis of a Programmable Single-Chip Architecture for DVB-T Base-Band Receiver*", C. Pan, N. Bagherzadeh, A. Kamalizad and A. Koohi, Proceedings of the Design, Automation, and Test in Europe Conference (DATE '03), March 3-7, 2003, pp 468-473
Design Space Exploration	"*Analytical Design Space Exploration of Caches for Embedded Systems*", A. Ghosh and T. Givargis, Proceedings of the Design, Automation, and Test in Europe Conference (DATE '03), March 3-7, 2003, pp 650-655
Power Consumption	"*Reducing Power Consumption for High-Associativity Data Caches in Embedded Processors*", D. Nicolaescu, A. Veidenbaum and A. Nicolau, Proceedings of the Design, Automation, and Test in Europe Conference (DATE '03), March 3-7, 2003, pp 1064-1068
Memory Organization	"*On-Chip Stack Based Memory Organization for Low Power Embedded Architectures*", M. Mamidipaka and N. Dutt, Proceedings of the Design, Automation, and Test in Europe Conference (DATE '03), March 3-7, 2003, pp 1082-1087
Design Methodology	"*System Design Methodology and Tools*", D. Gajski, J. Peng, A. Gerstlauer, H. Yu, and D. Shin, UCI CECS Technical Report 03-02, January 12, 2003
Channel Mapping	"*Channel Mapping in System Level Design*", L. Cai and D. Gajski, UCI CECS Technical Report 03-03, January 7, 2003
HDL Generation	"***HDLGen**: Architecture Description Language Driven HDL Generation for Pipelined Processors*", A. Kejariwal, P. Mishra, J. Astrom, and N. Dutt, UCI CECS Technical Report 03-04, February 3, 2003
Retargetable Framework	"***ReXSim**: A Retargetable Framework for Instruction Set Architecture Simulation*", M. Reshadi, P. Mishra, N. Bansai, and N. Dutt, UCI CECS Technical Report 03-05, February 10, 2003
Formal Verification	"*Formal Verification of Specification Partitioning*", S. Abdi and D. Gajski, UCI CECS Technical Report 03-06, March 6, 2003

Publications continued on page 4

CECS—Solving Tomorrow's Problems!

Center for Embedded Computer Systems, University of California, Irvine

***CECS** Mission Statement:*

To conduct leading-edge interdisciplinary research in embedded systems, emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.

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Looking Deeper, Reaching Farther

We all know that ***CECS*** is an acronym for the Center for Embedded Computer Systems which is located at the University of California, Irvine. Here is a thought about a deeper and more profound meaning of ***CECS***.

C*HALLENGE*–Solving Grand Challenge Problems!

What are "grand challenge problems"? They are seminal problems that are confronting government, industry, society, or the individual today, tomorrow, and in the future. They are problems, that when solved, will have profound impact on productivity, enhance individual convenience, prolong life, or make life more enjoyable. *Grand Challenge Problems* are at the heart of meaningful research.

E*DUCATION*-Education Through Research!

CECS is dedicated to producing well trained graduates that can be the future leaders in education, government, or industry. Research is the most provocative educational experience for students. In research projects, they learn to define the problem, explore potential solutions, develop an optimal solution, and document their findings. It becomes their first experience with creativity and innovative thinking.

C*OLLABORATION* – Collaboration with Industry and Government!

Effective collaborative research is when both parties develop win-win strategies. CECS wins by being exposed to relevant industrial-grade problems and industry wins by receiving creative algorithms or solutions to challenging problems. Research thrives in this wholesome exploratory environment.

The product of effective collaborative research is technology transfer. Both parties must recognize the paramount importance of technology transfer. Professors, graduate students, and industrial representatives must realize that success can only be measured by technology transfer metrics. Both parties must be winners!

S*CIENCE*—Interdisciplinary Science!

Today's complex embedded systems require the proper blending of mathematics, chemistry, physics, biology, and engineering. Bringing professors and students together from these different disciplines is not an easy task. We must constantly strive to develop research paradigms and platforms that promote interdisciplinary science.

Now when you recognize the ***CECS*** acronym or logo, we hope you will visualize a dynamic research organization dedicated to solving *Grand Challenge Problems* in embedded systems.

Bob Larsen