CECS eNEWS

Volume 2, Issue 2, April 2002

Center for Embedded Computer Systems, University of California, Irvine

Highlights

- CECS at DATE 02
- CECS at ASP-DAC
- Professor Gupta
- Professor Choi
- Publications

Inside this issue:

CECS at DATE 02

The Center for Embedded Computer Systems (CECS) at the University of California, Irvine played a dominant role at the Design, Automation and Test in Europe Conference (DATE 02) held at Le Palais des Congres, Paris, France on March 4-8, 2002. CECS had 6 professors and 4 graduate students in attendance.

The following technical presentations were made by CECS faculty affiliates and their graduate students at DATE 02 and the technical papers can be found in the conference proceedings at the cited pages:

- "Automatic Verification of In-Order Execution in Microprocessors with Fragmented Pipelines and Multicycle Functional Units", Prabhat Mishra, Hiroyuki Tomiyama, Nikil Dutt, and Alex Nicolau, pp 36—43
- "Competitive Analysis of Dynamic Power Management Strategies for Systems with Multiple Power Saving States", Sandy Irani, Sandeep Shukla, and Rajesh Gupta, pp 117—123
- "Profile-Based Dynamic Voltage Scheduling Using Program Checkpoints", Ana Azevedo, Ilya Issenin, Radu Cornea, Rajesh Gupta, Nikil Dutt, Alex Veidenbaum, and Alex Nicolau, pp 168—175
- "Gate Level Fault Diagnosis in Scan-Based BIST", Ismet Bayraktaroglu and Alex Orailodlu, pp 376—381
- "Reducing Test Application Time Through Test Data Mutation Encoding", Sherief Reda and Alex Orailoglu, pp 387—393
- "An Efficient Compiler Technique for Code Size Reduction Using Reduced Bit-Widths ISAs", Ashok Halambi, Aviral Shrivastava, Partha Biswas, Nikil Dutt, and Alex Nicolau, pp 402—408
- "Power Savings in Embedded Processors Through Decode Filter Cache", Weiyu Tang, Rajesh Gupta, and Alex Nicolau, pp 443—448
- "Test Planning and Design Space Exploration in a Core-Based Environment", Erika Cota, Luigi Carro, Alex Orailoglu, and Marcelo Lubaszewski, pp 478—485
- "A Complete Data Scheduler for Multi-Context Reconfigurable Architectures", M. Sanchez-Elez, M. Fernandez, R. Maestre, R. Hermida, N. Bagherzadeh, and F. J. Kurdahi, pp 547—552

Continued on page 5, DATE 02

CECS at ASP-DAC

Professors Pai H. Chou, Nikil D. Dutt, Daniel D. Gajski, and Rajesh K. Gupta and Graduate Students Samar Abdi and Prabhat Mishra attended the 7th Asia and South Pacific Design Automation Conference and 15th International Conference on VLSI Design (ASP-DAC/ VLSI Design 2002) held in Bangalore, India on January 7—11, 2002. Professor Chou was honored by receiving the *Best Paper Award* (see ◙ below) at the conference.

They presented the following technical papers with the cited pages from the conference proceedings:

- "Automatic Model Refinement for Fast Architecture Exploration", Junyu Peng, Samar Abdi, and Daniel Gajski, pp 332-337
- "Automatic Modeling and Validation of Pipeline Specifications Driven by an Architecture Description Language", Prabhat Mishra, Hiroyuki Tomiyama, Ashok Halambi, Peter Grun, Nikil Dutt, and Alex Nicolau, pp 458

Continued on page 5, ASP-DAC

Veidenbaum Leave

Professor Alex Veidenbaum has returned from a year 2001 leave of absence during which he helped start a wireless network infrastructure company, Bytemobile, Inc., Mountain View, CA. Bytemobile makes networking systems that allow wireless carriers to deliver faster, more reliable, and secure wireless data network access and enhanced services to their clients. The company's product solves performance problems and increases wireless bandwidth utilization via a combination of protocol acceleration, data compression, and other proprietary techniques.

The company has sold its product to several wireless carriers in the US and Europe, including the Vodaphone Group, PLC—the world's largest wireless operator. The U.K. operations of Vodaphone installed Bytemobile's network optimization platform to boost performance on its 2.5G GPRS network. Development activities are in progress on a next-generation platform for 3G networks.

Professor Veidenbaum's participation was instrumental in obtaining the first round of financing and in developing the company's first product. Employed as the Director of System Platforms, he used his expertise in networking hardware and software, systems architecture and embedded systems to define and lead the development of the company's *Macara*™ platform.

The engineering effort involved in product development, as well as the interaction with cellular network experts and networking companies, have increased his expertise and broadened his research horizons. This industrial experience has provided ideas and motivation for new research projects that Professor Veidenbaum plans to initiate now that he has returned to the Center for Embedded Computer Systems (CECS).

CHECK OUR WEB SITE!
WWW.CECS.UCI.EDU

Knight Joins CECS Staff

Dr. Susan J. Knight has joined the CECS staff as a Corporate Relations Officer. As such, she will be responsible for developing corporate and government research relations for CECS.

Susan received a BA in Biology from the College of Wooster, Wooster, Ohio. In 1992 she received an MBA in Marketing and in 1999 she received a PhD in Management from the University of California, Irvine. From 1983 to 1990 she was employed by Ansys Technologies, Inc., Laguna Hills, Ca as a toxicologist and clinical laboratory supervisor.

Susan resides in Newport Beach, CA with her husband Lee.

We are delighted to have Susan as a CECS staff member and her technical and managerial expertise, together with her charm, will benefit and enhance our embedded systems research programs.

Susan J. Knight meeting with Professor Daniel D. Gajski

Visitations

- Professor Soo-Ik Chae, School of Electrical Engineering and Computer Science, Seoul National University and Director of Inter-University Semiconductor Research Center, Seoul, Korea visited CECS on January 29, 2002. He held technical meetings with Professor Nikil D. Dutt, Professor Daniel D. Gajski, and Visiting Researcher Professor Kiyoung Choi.
- Professor Dirk Jensen, Director of the Institute for Applied Research, University of Technology and Business Administration, Offenburg, Germany visited CECS on February 11—15, 2002 to review the research progress of his Graduate Students David Berner and Alex Gluhak. These students have been performing research under the direction of Professor Daniel D. Gajski at CECS but will receive their graduate degrees from the German university.

Awards

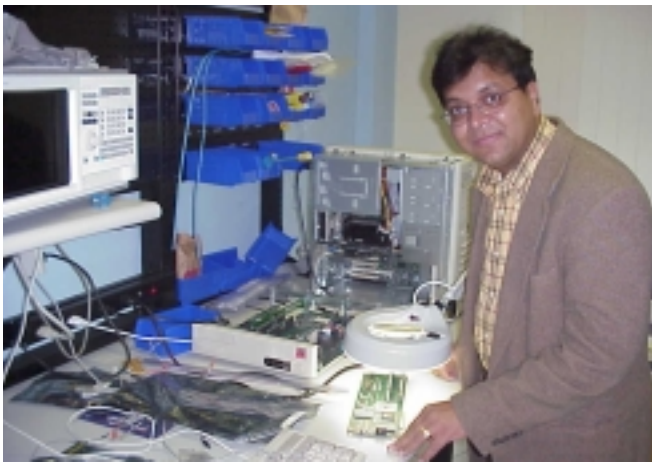
The IEEE Computer Society and its Test Technology Technical Committee recently presented the following awards to CECS faculty affiliates:

- Professor Alex Orailoglu received a *Meritorious Service Award* at the Tenth Asian Test Symposium held in Kyoto, Japan
- Professor Rajesh K. Gupta received a *Certificate of Appreciation Award* at the International Test Conference 2001 in Baltimore, MD

Contracts

- Professor Daniel D. Gajski received a ¥3,000,000 contract from the Semiconductor Technology Academic Research Center, Kohoku-ku, Japan to develop software to translate the SpecC language into C++ language for simulation and synthesis
- Professor Nikil D. Dutt received a developmental research contract from Lockheed Martin Corporation, Eagen, MN for supporting the National Experimental Platform for Hybrid and Embedded Systems Technology project

Professor Profile



CECS is proud to profile Associate Professor Rajesh K. Gupta, Department of Information and Computer Science , University of California, Irvine (UCI), as an outstanding research affiliate. Professor Gupta was born in Kanpur, India and received a B Tech from Indian Institute of Technology, Kanpur, India in 1984, MS from University of California, Berkeley in 1986, and a PhD from Stanford University in 1993. From 1986 to 1989 he was employed by Intel Corporation in microprocessor design. From 1993 to 1996 he was an Assistant Professor in the Department of Electrical and Computer Engineering, University of Illinois, Urbana– Champaign and has been a professor at UCI since 1996.

Professor Gupta is married to Neelam and they have 2 children, Anand, 10 and Hersh, 4.

Professor Gupta currently serves as Editor in Chief of the IEEE Design and Test of Computers magazine, is a member of the Board of Governors, IEEE Circuits and Systems Society, and is a member of the Editorial Boards of the IEEE Transactions on CAD/CAS and IEEE Transactions on Mobile Computing. He is a Past Chair of the IEEE CANDE Technical Committee.

Professor Gupta received a National Science Foundation Career Award in 1995, a UCI Chancellor's Award for Undergraduate Research in 1996, and was designated a Distinguished Lecturer, IEEE Circuits and Systems Society in 2001, and a Distinguished Lecturer, ACM SIGDA in 2001.

Professor Gupta is actively involved in California Institute for Telecommunications and Information Technology (CAL-IT^2) where he leads researchers in the area of software and interfaces. His current research interests are primarily focused on power management in embedded systems and mobile computing and communications. He has published over 100 technical papers and is the holder of 3 US patents.

Professor Gupta is the author of the following book:

- "Co-Synthesis of Hardware and Software for Embedded Systems", Rajesh K. Gupta, Kluwer Academic Publishers, 1995

Visitor Profile

CECS is very privileged to host for the academic year 2001-2002 a Visiting Researcher, Professor Kiyoung Choi, School of Electrical Engineering and Computer Science, Seoul National University, Seoul, Korea. He was born in Seoul and received his BS from Seoul National University in 1978, an MS from Korea Advanced Institute of Science and Technology in 1980, and PhD from Stanford University in 1989.

From 1978 to 1983 he worked for GoldStar, Inc., Seoul, Korea and from 1989 to 1991 he worked for Cadence Design Systems, Inc. in Santa Clara.

He served APCHDL'98 as a technical program co-chair and is now serving ICCAD as an executive committee member (Asian Representative). He has been serving on the program committees of CODES, ASP-DAC, and ISLPED. His primary research interests are in computer-aided microelectronic systems design including embedded systems design, hardware-software codesign, high-level synthesis, and low-power design.

He is the co-author of the following recent technical publications:

- "Behavior-to-Placed RTL Synthesis with Performance-Driven Placement", D. Kim, J. Jung, S. Lee, J. Jeon, and K. Choi, Proceedings of ICCAD, November 2001

- "Narrow Bus Encoding for Low Power DSP Systems", Y. Shin, K. Choi, and Y. Chang, IEEE Transactions on VLSI Systems, October 2001

- "Low Power Pipelining of Linear Systems: A Common Operand Centric Approach", D. Kim, D. Shin, and K. Choi, Proceedings of ISLPED, August 2001

- "Area Efficient Buffer Binding Based on a Novel Two-Port FIFO Structure", K. Rha, and K. Choi, Proceedings of CODES, April 2001

- "Scheduling Based Code Size Reduction in Processors With Indirect Addressing Mode", S. Lim, J. Kim, and K. Choi, Proceedings of CODES, April 2001

- "Partial Bus-Invert Coding for Power Optimization of Application Specific Systems", Y. Shin, S. Chae, and K. Choi, IEEE Transactions on VLSI Systems, April 2001

Continued on page 5, VISITOR PROFILE

PUBLICATIONS

The following were published by CECS faculty affiliates during the period of January 1, 2002 to March 31, 2002:

Focus	Title, Authors, Publication
Scan-Based BIST	"Cost-Effective Deterministic Partitioning for Rapid Diagnosis in Scan-Based BIST", Ismet Bayraktaroglu and Alex Orailoglu, IEEE Design and Test of Computers, January-February 2002, pp 42—53
Model Refinement	"Automatic Model Refinement for Fast Architecture Exploration", Junyu Peng, Samar Abdi, and Daniel Gajski, Proceedings of 7th Asia and South Pacific Design Automation Conference and 15th International Conference on VLSI Design (ASP-DAC/ VLSI Design 2002), pp 332-337
Automatic Modeling & Validation	"Automatic Modeling and Validation of Pipeline Specifications Driven by an Architecture Description Language", Prabhat Mishra, Hiroyuki Tomiyama, Ashok Halambi, Peter Grun, Nikil Dutt, and Alex Nicolau, Proceedings of 7th Asia and South Pacific Design Automation Conference and 15th International Conference on VLSI Design (ASP-DAC/ VLSI Design 2002), pp 458-463
Mode Modeling	"Mode Selection and Mode Dependency Modeling for Power-Aware Embedded Systems", Dexin Li, Pai H. Chou, and Nader Bagherzadeh, Proceedings of 7th Asia and South Pacific Design Automation Conference and 15th International Conference on VLSI Design (ASP-DAC/ VLSI Design 2002), pp 697-704
Automatic Verification	"Automatic Verification of In-Order Execution in Microprocessors with Fragmented Pipelines and Multicycle Functional Units", Prabhat Mishra, Hiroyuki Tomiyama, Nikil Dutt, and Alex Nicolau, Proceedings of Design, Automation and Test in Europe Conference, March 4—8, 2002, pp 36—43
Dynamic Power Strategies	"Competitive Analysis of Dynamic Power Management Strategies for Systems with Multiple Power Saving States", Sandy Irani, Sandeep Shukla, and Rajesh Gupta, Proceedings of Design, Automation and Test in Europe Conference, March 4—8, 2002, pp 117—123
Dynamic Voltage Scheduling	"Profile-Based Dynamic Voltage Scheduling Using Program Checkpoints", Ana Azevedo, Ilya Issenin, Radu Cornea, Rajesh Gupta, Nikil Dutt, Alex Veidenbaum, and Alex Nicolau, Proceedings of Design, Automation and Test in Europe Conference, March 4—8, 2002, pp 168—175
Fault Diagnosis	"Gate Level Fault Diagnosis in Scan-Based BIST", Ismet Bayraktaroglu and Alex Orailodlu, Proceedings of Design, Automation and Test in Europe Conference, March 4—8, 2002, pp 376—381
Reducing Test Time	"Reducing Test Application Time Through Test Data Mutation Encoding", Sherief Reda and Alex Orailoglu, Proceedings of Design, Automation and Test in Europe Conference, March 4—8, 2002, pp 387—393
Code Size Reduction	"An Efficient Compiler Technique for Code Size Reduction Using Reduced Bit-Widths ISAs", Ashok Halambi, Aviral Shrivastava, Partha Biswas, Nikil Dutt, and Alex Nicolau, Proceedings of Design, Automation and Test in Europe Conference, March 4—8, 2002, pp 402—408
Power Savings	"Power Savings in Embedded Processors Through Decode Filter Cache", Weiyu Tang, Rajesh Gupta, and Alex Nicolau, Proceedings of Design, Automation and Test in Europe Conference, March 4—8, 2002, pp 443—448
Test/Design Exploration	"Test Planning and Design Space Exploration in a Core-Based Environment", Erika Cota, Luigi Carro, Alex Orailoglu, and Marcelo Lubaszewski, Proceedings of Design, Automation and Test in Europe Conference, March 4—8, 2002, pp 478—485
Data Scheduler	"A Complete Data Scheduler for Multi-Context Reconfigurable Architectures", M. Sanchez-Elez, M. Fernandez, R. Maestre, R. Hermida, N. Bagherzadeh, and F. J. Kurdahi, Proceedings of Design, Automation and Test in Europe Conference, March 4—8, 2002, pp 547—552
Component Composition	"An Environment for Dynamic Component Composition for Efficient Co-Design", Frederic Doucet, Sandeep Shukla, Rajesh Gupta, and Masato Otsuka, Proceedings of Design, Automation and Test in Europe Conference, March 4—8, 2002, pp 736—743
Concurrency Re-assignment	"Automatic Concurrency Re-assignment in High Level System Models for Efficient System-Level Simulation", Nick Savoiu, Sandeep Shukla, and Rajesh Gupta, Proceedings of Design, Automation and Test in Europe Conference, March 4—8, 2002, pp 875—881

Continued on page 5, PUBLICATIONS

From page 1, DATE 02

- "An Environment for Dynamic Component Composition for Efficient Co-Design", Frederic Doucet, Sandeep Shukla, Rajesh Gupta, and Masato Otsuka, pp 736—743
- "Automatic Concurrency Reassignment in High Level System Models for Efficient System-Level Simulation", Nick Savoiu, Sandeep Shukla, and Rajesh Gupta, pp 875—881
- "Memory System Connectivity Exploration", Peter Grun, Nikil Dutt, and Alex Nicolau, pp 894—901
- "Power Efficient Embedded Processor IP's Through Application-Specific Tag Compression in Data Caches", Peter Petrov and Alex Orailoglu, pp 1065—1071

The following technical presentation was made at the Poster Session:

- "Top-Down System Level Design Methodology Using SpecC, VCC, and SystemC", Lukai Cai, Paul Kritzinger, Mike Olivares, and Daniel Gajski, pp 1137

Professor Daniel Gajski and Graduate Student Andreas Gerstlauer were presenters at a Tutorial titled "System Level Specification Beyond RTL".

Professor Nikil Dutt and Professor Rajesh Gupta served as Technical Program Chairs and they, together with Professor Daniel Gajski, were members of the Technical Program Committee.

CECS is extremely proud of its technical influence at DATE 02 which reflects the level of technical relevance in its collaborative research programs.

From page 1, ASP-DAC

- "Mode Selection and Mode Dependency Modeling for Power-Aware Embedded Systems", Dexin Li, Pai H. Chou, and Nader Bagherzadeh, pp 697-704
- Professor Gupta was a participant in the tutorial titled "Specification, Modeling, and Design Tools for System-on-Chip", pp 21-23

Professor Dutt also served on the ASP-DAC Steering Committee as the ACM SIGDA representative and Professor Gajski served on the Technical Program Committee.

From page 3, VISITOR PROFILE

- "Performance Improvement of Multi-Processor Systems Cosimulation Based on SW Analysis", J. Jung, S. Yoo, and K. Choi, Proceedings of DATE, March 2001
- "Performance Driven High-Level Synthesis with Bit-Level Chaining and Clock Selection", S. Park and K. Choi, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, February 2001
- "High-Level Synthesis Under Multi-Cycle Interconnect Delay", J. Jeon, D. Kim, D. Shin, and K. Choi, Proceedings of ASP-DAC, January 2001

Visit our site at *www.cecs.uci.edu*

From page 4, PUBLICATIONS

Focus	Title, Authors, Publication
Connectivity Exploration	"Memory System Connectivity Exploration", Peter Grun, Nikil Dutt, and Alex Nicolau, Proceedings of Design, Automation and Test in Europe Conference, March 4—8, 2002, pp 894—901
Embedded IPs	"Power Efficient Embedded Processor IP's Through Application-Specific Tag Compression in Data Caches", Peter Petrov and Alex Orailoglu, Proceedings of Design, Automation and Test in Europe Conference, March 4—8, 2002, pp 1065—1071
Aspect Oriented Programming	"Aspect + Gamma = AspectGamma: A Framework for Aspect Oriented Programming", M. Mousavai, G. Russello, M. Chaudron, M. Reniers, T. Basten, A. Corsaro, S. Shukla, R. Gupta, and D. Schmidt, UCI CECS Technical Report 02-01, March 5, 2002
Power Aware Real-Time OS	"A Software Architecture for Building Power Aware Real Time Operating Systems", Cristiano Pereira, Vijay Raghunathan, Shalabh Gupta, Rajesh Gupta, and Mani Srivastava, UCI CECS Technical Report 02-02, March 14,2002
Static Slowdown	"Efficiency and Optimality of Static Slowdown for Periodic Tasks in Real-Time Embedded Systems", Ravindra Jejurikar and Rajesh Gupta, UCI CECS Technical Report 02-03, March 19, 2002
Execution Semantics	"The Formal Execution Semantics of SpecC", Wolfgang Mueller, Ranier Doemer, and Andreas Gerstlauer, UCI CECS Technical Report 02-04, January 11, 2002
Datapath Synthesis	"Datapath Synthesis for a 16-bit Microprocessor", Haobo Yu and Daniel D. Gajski, UCI CECS Technical Report 02-05, January 22, 2002
Parity Checker	"Parity Checker Implementations in SpecC", Qiang Xie and Daniel D. Gajski, UCI CECS Technical Report 02-06, January 27, 2002

CECS—Solving Tomorrow's Problems!

Center for Embedded Computer Systems, University of California, Irvine

CECS Mission Statement:

To conduct leading-edge interdisciplinary research in embedded systems, emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.

Primary Contact:
Robert P. Larsen
Center for Embedded Computer Systems
University of California, Irvine
Irvine, CA 92697-3425
Phone: 949-824-2960
Fax: 949-824-8919
Email: larsen@cecs.uci.edu

Peeking Under The Hood

Remember the good old days when computers used to come in cabinets. The cabinets were filled with circuit boards that were densely populated with transistor cans. You could easily probe the interface between the processor and memory. Seeing the signal activity on an oscilloscope was exciting and debugging was a challenge to the system designer.

Today, approximately 95% of the microprocessors sold end up in embedded systems. These embedded systems range from robotic toys to interactive gaming systems to microwave ovens to automobile GPS systems to cellular phones to singing greeting cards. Since the microprocessors are embedded with other system functions and architectured to form a system-on-chip (SoC), the microprocessor has now become pervasive and ubiquitous. The boundaries outlining the microprocessors, RAM and ROM memories, and input-output functions can now only be ascertained by studying the photomicrographs of the SoC. You can't *peek under the hood* anymore! The old fashioned fun of playing with real-time signals has gone forever.

The operating system of embedded systems has also undergone tremendous change in the last few years. With memory dimensionality and speeds increasing and cost decreasing, the real-time operating system (RTOS) has corresponding grown more complex. Now multiple system interrupts can be fielded and concurrently processed so the user experiences no delay in accomplishing real-time tasks. Smart power saving techniques and predictive look-ahead processing strategies have made applications software the challenging design problem today. Most of the value added to embedded systems applications today comes from the embedded software.

CECS will strive to continue its inquisitive *peeking under the hood* policy with regard to its hardware and software research programs in embedded systems.

Bob Larsen