## Embedded System Design
- Embedded systems are special purpose computer systems with a wide application domain, e.g., automobiles, medical devices, communication systems, etc.
- Electronic System-Level (ESL) design models embedded systems: at different abstraction levels.
- ESL models are usually described in System-Level Description Languages (SLEDs), e.g., SystemC and SpecC.
- ESL models are typically validated by Discrete Event (DE) simulation.

## Parallel Discrete Event Simulation (PDES)
- Executes threads in the same simulation cycles (time, delta) in parallel
- Needed protection of communication and synchronization can be automatically instrumented

## Static Conflict Analysis
- Compiler builds Segment Graph (SG) derived from Control Flow Graph (CFG) of applications
- Compiler builds Segment Conflict Tables for quick look-up at runtime

## Experiments and Results
- Parallel Fibonacci calculation with timing information
- Parallel JPEG image encoder with 3 color components encoded in parallel, a sequential Huffman encoding
- Parallel H.264 video decoder with 4 slice decoders and a sequential slice reader and synchronizer
- Host: 64-bit Fedora 12 Linux with 2 6-core CPUs (Intel(R) Xeon(R) X5650) at 2.67 GHz with 2 hyper-threads per core (supports 24 threads in parallel)

## Selection of Relevant Publications
- W. Chen, K. Han, R. Dömer, “‘Parallel Discrete Event Simulation of Transaction-Level Models using the System-on-Chip Environment”, DATE 2010
- W. Chen, K. Han, R. Dömer, “‘An Algorithm to Check Out-of-Order Parallel Simulation”, ACM SIGPLAN Notices, 2010
- W. Chen, K. Han, R. Dömer, “‘ ‘Parallel Discrete Event Simulation of Transaction-Level Models using the System-on-Chip Environment’, DATE 2010
- W. Chen, et al., “‘ ‘Multi-Core Parallel Simulation of System Level Description Languages”, ASPDAC 2011
- W. Chen, K. Han, R. Dömer, “‘ ‘Multi-Core Parallel Simulation of System Level Description Languages”, ASPDAC 2011
- W. Chen, et al., “‘ ‘Multi-Core Parallel Simulation of System Level Description Languages”, ASPDAC 2011
- W. Chen, K. Han, R. Dömer, “‘ ‘Multi-Core Parallel Simulation of System Level Description Languages”, ASPDAC 2011


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**Out-of-Order Parallel Simulation for Electronic System-Level Design**
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