Synchronous Parallel Discrete Event Simulation (SPDES)

- Executes threads in the same simulation cycles (time, delta) in parallel
- Needed protection of communication and synchronization can be automatically instrumented

Traditional DE simulation  |  Synchronous PDES  |  Out-of-order PDES
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Simulation Time  |  One global time tuple  |  Local time for each thread in tuple
  |  shared by every thread and event  |  Time advance out-of-order if no conflicts exist
Event Description  |  Events are identified by their ids, i.e. event (id)  |  Events are organized as subsets with the same timestamp: (t, δ)
Simulation Thread Sets  |  READY, RUN, WAIT, WAITT,  |  Threads are organized as subsets with the same timestamp: (t, δ)
  |  JOIN, COMPLETE  |  Threads are organized as subsets with the same timestamp: (t, δ)
Threading Model  |  User-level or OS kernel level  |  OS kernel-level
Run Time Scheduling  |  Event delivery in order delta cycle loop  |  Event delivery out-of-order if no conflicts exist
  |  Time advance in order delta loop  |  Time advance out-of-order if no conflicts exist
Compile Time Analysis  |  No synchronization  |  Need synchronization protection for shared resources,
  |  No conflict analysis needed  |  e.g. any user-defined and hierarchical channels, data structures in the scheduler

Static Conflict Analysis
- Compiler builds Segment Graph (SG) derived from Control Flow Graph (CFG) of applications
- Compiler builds Segment Conflict Tables for quick look-up at runtime

**Example:**
- Segment Graph
- Segment Data Conflict Table
- Out-of-order Parallel Discrete Event Simulation with Predictions (n=244 encoder)

**Related Work:** Accelerate TLM simulation
- Distributed simulation
  - Chandye et al. [TSE’79]
  - Huang et al. [IEEE’08]
  - Chen et al. [IEEE’11]
- Hardware-based Acceleration
  - Sirowy et al. [DAC’10]
  - Nanjundappa et al. [ASPDAC’10]
  - Simha et al. [ASPDAC’13]
  - Vincio et al. [DAC’12]
- Modeling Techniques
  - Transaction-level modeling (TLM)
  - TLM temporal decoupling
  - Source-level simulation
  - Stattelmann et al. [DAC’11]
- Host-Compiled Simulation
  - Gentlau et al. [HLDVT’11]

**SMP Parallel Simulation**
- Fujimoto, [CAS&C’06]
- Chopard et al. [ICCC’06]
- Ezuheen et al. [PADS’09]
- Mello et al. [DATE’10]
- Schumacher et al. [CODES’11]
- Chen et al. [IEEEED&T’11]
- Yun et al. [TCAD’11]

**Experiments and Results**
- Parallel Fibonacci calculation timing information
- Parallel JPEG image encoder with 3 color components encoded in parallel, a sequential Huffman encoding
- Parallel H.264 video decoder with 4 slice decoders and a sequential slice reader and synchronizer
- Host: 64-bit Fedora Linux with 2 6-core CPUs (Intel® Xeon® X5650) at 2.67 GHz with 2 hyper-threads per core (supports 24 threads in parallel)