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SAMAR ABDI

CITIZENSHIP	Indian (US Visa: J1)	
EDUCATION	University of California Irvine Ph.D. Information and Computer Science (Advisor: Prof. Daniel Gajski)	December 2005
	University of California Irvine M.S. Information and Computer Science	June 2003
	Indian Institute of Technology, Kharagpur B. Tech. Computer Science and Engineering	June 1998
RESEARCH EXPERIENCE	<u>Center for Embedded Computer Systems, University of California, Irvine</u> Assistant Project Scientist	Dec. 2005 - Present
	<ul style="list-style-type: none">- Successfully proposed and led a Gigascale Systems Research Center (GSRC) project on formal equivalence verification of Transaction Level Models (TLMs).- Led an eight member team to develop and release Embedded System Environment (ESE), a toolset for automatic TLM generation and synthesis of multicore embedded systems.- Developed a transaction level design methodology for multicore embedded systems. Defined TLM semantics and devised methods for automatic TLM generation.- Developed embedded SW semantics and methods for automatic synthesis of application-specific and platform-specific embedded SW from TLMs.- Architected a parameterizable communication module, called <i>Transducer</i>, for heterogeneous multicore platforms. Developed methods for automatic Transducer RTL generation from TLMs.- Demonstrated ESE at major conferences as well online and on-site, leading to several industrial and academic collaborations.	
	<u>School of Information and Computer Science, University of California Irvine</u> Graduate Student Researcher, Design Methodology Lab	Jun. 2000-Dec. 2005
	<ul style="list-style-type: none">- Developed automatic bus-functional model generation as part of SpecC team, contributing to a successful \$3M R&D proposal to Japanese Aerospace Exploration Agency.- Developed the theory of <i>Model Algebra</i>, and formal verification algorithms for various system level refinements, such as partitioning, scheduling and routing.	
GRANTS	GSRC Task Title: "Functional Equivalence Verification of Transaction Level Models," (co-PI with D. Gajski), USD 275,000	Sep. 2006-09
	ACM Travel Grant, USD 1000	Jan. 2004
THESES	S. Abdi , "Functional Verification of System Level Model Refinements," PhD Thesis, University of California, Irvine, December 2005	

Invited Lecturer

Fall 2008, Spring 2006

- Delivered graduate course lectures on SW/HW design of multicore embedded systems.
- Created multicore JPEG Encoder design project for System-on-Chip Software Synthesis course (EECS 222C, Fall 2008).
- Created MP3 Decoder design project on Xilinx Virtex II FPGA board for System-on-Chip Design and Exploration course (EECS 298, Spring 2006).

Teaching Assistant

Sep. 2001 - Jun. 2002

- Conducted discussion and laboratory sessions for undergraduate courses on Introduction to Computer Architecture, Operating Systems Theory and Operating Systems Lab.
- Developed and graded course projects, assignments and examinations for class size varying from 30 to 120 students.

TUTORIALS

- T3 - **S. Abdi**, A. Gerstlauer, W. Ecker, C. Haubelt, J. Teich, M. Speitel, "System Level Modeling, Analysis and Synthesis of Embedded Multicore Designs," *to appear* in Design Automation and Test in Europe (DATE), March 2009
- T2 - **S. Abdi**, A. Gerstlauer, D. Gajski, "Principles of Embedded Systems: Modeling, Synthesis and Verification," in High-Level Design, VLSI Design Education Center (VDEC), Tokyo, Japan, January 2008
- T1 - D. Gajski, A. Gerstlauer, **S. Abdi**, "Concepts and Tools for Practical Embedded System Design," ASPDAC (*Covered by Japanese Nikkei Times*), January 2007

BOOK CHAPTERS

- B2 - L. Yu, **S. Abdi**, D. Gajski, "Transaction Level Model Automation for MultiCore Systems," *to appear* in "Behavioral Modeling for Embedded Systems and Technologies: Applications for Design and Implementation", editors: L. Gomes, J.M. Fernandes, IGI Global Publishers
- B1 - D. Gajski, **S. Abdi**, "Transaction Level System Modeling," in Practical Design Verification, editors: D. Pradhan, I. Harris, Cambridge University Press ISBN-13: 9780521859721

**JOURNAL
PUBLICATIONS**

- J4 - **S. Abdi**, L. Yu, Y. Hwang, D. Gajski, "Automatic Generation of Timed TLMs for Multicore Systems," *in submission* to IEEE Transactions of Computer Aided Design (TCAD)
- J3 - **S. Abdi**, D. Gajski, I. Viskic "Model Based Synthesis of Embedded Software," *to appear* in Journal of Software (JoSW), special issue Best of SEUS 2008, Spring 2009
- J2 - R. Doemer, A. Gerstlauer, J. Peng, D. Shin, L. Cai, H. Yu, **S. Abdi**, D. Gajski, "System-on-Chip Environment: A SpecC-Based Framework for Heterogeneous MPSoC Design," EURASIP Journal on Embedded Systems (JES), vol. 2008
- J1 - **S. Abdi**, D. Gajski "Verification of System Level Model Transformations," in Springer International Journal of Parallel Programming, February 2006

**CONFERENCE
PUBLICATIONS**

- C15 - H. Cho, **S. Abdi**, D. Gajski, "Automatic Generation of RTL Communication Modules for Multicore Embedded Systems," *in submission* to Design Automation Conference 2009
- C14 - **S. Abdi**, G. Schirner, I. Viskic, H. Cho, Y. Hwang, L. Yu., D. Gajski, "Hardware Dependent Software Synthesis for Many-core Embedded Systems," *to appear* in Asia and South Pacific Design Automation Conference (ASP-DAC), January 2009, Yokohama, Japan

- C13 - Y. Hwang, **S. Abdi**, D. Gajski, "Cycle-approximate Retargetable Performance Estimation at the Transaction Level," in Design Automation and Test in Europe (DATE), March 2008, Munich, Germany, pp 3-8
- C12 - L. Yu, **S. Abdi**, "Automatic SystemC TLM generation for custom communication platforms," in International Conference on Computer Design (ICCD), October 2007: 41-46
- C11 - H. Cho, **S. Abdi**, D. Gajski, "Interface synthesis for heterogeneous multi-core systems from transaction level models," in Languages, Compilers and Tools for Embedded Systems (LCTES), March 2007, San Diego, CA, USA pp 140-142
- C10 - I. Viskic, **S. Abdi**, D. Gajski, "Automatic generation of embedded communication SW for heterogeneous MPSoC platforms," in Languages, Compilers and Tools for Embedded Systems (LCTES), March 2007, San Diego, CA, USA pp 143-145
- C9 - H.Cho, **S. Abdi**, D.Gajski, "Design and Implementation of a Duplex AMBA-TMS Transducer," in Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC) , January 2006, Yokohama, Japan, pp 126-127
- C8 - **S. Abdi**, D. Gajski, "Validation of System Level Static Scheduling," Proceedings of Design Automation and Test in Europe (DATE), March 2005, Munich, Germany, pp 542-547
- C7 - **S. Abdi**, D. Gajski, "A Formalism for Functionality Preserving System Level Transformations," Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC) , January 2005, Shanghai, China, pp 139-144
- C6 - J. Peng, **S. Abdi**, D. Gajski, "A Clustering Algorithm for Optimization of HW/SW Synchronization," Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC) , January 2005, Shanghai, China, pp 965-968
- C5 - **S. Abdi**, D. Gajski, "Automatic Generation of Equivalent Architecture Model from Functional Specification," Proceedings of ACM Design Automation Conference (DAC) , June 2004, San Diego, CA, USA, pp 608-613
- C4 - **S. Abdi**, D. Gajski, "On Deriving Equivalent Architecture Model from System Specification," Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), January 2004, Yokohama, Japan, pp 322-327
- C3 - D.Shin, **S. Abdi**, D. Gajski, "Automatic Generation of Bus Functional Models from Transaction Level Models," Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), January 2004, Yokohama, Japan, pp 756-758
- C2 - **S. Abdi**, D. Shin, D. Gajski, "Automatic Communication Refinement for System Level Design," Proceedings of ACM Design Automation Conference (DAC), June 2003, Anaheim, CA, USA, pp 300-305
- C1 - J. Peng, **S. Abdi**, D. Gajski, "Automatic Model Refinement for Fast Architecture Exploration," Proceedings of Joint Asia and South Pacific Design Automation Conference (ASP-DAC) and VLSI Design Conference, January 2002, Bangalore, India, pp 332-337
- WORKSHOP PUBLICATIONS
- W4 - D. Gajski, **S. Abdi**, I. Viskic, "Model Based Synthesis of Embedded Software," Software for Embedded and Ubiquitous Systems (SEUS), October 2008, Capri Island, Italy, pp 21-33
- W3 - L. Yu, **S. Abdi**, "Automatic TLM Generation for C based MPSoC Design," High Level Design Validation and Test (HLDVT) , November 2007, Irvine, USA
- W2 - **S. Abdi**, D.Gajski, "Transaction Routing and its Verification by Functionality Preserving Transformations," High Level Design Validation and Test (HLDVT), November 2006, Monterey, USA

W1 - **S. Abdi**, D. Gajski, "Model Validation for Mapping Specification Behaviors to Processing Elements," High Level Design Validation and Test (HLDVT) , November 2004, Sonoma, CA, USA

INVITED TALKS

I4 - "Transaction Level Design of Multicore Systems" *to appear* in The Future of ESL Synthesis, Friday Workshop at Design Automation and Test in Europe (DATE), March 2009

I3 - "Design of Multicore Embedded Systems with ESE," SoC Design Methodology Workshop, National Tsinghua University, Hsinchu, Taiwan, September 2008

I2 - "Embedded System Environment: Technical Overview," Freescale Semiconductor, Austin TX, June 2008

I1 - **Keynote Speaker**, "System Verification and Debugging: A New Challenge," Verify Seminars, September-October 2003

PROFESSIONAL DOCUMENTS

"Embedded System Environment (ESE), Version 2.0: Tutorial and User Manual," November 2008

"System-on-Chip Environment (SCE), Version 2.2.0 Beta: Tutorial," July 2003

AWARDS

Young Student Award, Design Automation Conference **2001, 2004**

National Talent Search Scholar, Govt. of India **1992-98**

INDUSTRIAL EXPERIENCE

Cadence Design Systems, India

Member of Technical Staff **June 1998 - June 2000**

- Developed and maintained Verilog and VHDL native compiled simulation (NCSim) tools (>1 million lines of code). Performed critical customer support and upgrades to simulation kernel.
- Implemented waveform viewing features to simulator for debugging of HDL models.

PROFESSIONAL SERVICE

Program Committee Member for ASPDAC 2009, HLDVT 2007-08, IESS 2007

Technical Session Chair for ASPDAC 2009, IESS 2007, ASPDAC 2004

Reviewer for DAC, TCAD, TCOMPUTER, IESS, HLDVT, TECS, JASA, ISSS, DATE, ASPDAC

PROFESSIONAL MEMBERSHIPS

Faculty Member: Gigascale Systems Research Center, UC Berkeley **2006-Present**

Member: ACM-Special Interest Group on Design Automation **2003-Present**

SKILLS

Programming languages: C++, C, SystemC, VHDL, Verilog, Java, x86 assembly

Tools: Xilinx EDK/ISE, ModelSim, NCSim, Microsoft Visual Studio, LLVM

Operating systems: Linux, Windows, Windows CE, Xikernel RTOS

MISCELLANEOUS

Languages: English (fluent), Hindi (native)

Communication: Excellent presentation and writing skills

Outreach: K-12 Math Festival Volunteer for Long Beach City Schools

REFERENCES

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