AER Circuits, Systems, and Tools

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Outline

• Introduction: AER, a technology for building large scalable neuromorphic systems

• Some useful circuits: - calibration
  - LVDS interface

• Some example systems at IMSE: - spatial contrast retina
  - mixed-mode convolution chip
  - fully digital convolution chip

• HW Tools from Sevilla: - some FPGA-based PCBs
  - example use in CAVIAR

• SW Tool: - Behavioral Matlab Simulator
  - Example 1: neocognitron emulation
  - Example 2: texture classification
Conventional Vision Sensing/Processing/Recognition

FRAMES

• Feature Extraction Stages
• Feature Combination Stages
• Classification/Decision Stages
Biology

Recognition Delay < 150ms

Simon Thorpe
Nature 1996
Biology

Recognition Delay < 150ms

- feedforward
- 1 spike/neuron

Simon Thorpe Nature 1996
Serre & Poggio (MIT)

Ventral Stream Model for Immediate Recognition

- projection field processing
- short-range & dense for first layers
- long-range & sparse for later layers
- hard-wired for first layers
- plastic for later layers
- first layers: massive 2D filtering for different angles and scales
- first layers: basic feature extraction
- later layers: grouping of features -> abstractions
AER (Address Event Representation)
Feature Extraction

(AER Convolution Chip)

Matrix of integrators in the receiver chip
• Events are routed to neighbors through local on-chip routing tables
• Any arbitrary multi-layer feed-forward + feed-back hierarchy can be programmed
• LVDS links allow low-power high-speed event traffic
• Each tile could be a 128x128 programmable kernel convolution chip with local re-routing and remapping capability
• Hundreds of convolution chips can be fit in a ‘Cortical Tissue’ PCB

CORTICAL TISSUE

128 x 128 AER convolution chip

AER serial LVDS links
Computing Power of one such Cortical Tissue PCB

- 120 chips & 436 AER inter-chip links
- Each chip 128x128 neurons and kernel up to 128x128
- Total of 2M neurons
- Total of 32G synapses
- If each AER link requires 30ns per AE:
  - 14Geps (interchip)
  - 238 Tconnections/sec
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Calibration in Neuromorphic Cells

- large arrays
- small cell area
- very low currents (nano-pico amsp)
- high inter-pixel mismatch:
  \[ \sigma \approx 10-20\% \Rightarrow 6\sigma \approx 60-120\% \]
Compact Calibration Circuit


- Ladder-based digi-MOS:

\[ g(w_{cal}) \]

3 \( N + 1 \) unit transistors

\( N = \text{number of bits} \)
one point calibration

\[ I_{out}(\mu A) \]

\[ w_{DAC} \]
max current: ~2.5µA
unit transistor: 5 x 5µm²

max error: 6σ~3-4%
(~ 4-bit precision)
For Higher Precision

![Circuit Diagram]

- **Figure (a)**: A circuit diagram showing a chain of switches labeled with bits $b_{N-1}$ to $b_0$ and control signals $G$, $S$, and $V_{\text{dummy}}$.
- **Figure (b)**: A simpler circuit showing a control signal $g(w_{cal})$ and a switch $w_{cal}$.

- The circuit in (a) includes a calibration process for each bit, with $2^N I$, $4I$, $2I$, and $I$ representing the calibration currents for bits $N$, 0, 1, and 2, respectively.

---

Note: The diagram contains electronic symbols and annotations indicating the flow of currents and control signals, as well as the calibration process for each bit.
New Concept based on parallel/series MOS association

[Galup-Montoro et al., IEEE JSSC 1994]

From EKV/ACM models: \( I_{DS} = \frac{W}{L} \left[ f(V_G, V_S) - f(V_G, V_D) \right] \)

- Generic:  
  - parallel: \( \left( \frac{W}{L} \right)_{eq} = \left( \frac{W}{L} \right)_A + \left( \frac{W}{L} \right)_B \)
  - series: \( \left( \frac{W}{L} \right)_{eq} = \frac{\left( \frac{W}{L} \right)_A \left( \frac{W}{L} \right)_B}{\left( \frac{W}{L} \right)_A + \left( \frac{W}{L} \right)_B} \)

Consequently,

- Series association with equal \( W \),  \( \rightarrow L_{eq} = \sum L_i \)
\[ W/(L/2) \]
\[ W/(L/4) \]
\[ W/(L/8) \]
\[ \ldots \]
\[ W/(L/2^N) \]
\[ W/(L/2) \]
\[ W/(L/4) \]
\[ W/(L/8) \]
\[ \cdots \]
\[ W/(L/2^N) \]

\[ \frac{W}{L} = \frac{W}{Lg(w_{cal})} \]
$S_{n-1}$

$S_0$

$G$

$D$

$W/(L/2)$

$W/(L/4)$

$W/(L/8)$

$W/(L/2^N)$

$S_{n-1}$

$S_0$

$G$

$D$

$(2W)/L$

$(4W)/L$

$(8W)/L$

$(2^N W)/L$
\[ \frac{W}{L} = \frac{W}{\text{Lg}(w_{cal})} \]
Ical

4-bit Monte Carlo Simulation

sub-pA current mirror

$$\frac{I_{cal}}{I_{REF}} = \frac{W/L}{W/(L + Lg(w_{cal}))}$$

$$I_{cal} = I_{REF} \times (1 + g(w_{cal}))$$

want to avoid large up-steps

want to approach this line

nice down-steps
Before Calibration

\[ I_{\text{cal}} \]

\[ I_{\text{ref}} \]

(a)

After Calibration (at 3nA)

\[ I_{\text{cal}} \]

\[ I_{\text{ref}} \]

(b)

110% (0 bits)

4% (4.6 bits)
• we don’t need nice precise stairs, but good coverage
• we like down-steps
• we like randomness
• we use same $W = 2\mu m$ and $L = \{3.0, 1.8, 1.8, 1.0, 0.7\}$ for a 5-bit digi-MOS
• we don’t need nice precise stairs, but good coverage
• we like down-steps
• we like randomness
• we use same $W = 2\mu m$ and $L = \{3.0, 1.8, 1.8, 1.0, 0.7\}$ for a 5-bit digi-MOS
And we want two additional features:

- FEATURE-1: no recalibration when changing operating current
- FEATURE-2: take maximum advantage of calibration range: B>A but B~A

-want B above A
-want B close to A
FEATURE-1: no recalibration

• for simple current mirror

\[
\frac{W}{L} g(w_{cal}) \quad I_{cal} \quad I_{REF}
\]

\[
\frac{W}{L} \quad I_{b} \quad w_{cal}
\]

<table>
<thead>
<tr>
<th>$I_{REF}$</th>
<th>$I_{cal}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$10^{-11}$</td>
<td>$10^{-10}$</td>
</tr>
<tr>
<td>$10^{-9}$</td>
<td>$10^{-8}$</td>
</tr>
<tr>
<td>$10^{-7}$</td>
<td>$10^{-6}$</td>
</tr>
</tbody>
</table>

bit precision

Mirror Current

nocalib 3n 1p 10p 100p 1n 10n 100n 1u

$10^{-11}$ $10^{-10}$ $10^{-9}$ $10^{-8}$ $10^{-7}$ $10^{-6}$

$I_{REF}$

plot
FEATURE-1: no recalibration

- by adding peripheral translinear tuning:

\[ I_1 I_2 = I_{i3} I_4; I_{i3} = I_3/(2 + g(w_{cal})) \]

\[ I_{oi} = \frac{I_1 I_2}{I_3} (2 + g(w_{cal})) \]

- \( I_3 \) is constant, so currents through branch \( I_{i3} \) is constant

- \( M_1 \) has similar bias condition than \( M_3 \), so \( I_1 \) is also kept constant

- \( M_2 \) has similar bias condition than \( M_4 \), so \( I_{oi} \) is scaled by changing only \( I_2 \)
FEATURE-2: approach A and B

\[ I_{oi} = \frac{I_1 I_2}{I_3} (g(w_{adj}) + g(w_{cal})) \]

local for each pixel

global for array

(a) \( w_{adj} = 31 \)
(b) \( w_{adj} = 20 \)
(c) \( w_{adj} = 0 \)
Experimental prototype CMOS 0.35μm

- single current source calibrated at 10nA
Experimental prototype CMOS 0.35um

- single current source calibrated at 10nA
• DAC: five current sources calibrated at 10nA, 5nA, 2.5nA, 1.25nA, 625pA and 16°C
Another Translinear Tuning Circuit [TCAS-II, in Press]

- achieves higher precision (7-bit) using a 5-bit circuit
- degrades more rapidly when changing bias conditions
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The bit serial LVDS AER interface

- Several options are possible:
  - Transmitting data and clock by different physical paths.
  - Recovering the clock using a PLL-based circuit.
  - Extracting the clock from the receiver data (e.g. using a Manchester coding).

A transition takes place every $T_b$!
The bit serial LVDS AER interface

- In AER links we will need:
  - Keeping the receiver synchronized in the silent periods.
  - Detecting a new address start.
  - Implementing a fast and robust synchronization scheme.
The bit serial LVDS AER interface (IV)

- Fast synchronization is a must in AER links because the events are generated in an asynchronous way.
- A Manchester coding scheme allows the receiver to recover the clock directly from the data flow.
The bit serial LVDS AER interface (V).

Transmitter

- **clk**
- **transmitted_data**
- **Manchester**

Receiver

- **recovered_clock**
- **recovered_data**

Logical timing:

- $T_b = 1\text{ns}$

Notations:

- AER Data
- Transmitter
- Receiver
- Deserializer
- Manchester Coder
- LVDS driver
- LVDS Receiver
- Manchester Decoder
- Clock Generator
- Clock Recovery
- Ack
- Req
Transmitter circuit

Serializer circuit

Manchester coder
The only requirement for the CDR design is that five delay elements must introduce a delay between $T_b/2$ and $T_b$. 
Receiver circuitry

- A Delay Locked Loop is used to fix the delay introduced by the inverters. The phase difference between the reference clock and a 360°-delayed version of it is compared and the delay elements control voltage is changed depending on the phase error.
Burst mode operation (II)

Control voltage generator circuit

- $V_{up}$
- UP
- DOWN
- $V_{down}$

- $R_1$
- $C_1$
- $C_2$

- $R_3$
- $C_3$

- SW1
- SW2

- resetPD

ADC, Latch, DAC
• ST 90nm CMOS
• 50cm cat5E UTP cable
• 5cm microstrip traces
• LVDS pads
• ESD protection circuits
• LVDS drivers available from ST 90nm library
• connectors
• simulated for all technology process corners
• temperature range 0-80ºC
• 5% variation in Supply Voltage
Simulation results

Signals involved in the clock recovery when the loop is locked

Control voltage

Recovered clock

Manchester data
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What we want:

- Retina with AER output
- Output frequency proportional to instantaneous *Spatial Contrast*
- *Spatial Contrast* computation not limited to nearest neighbors
- Fully Asynchronous output (no frames)
- low mismatch (FPN)
What we want:

- Retina with AER output
- Output frequency proportional to instantaneous Spatial Contrast
- Spatial Contrast computation not limited to nearest neighbors
- Fully Asynchronous output (no frames)
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What we want:

- Retina with AER output
- Output frequency proportional to instantaneous *Spatial Contrast*
- *Spatial Contrast* computation not limited to nearest neighbors
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\[
OutputFreq = f(I_{\text{photo}}(x, y), I_{\text{neighbours}})
\]
What we want:

- Retina with AER output
- Output frequency proportional to instantaneous *Spatial Contrast*
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- Fully Asynchronous output (no frames)
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*use of diffusers*
What we want:

- Retina with AER output
- Output frequency proportional to instantaneous *Spatial Contrast*
- *Spatial Contrast* computation not limited to nearest neighbors
- Fully Asynchronous output (no frames)
- low mismatch (FPN)

- each pixel decides when to generate an event
- there is no global periodic reset (no frames)
What we want:

- Retina with AER output
- Output frequency proportional to instantaneous *Spatial Contrast*
- *Spatial Contrast* computation not limited to nearest neighbors
- Fully Asynchronous output (no frames)
- low mismatch (FPN)

in-pixel calibration
Calibration Technique

Active Current Generation

- Active current sources, controlled digitally
- Can be used as a Current DAC
$w_{DAC} = \{b_4, b_3, b_2, b_1, b_0\}$
Example Layout for 0.35\(\mu m\) CMOS 5-bit digi-MOS

- unit transistor \(W = L = 3\mu m\)
Spatial Contrast Computation

Michelson Contrast: \( I_{cont}(x, y) = I_{ref} \frac{I_{photo}(x, y) - I_{avg}(x, y)}{I_{photo}(x, y) + I_{avg}(x, y)} \)

Weber Contrast: \( I_{cont}(x, y) = I_{ref} \frac{I_{photo}(x, y) - I_{avg}(x, y)}{I_{avg}(x, y)} \)

Simple Ratio Contrast: \( I_{cont}(x, y) = I_{ref} \frac{I_{avg}(x, y)}{I_{photo}(x, y)} \)
Calibrating for Mismatch

Sums/Subtractions & Multiplications/Division:

\[
I_o = I_1 \frac{I_2 - I_3}{I_4} \quad \rightarrow \quad I_o + \Delta_o = (I_1 + \Delta_1) \frac{(I_2 + \Delta_2) - (I_3 + \Delta_3)}{(I_4 + \Delta_4)}
\]

\[
I_o + \Delta_o \approx \frac{I_1 I_2}{I_4} (1 + \Delta_1 + \Delta_2 - \Delta_4) - \frac{I_1 I_3}{I_4} (1 + \Delta_1 + \Delta_3 - \Delta_4)
\]
Calibrating for Mismatch

Sums/Subtractions & Multiplications/Divisions:

\[ I_o = I_1 \frac{I_2 - I_3}{I_4} \rightarrow I_o + \Delta_o = (I_1 + \Delta_1) \frac{(I_2 + \Delta_2) - (I_3 + \Delta_3)}{(I_4 + \Delta_4)} \]

\[ I_o + \Delta_o \approx \frac{I_1 I_2}{I_4} (1 + \Delta_1 + \Delta_2 - \Delta_4) - \frac{I_1 I_3}{I_4} (1 + \Delta_1 + \Delta_3 - \Delta_4) \]

Only Multiplications/Divisions:

\[ I_o = I_1 \frac{I_2}{I_4} \rightarrow I_o + \Delta_o = (I_1 + \Delta_1) \frac{(I_2 + \Delta_2)}{(I_4 + \Delta_4)} \]

\[ I_o + \Delta_o \approx \frac{I_1 I_2}{I_4} (1 + \Delta_1 + \Delta_2 - \Delta_4) \]

only one calibration current per pixel
Asynchr. Comm.

**Photo Sensor**

\[ I_{\text{photo}} \]

Diffusers

\[ I_{\text{avg}} \]

Translinear Circuit

\[ I_{\text{cont}} \]

**i&f**

\[ f_{\text{cont}} \]

Asynchr. Comm.

\[ V_{\text{slc}} \]

**Diffusers**

\[ I_{\text{photo}(x,y)} \]

Translinear Multiplier

\[ I_{\text{ref}} \]

\[ I_{\text{cont}(x,y)} \]

\[ I_{\text{avg}(x,y)} \]

Diffusive Network

\[ I_{\text{bias}} \]

\[ I_{\text{photo}(x,y)} \]

\[ I_{\text{cont}(x,y)} \]

\[ I_{\text{cont}(x,y)} \]

\[ I_{\text{cont}(x,y)} \]
Asynchr.
Comm.

Photo
Sensor

Diffusers

Translinear
Circuit

i&f

f_cont

Asynchr.
Comm.

I_{photo}

I_{avg}

I_{photo}

I_{cont}

I_{cont}

I_{avg}

I_{ref}

I_{cont}(x,y)

I_{avg}(x,y)

I_{photo}(x,y)

I_{photo}(x,y-
1)

I_{bias}

V_{slc}

Translinear Multiplier

Diffusive
Network
\[ f_{\text{cont}}(x, y) = \frac{I_{\text{ref}}}{C(V_{\text{reset}} - V_{\text{ref}})} \frac{I_{\text{avg}}(x, y)}{I_{\text{photo}}(x, y)} \]
\[ f_{cont}(x, y) = \frac{I_{ref}}{C(V_{reset} - V_{ref})} \frac{I_{avg}}{I_{photo}} \times \left( 1 + \frac{\Delta I_{ref}}{I_{ref}} - \frac{\Delta V}{V_{reset} - V_{ref}} \frac{\Delta C}{C} + \frac{\Delta I_{avg}}{I_{avg}} \frac{\Delta I_{photo}}{I_{photo}} + \Delta_{TL} \right) \]

\[ = f_{nominal}(1 + \Delta(x, y)) \]
\[
f_{\text{cont}}(x, y) = \frac{I_{\text{ref}}}{C(V_{\text{reset}} - V_{\text{ref}})I_{\text{photo}}} \times \left(1 + \frac{\Delta I_{\text{ref}} + I_{\text{cal}}}{I_{\text{ref}}} - \frac{\Delta V}{V_{\text{reset}} - V_{\text{ref}}} - \frac{\Delta C}{C} + \frac{\Delta I_{\text{avg}}}{I_{\text{avg}}} - \frac{\Delta I_{\text{photo}}}{I_{\text{photo}}} + \Delta_{\text{TL}}\right)
\]

\[
= f_{\text{nominal}}\left(1 + \Delta(x, y) + \frac{I_{\text{cal}}}{I_{\text{ref}}}\right)
\]
\[ f_{cont}(x, y) = \frac{I_{\text{ref}}}{C(V_{\text{reset}} - V_{\text{ref}})I_{\text{photo}}} \times \left( 1 + \Delta(x, y) + \frac{I_{\text{cal}}(w_{\text{cal}})}{I_{\text{ref}}} \right) \]
## CMOS test prototype in AMS 0.35µm

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Array size</td>
<td>32 x 32</td>
</tr>
<tr>
<td>Pixel size</td>
<td>58µm x 56µm</td>
</tr>
<tr>
<td>Pixel components</td>
<td>104 transistors + 1 capacitor</td>
</tr>
<tr>
<td>Photodiode quantum efficiency</td>
<td>0.34 @ 450nm</td>
</tr>
<tr>
<td>Fill factor</td>
<td>3%</td>
</tr>
<tr>
<td>Pixel current consumption</td>
<td>20nA @ 1keps, 1nA @ standby</td>
</tr>
<tr>
<td>Matching before calibration (indoor light)</td>
<td>57%</td>
</tr>
<tr>
<td>Matching after calibration (indoor light)</td>
<td>6.6%</td>
</tr>
<tr>
<td>Contrast sensitivity</td>
<td>10 Hz/%relative contrast @ 400Hz DC</td>
</tr>
<tr>
<td>Range of diffusers</td>
<td>~10 pixels</td>
</tr>
<tr>
<td>Noise standard deviation</td>
<td>~6% fluctuation of spike rate</td>
</tr>
<tr>
<td>Dark current</td>
<td>~500fA</td>
</tr>
<tr>
<td>Handshaking cycle</td>
<td>15ns/ev (shorting Ack and Rqst)</td>
</tr>
</tbody>
</table>
Indoor light

\[ \frac{\sigma_f}{f_{\text{central}}} = 57\% \]

\[ \frac{\sigma_f}{f_{\text{central}}} = 6.6\% \]
Uncalibrated vs. Calibrated for indoor illumination:

- Indoor illumination
  - Uncalibrated image
  - Calibrated image

- Bright illumination
  - Uncalibrated image
  - Calibrated image
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AER Convolution Chip

Matrix of integrators in the receiver chip

Pixel Array

AER-output

F(p,q)

(x,y)

(x-neighbourhood)

Kernel-RAM

I/O

Address

Rqst

Ack

Monostable

Control Block

High Speed Clock

BUS

x1

y1

Xpq

F(p,q)

AER-output

Pixel Array

(x,y)
Pixel

(a) Input spikes

(b) Positive and negative spikes

$V_c$ 

$E_{ref}$ 

$I_w$ 

$E_{reset}$ 

$E_{ref}^+$ 

$E_{ref}^-$ 

$E_{out}^+$ 

$E_{out}^-$
Pixel

(a) Input spikes $I_w$ to $V_c$ then to out

(b) Positive spikes $+I_w$ to $V_c$ then to out+

Negative spikes $-I_w$ to $E_{reset}$, then to out-

$V_{spike}$, $V_{off}$, $I_{out}$, $I_w$
Pixel

(a) Input spikes

(b) Positive spikes

(c) Negative spikes

V_spike = V_off

I_w = I_cal_N

V_c = E_ref

Out spikes

E_reset

E_ref+

E_ref−

I_w

Io

Out−

CapSign

Pulse−

Pulse+

V_gndA

V_gndB

V_offp

V_offn

M_{p0}

M_{p1}

M_{p2}

M_{p3}

M_{n0}

M_{n1}

M_{n2}

M_{n3}

Logic

Positive Event Block

Negative Event Block
• pixel current pulses may range from ~1pA to ~1µA
• pixel size $90\mu m \times 90\mu m$
• 364 transistors + 1 capacitor
• kernel weight resolution: 4 bit
• calibration register resolution: 5 bit
• interpixel mismatch (after calibration): $< 2\%$
kernel

Input A

Output 1

Input B

Output 2
PCB with 4 32x32 Conv. Chips + Event Routing
kernel \{-3,+3,+7\}
Input Output

kernel \{-3,+3,+7\}

S-shaped propeller
Rectilinear propeller

Short Frame Time (0.05ms) Long Frame Time (150ms)
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Fully Digital Convolution Chip (I): Architecture

- Array of pixels (Digital)
- Random Access Memory (Kernel programmed)
- Horizontal Shift Block
- 2’s complement
- Synchronous controller (input communication)
- AER block (output communication)
- Configuration registers
Fully Digital Convolution Chip (II): The Pixel

- Arithmetic unit
- Accumulator (18 bits)
- Comparator
- AER output communication
Fully Digital Convolution Chip (III): Layout

Chip Size: 5.4mm x 4.3mm

Photograph of the fabricated chip
Experimental Results (I): Single Chip Configuration

Input image

High-Pass Kernel

Measured output

Ideal output
**Experimental Results (II): Multichip Configuration**

- **Input image**
- **Gabor vertical edge-extraction**
- **Measured output**
- **Ideal output**
Experimental Results (III): Multichip Configuration

Input image

Gabor vertical edge-extraction

Measured output

Ideal output
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PCI-AER

- sequences AEs from the computer out to the AER port
- transforms video-frames to AER in real-time (uses rate coding)
- captures and timestamps AEs from the AER port into the computer
- peak rate 15Meps, sustained rate 10Meps.
- FPGA: Spartan-II
- performs bus mastering
USB-AER

- USB connection to computer
- **sequencer**: either frame-AER or recorded AE-player (up to 25Meps)
- **monitor**: either AER-frame or timestamping and data-logging (up to 25Meps)
- data logging/playing up to 512 Kevents (**very useful for multi-lab experiments**)  
- **mapper** (stand-alone mode) 25Meps; mappings from 1-1 up to 1-8
- VGA output
- firmware loaded through USB or MMC/SD card
Splitter/Merger

- uses a CPLD as the communication center
- splitter: 1 to 4
- merger: 4 to 1
- reconfigured by jumpers
- delay introduced: 20ns
USB2AER

- uses high speed USB2 (up to 6Meps between AER-port and computer)
- only functionalities: AE monitor & AE sequencer (AER-port to/from computer-USB2)
- monitoring & sequencing can be simultaneous
- no FPGA, just a CPLD (timestamping) and a microcontroller (for USB traffic management)
- USB powered
- compatible with jAER viewers and Matlab
AER-Robot

- for controlling motors directly from an AER bus
- each PCB has 4 motor connectors
The CAVIAR Vision System

(a) Diagram of the system components:
- 1: moving stimulus
- 2: mirror
- 3: retina chip
- 4: USB monitor
- 5: USB mapper
- 6: Splitter Merger
- 7: USB monitor
- 8: USB mapper
- 9: object chip
- 10: USB monitor
- 11: Microcontroller
- 12: USB mapper
- 13: delay line chip
- 14: USB mapper
- 15: learning chip

(b) Image of the CAVIAR Vision System setup.
• 4-layer system
• 45k neurons
• up to 5M synapses
• 12Geps
• 1-3ms latency for tracking
• scalable w/o performance degration
Latency Measurement
Outline

• Introduction: AER, a technology for building large scalable neuromorphic systems

• Some useful circuits:  
  - calibration
  - LVDS interface

• Some example systems at IMSE:  
  - spatial contrast retina
  - mixed-mode convolution chip
  - fully digital convolution chip

• HW Tools from Sevilla:  
  - some FPGA-based PCBs
  - example use in CAVIAR

• SW Tool:  
  - Behavioral Matlab Simulator
  - Example 1: neocognitron emulation
  - Example 2: texture classification
CORTICAL TISSUE

- Potentially Very High Computational Power: 2Mneurons, 32Gsynapses, 238Tconn/sec
- ¿How to reconfigure?
- ¿What hierarchies and structures?
- ¿What kernels?
- We need theories for implementing desired functionalities (hopefully before the HW is available)
MATLAB based AER Behavioral Simulator

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%First, we declare sources to the system
% SOURCES SOURCES DATA
sources (1) (data1)
%Next, we declare priorities
priorities (0.9,0.8,0.7,0.6,0.5,0.4,0.3,0.2)
%Next, we declare blocks
%NAME IN-CHANNELS OUT-CHANNELS PARAMS STATES
splitter (1) (2,4) (params1) (state1)
hsobel (2) (3) (params2) (state2)
imrotate90 (4) (5) (params3) (state3)
h_sobel (5) (6) (params4) (state4)
imrotate90 (6) (7) (params5) (state5)
merger (3,7) (8) (params6) (state6)
ack (8) () (params7) (state7)

Read Netlist & Conf.

Find channel with 1st PreRqst

Call AER module

Write events on out channels

Find channel with next PreRqst
Multi-Chips Multi-Layer Processing Systems

Neocognitron & Convolution Neural Networks

8 layers, 376 Convolutions

K. Fukushima
1969

Applied to handwritten character recognition
Example: Simplified Neocognitron

- 4 layers, 68 convolution modules
- Inputs 16x16 b&w pixels
- 7 output categories
Large kernels

Layer 1

Layers 2 & 4
15 µs

7.5 µs
Texture Classification

- input 90x90 pixels
- 48 convolutions
- kernel sizes up to 50x50
Detecting People & displaying using jAER

raw input from Tobi’s temporal contral DVS

Vertical Gabor Filter
7x7 kernel

crude template matching
19x36 kernel
Conclusions

• AER has high potential for building complex neurocortical hierarchies.

• A variety of AER sensors are available.

• With present day technology it is feasible to build programmable & reconfigurable “Cortical Tissues” with millions of neurons, billions of synapses, and Tconn/sec.

• We need to develop knowledge for configuring, programming, and training optimally such systems.