Design and Optimization on Dynamic Power System for Self-Powered Integrated Wireless Sensing Nodes

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ABSTRACT

This paper presents an integrated power system for low-power wireless sensor networks with dynamic efficiency optimization technique. By adaptively resizing power transistors and adjusting switching frequency, system efficiency is enhanced significantly. Theoretical analysis is elaborated to support the proposed technique. A prototype integrated power system for self-powered photovoltaic wireless sensing node was designed and simulated with TSMC 0.35μm CMOS process. With a power range of 0.5μW to 10mW, power efficiency stays above 71%. Tolerance between theoretical and simulated optimal power transistor sizes is less than 6.7%, while that of optimal switching frequencies is less than 5%. The paper gives another solution to minimizing system power in the perspective of power processing.

Categories and Subject Descriptors

B.7, B.8

General Terms

Management, performance, design, theory, verification

Keywords

Power efficiency, dynamic power loss control, wireless sensing node, charge pump, DC-DC converter

1. INTRODUCTION

Over the past few years, there has been ever-increasing focus on low-power, wireless sensor networks. It is widely believed that the next revolution in computing technology will be widespread deployment of small wireless computing and communication devices [1, 2], enabling significant improvements on a large variety of applications. The operation of such sensor networks relies on low power wireless sensing nodes, where node-to-node and node-to-station RF communications are strongly demanded. The issue of powering a large number of nodes thus becomes critical. Scavenging energy directly from environment makes the networks autonomous and maintenance free, but the nodes must be designed with ultra-low power dissipation for acceptable lifetime. In addition, in order to be conveniently placed and used, the nodes must be small which also places severe limits on the system designs.

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Currently, advances in integrated circuits (IC) allow us to design systems with low power and small system volume, which fit in well with the demands of wireless sensor networks. However, different from traditional electronic designs, self-powered wireless sensor node must consider reliability of energy sources and a variety of operation modes, introducing new challenges: first, power and voltage generated by self-energy scavenging mechanisms have large variations due to varying intensity and availability of power sources, which cannot be directly used for most low-power IC systems. For instance, the power density of solar energy varies from 6.5 (office lighting) to 15,000 $\mu W/cm^3$ (direct sun). Accordingly, the voltage generated by a photovoltaic cell changes from 0.3 to 2.8V [3]. This severely affects circuit performance and leads to failure of operation in the worst case. Second, traditional power regulation circuits are designed and operated with fixed input and output voltages and switching frequency. High efficiency is thus relatively easy to maintain. Wireless sensing nodes normally need to operate in multi-modes (active, idle, sleeping, etc.) with a large power range [1, 2]. Traditional efficiency optimization methods are then not good enough for high power efficiency. Third, to achieve ultra-low power operation, major circuit modules such as RF transceiver and processors are desired to be power-aware. Hence, low-power operation strategies such as dynamic voltage scaling (DVS) techniques should be embedded with special power system designs [4-7].

In this paper, we propose a new dynamic power loss control scheme and an adaptive power regulation system. The proposed system not only operates as a power interface, but also performs adaptive power management in the whole network. The rest of this paper is organized as follows. Section 2 introduces the system architecture and discusses major circuit modules. In Section 3, we perform theoretical analysis on power losses in major power paths based on the proposed system architecture. Parameters affecting system efficiency will be addresses. Then optimization method on global system efficiency will be introduced. Section 4 depicts the circuit implementation and simulation results in both system and transistor level. We conclude our research efforts in Section 5.

2. SYSTEM ARCHITECTURE

Figure 1 shows the block diagram of the proposed wireless sensing node. The system consists of power scavenging unit, power regulation unit, dynamic power management unit and wireless communication and signal processing unit.

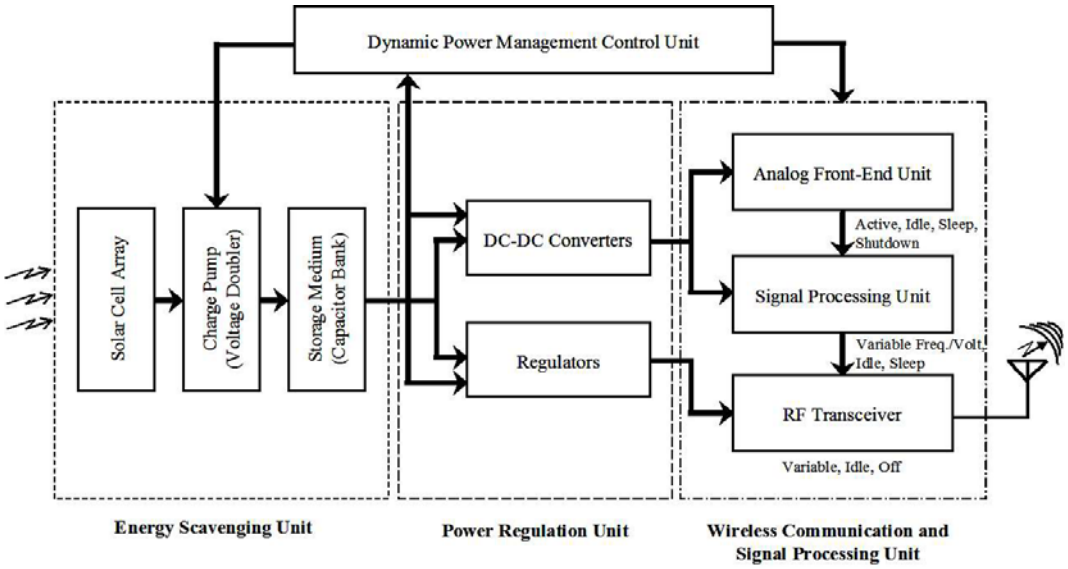

Figure 1 Block diagram of the proposed wireless sensing node

In energy scavenging unit, photovoltaic source is chosen as the major power source. In this design, solar cell array has a DC output of 1.5V. However, it varies by up to 50%, depending on the intensity of energy sources. A charge pump circuit is thus inserted between the solar array and energy storage medium, providing a stabilized supply voltage with a voltage ripple of less than 200mV, such that ICs can be safely self-powered in the later stages. Since the charge pump only needs to perform pre-regulation, design complexity and power dissipation can be largely reduced. Another advantage of using charge pump is that its step-up output voltage allows the capacitor bank to store more energy than step-down cases. The presence of storage medium is critical for system reliability. Energy will be stored when source power is intense and stable, while the stored energy will be released to power the ICs when power source is not reliable.

The power regulation unit converts the output power of charge pump into different voltage levels for different functional modules. For example, analog front-end circuits are very sensitive to noise. A linear regulator is employed as the power interface. Due to multi-mode operations, system power demand varies with time. Dynamic voltage scaling (DVS) techniques should be employed to reduce power dissipations of critical components such as power amplifier in RF transceiver and processor in signal processing units. One best solution to enabling DVS techniques is to design variable- or adaptive-output DC-DC switching power converters [4-7], due to the robustness and high power efficiency. For wireless sensing nodes, non-inverting flyback topology is very attractive, since it can flexibly achieve either step-up or step-down voltage conversion. Thus, the desired output voltage level can always be achieved by adjusting the conversion ratio.

Dynamic power management unit fulfills two major tasks. The first is to incorporate DVS techniques, detect major power activities and enable supply voltage adjustment. The other is to accomplish dynamic power loss control (DPLC) in power stage. This part had been seldom considered, or only individual power converter is done in very simple way. However, power loss in the power system can be the dominant factor in ultra-low power operations, since more than 95% energy flows through it. Traditional power circuits are designed and optimized with fixed input and output voltage levels. High efficiency is thus relatively easy to maintain. Wireless sensing nodes operate in multi-modes with a very large power range. To maintain high efficiency, on-chip power devices in major power paths must be adaptively resizable and controllable based on real-time power demand. In addition, more aggressive power loss control can be done by not only adjusting the sizes of power devices, but also the switching frequency and pumping capacitance. As a result, a global DPLC scheme with multi-variable factors can be derived, which will be addressed in the coming sections.

3. THEORITICAL ANALYSIS

Figure 2 shows the simplified circuit schematic of the power system used to power signal processing unit. We use one typical charge pump and one non-inverting flyback converter in series to demonstrate the method of optimization. However, the method holds for any power converter topologies. The design of the charge pump is inspired by [8] with improved body biasing. Especially, the transistors M5 and M6 are only used to connect the bulk of PMOS to the highest voltage. Hence, the sizes of those are much smaller than other power transistors, and can be negligible in power loss calculation. The power loss in a power transistor mainly consists of conduction loss and switching loss. For charge-pump type power converters, the conduction loss can be represented by

$$P_{Cond,Transistors} = \sum_{i=1}^{n} I_{COUT}{}^{2} R_{iON,PMOS} + \sum_{j=1}^{m} I_{COUT}{}^{2} R_{jON,NMOS} \quad (1)$$

where n and m represent the total number of PMOS and NMOS power transistors, respectively. If the conduction loss due to ESR and pumping capacitance should also be considered, the total conduction loss of charge pump is given by

$$P_{Cond,CP} = I_{COUT}{}^{2} \left(\sum_{i=1}^{n} R_{iON,PMOS} + \sum_{j=1}^{m} R_{jON,NMOS} + ESR + \frac{1}{2 f_S C} \right) \quad (2)$$

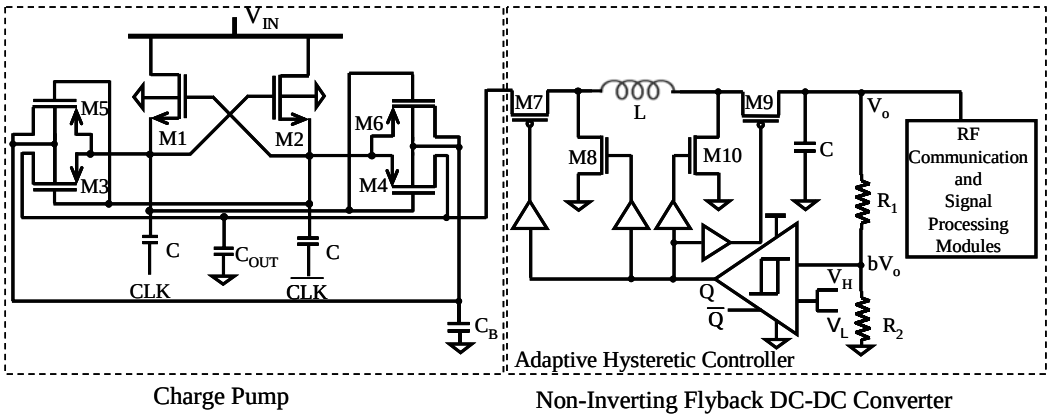

Figure 2. Schematic of a simplified power regulation system

The dynamic power loss for a charge pump stage is given by

$$P_{Dynamic,CP} \approx C_{ox} f_S V_{IN}^2 \left[\sum_{i=1}^{n} (WL)_{i,PMOS} + \sum_{j=1}^{m} (WL)_{j,NMOS} \right] \quad (3)$$

where f_s is the switching frequency. W and L are width and length of the power transistors, respectively. Thus, the total power loss of charge pump is approximately equal to

$$P_{TOTAL,CP} = P_{Cond,CP} + P_{Dynamic,CP}$$

$$= I_{COUT}^2 \left\{ \frac{1}{\mu C_{ox}(V_{IN} - V_T)} \left[\sum_{i=1}^{n} \left(\frac{W}{L} \right)_{i,PMOS} + \sum_{j=1}^{m} \left(\frac{W}{L} \right)_{j,NMOS} \right] + ESR + \frac{1}{2 f_S C} \right\}$$

$$+ C_{ox} f_S V_{IN}^2 \left[\sum_{i=1}^{n} (WL)_{i,PMOS} + \sum_{j=1}^{m} (WL)_{j,NMOS} \right] \quad (4)$$

For switch mode power converter (SMPC), the result is slightly complicated,

$$P_{Cond,SMPC} = I_{OUT}^2 \{ D^2 [\sum_{i=1}^{a} R_{ONi,NMOS} + \sum_{j=1}^{b} R_{ONj,PMOS}] + (1-D)^2 \cdot \quad (5)$$

$$[\sum_{k=1}^{c} R_{ONk,NMOS} + \sum_{l=1}^{d} R_{ONl,PMOS}] + [xD + y(1-D)]^2 ESR_L + ESR_C \}$$

where D is the duty ratio, ESR_L and ESR_C are the equivalent series resistance of the inductor and the output capacitor, respectively. For buck converter, x=1 and y=1; for boost converter, x=1 and y=0; for flyback and non-inverting flyback converters, x=0 and y=1. The switching power loss of a SMPC converter will be

$$P_{Dynamic,SMPC} = C_{OX} f_{SW} V_{COUT}^2 [\sum_{i=1}^{a} (WL)_{i,NMOS} + \sum_{j=1}^{b} (WL)_{j,PMOS} \quad (6)$$

$$+ \sum_{k=1}^{c} (WL)_{k,NMOS} + \sum_{l=1}^{d} (WL)_{l,PMOS}]$$

Specifically, for the power system illustrated in Fig. 2, the power loss due to charge pump will be

$$P_{TOTAL,CP} = I_{COUT}^2 [2L/(\mu C_{OX} W (V_{IN} - V_T)) + ESR_C + 1/(2 f_S C)] \quad (7)$$

$$+ 8WLC_{ox} f_s V_{IN}^2$$

Power loss due to non-inverting flyabck SMPC will be

$$P_{TOTAL,SMPC} = I_{OUT}^2 \{ 2D^2 L_D / (\mu C_{OX} W_D (V_{COUT} - V_T)) +$$

$$2(1-D)^2 L_{(1-D)} / (\mu C_{OX} W_{(1-D)} (V_{COUT} - V_T)) + (1-D)^2 ESR_L + ESR_C \} \quad (8)$$

$$+ C_{OX} f_{SW} V_{COUT}^2 [4(WL)_D + 4(WL)_{(1-D)}]$$

Based on Eqns. 7 and 8, the optimized width of the transistor can be derived by minimizing power loss in the equations. Accordingly,

$$W_{OPT,CP} = I_{COUT} / (2 C_{OX} V_{IN} \sqrt{(V_{IN} - V_T) f_S \mu}) \quad (9)$$

Similarly the optimized switching frequency will be

$$f_{S,OPT,CP} = I_{COUT} / (4 V_{IN} \sqrt{C C_{OX} WL}) \quad (10)$$

For non-inverting flyback converter, the optimized transistor width will be

$$W_{D,OPT} = D I_{OUT} / (C_{OX} V_{COUT} \sqrt{2 \mu f_S (V_{COUT} - V_T)}) \quad (11)$$

and

$$W_{(1-D),OPT} = (1-D) I_{OUT} / (C_{OX} V_{COUT} \sqrt{2 \mu f_S (V_{COUT} - V_T)}) \quad (12)$$

Because the SMPC converter is designed with pulse-frequency modulation (variable switching frequency), optimization method on its switching frequency does not apply here.

4. CIRCUIT IMPLEMENTATION & SIMULATION

The power system in Fig. 2 has been successfully designed and simulated with TSMC 0.35μm CMOS process. Figs. 3 and 4 show HSPICE simulation results in steady state and DVS transient, respectively. From top to bottom in Fig. 3 show the output voltages of non-inverting flyback switching converter and charge pump and the inductor current of the switching converter. The results demonstrate well-regulated operation and stable power flows in the power stages. Fig. 4 illustrates the waveforms in DVS transients. The prompt load transient performance can be clearly observed from the output voltage and inductor current in the 1st and 3rd panels. Very constant output voltage of charge pump in the second panel demonstrates excellent load regulation.

Efficiency optimization based on transistor resizing and switching frequency adjustment was also conducted. The power efficiency versus transistor sizing in SMPC converter is plotted in the Fig. 5. The optimized transistor width at peak power efficiency is 3075μm in simulation, which is very close to the theoretical result of 2870 μm, when the equivalent load is 50Ω. For charge pump, the optimized value is around 5000 μm. The system efficiency with respect to the charge pump switching frequency is plotted in Fig. 6. The results show that the

optimized frequency is around 20.0 MHz which is very close to the theoretical result of 21.0 MHz. Fig. 7 shows the two dimensional efficiency optimization curve of the power system when both transistor size and switching frequency are variable, which gives clear instruction on how to perform adaptive adjustment to achieve highest possible power efficiency on-chip. With the proposed optimization technique, the overall power efficiency can be kept above 70%.

5. CONCLUSION

An efficiency optimization method using dynamic power loss control is proposed and analyzed. By adaptively resizing the power transistors and adjusting switching frequency, system efficiency is greatly enhanced. Theoretical analysis of optimization on transistor size and clock frequency is explicitly elaborated by considering all possible power losses. Simulation results successfully verify the proposed theory on power efficiency optimization.

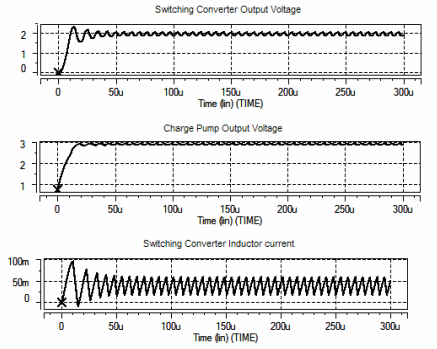

Figure 3. simulated waveforms in steady state

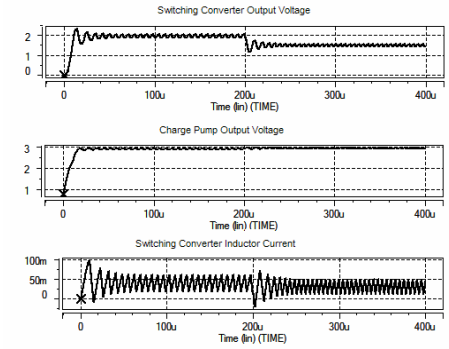

Figure 4. simulated waveforms during DVS transient

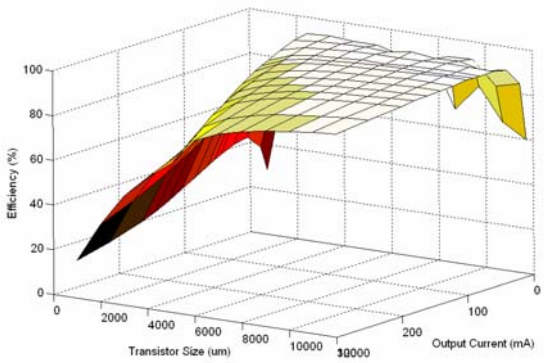

Figure 5. Efficiency vs transistor size of SMPC converter

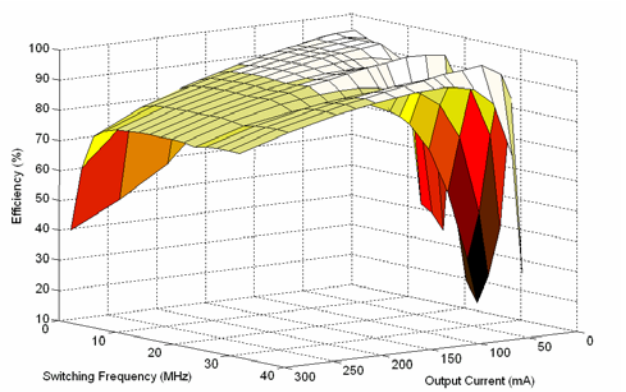

Figure 6. Efficiency versus switching frequency of charge pump

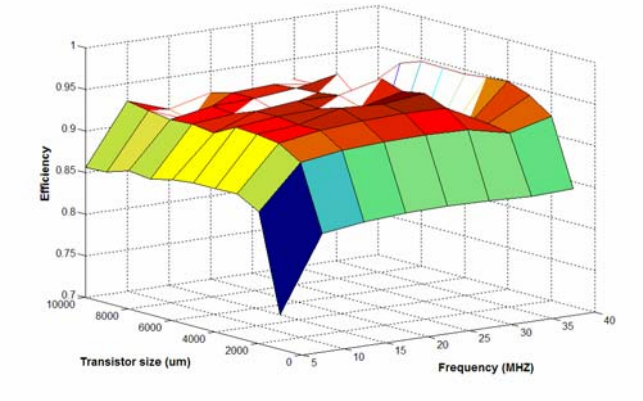

Figure 7. Two dimensional optimization of power system

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