# High Resolution Body Bias Techniques for Reducing the Impacts of Leakage Current and Parasitic Bipolar

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## ABSTRACT
With scaling process generation, power management techniques are more significant. Body bias techniques are useful for the solutions. We propose a high resolution body bias generation circuit which supplies optimal body bias in both the active and standby mode. By using this circuit, the adjustment accuracy of threshold voltage (Vt) in the active mode was improved about 4.1 times of the conventional circuits at 0.6V forward body bias condition. In addition, for standby mode, when 128 kByte SRAM was supplied back body bias by this generator, the off-state leakage current was reduced to 50% of a fixed back body bias.

## Categories and Subject Descriptors
B.7.1 [**Integrated Circuits**]: Types and Design Styles – advanced technologies, algorithms implemented in hardware, VLSI (verylarge scale integration).

## General Terms
Design, Theory.

## Keywords
CMOS scaling, leakage current, leakage components, band-to band tunneling, process variation, process compensation, substrate bias, body bias generator, dead lock.

## 1. INTRODUCTION
The variation of transistor characteristics is increasing in recent edge CMOS processes. In addition, for processors, the more performance is required. Therefore, with scaling process generation, the power consumption in the active mode increases to improve the performance. Moreover, the sub threshold leakage current in the standby mode also increases.

To solve these problems, the some methods are proposed, which compensates the variation of MOS characteristic by controlling body bias. Forward body bias techniques have advantage of reducing power consumption in the active mode[1]. In contrast, back body bias is useful for standby mode[2]. However, the body bias voltage range is limited. When a large forward body bias voltage is supplied, the drain current leakage and the substrate current increase by parasitic bipolar in CMOS devices structure. On the other hand, when a large back body bias voltage is supplied, the current factor of gate induced drain leakage (GIDL) and band to band tunneling (BTBT) increases by the leakage scaling effect [4]. Moreover, the back body bias voltage is also decided by the reliability, which the degradation of MOS is accelerated by the effect of both the hot career and negative bias temperature instability (NBTI).

Therefore, for the body bias generator circuits, supplying the optimal body bias voltages within the limited body bias voltage range are required. In the past, to accept the requirements, the body bias generators are proposed[1-7]. The body bias generators are classified into two categories. One technology is the sub threshold leakage reduction method by monitoring the drain current of MOS [2-4]. The other technology is the method which keeps the delay of critical paths constant [5-6]. However, in the active mode, the stability of forward body bias generator for producing minimum delay of logic circuits is not defined[2-6]. Moreover, when the body bias generator moves from the active mode to the standby mode, the stability of back body bias generator is not discussed[2-6].

In section 2, the design challenges for body bias generators in the active and standby mode are discussed, and we propose the high resolution body control method which controls both the variation of MOS devices in the active mode and the leakage current in the standby mode. In section 3, the implementation of our body bias generator is explained. In section 4, the measurement results of our body bias generator are shown. Finally, in section 5, we summarize our finding.

## 2. HIGH RESOLUTION BODY BIAS GENERATOR

### 2.1 Body Bias Generator for Active Mode
In the body bias control system which compares the delay of the critical path to the operational clock, the upper value of forward

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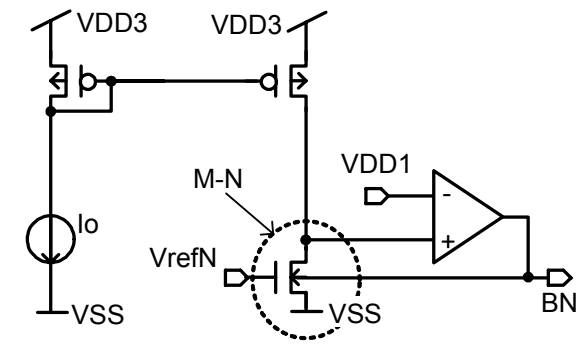
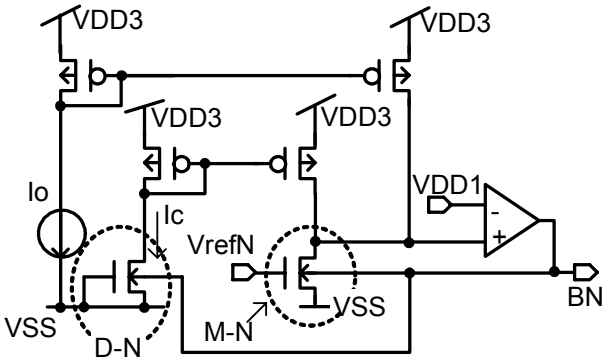



**(a) Conventional Circuits.**




**(b) Proposed Circuits.**

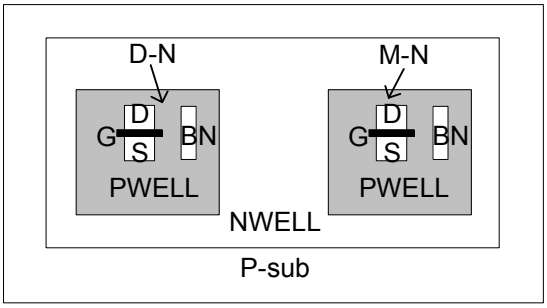
**Figure 1. NMOS type Fixed Vt Body Bias Generator.**

body bias is limited. It is because that the marginal value over a large forward body bias voltage induces a saturation phenomenon of circuit delay by the parasitic bipolar effect[8]. Once a body bias value above the saturation phenomenon is supplied, the system falls into incorrect state (the so-called "dead lock state"). A dead lock is the phenomenon which feedback control is emitted infinitely.

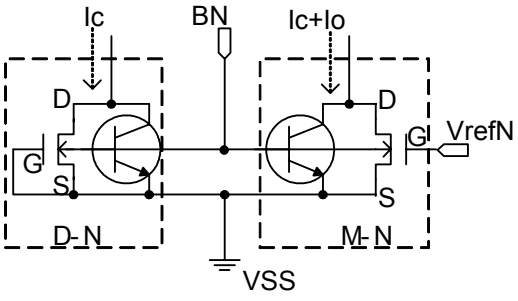
In contrast, the dead lock state does not happen with the body bias control method which monitors the drain current of MOS devices [4]. However, if a large forward bias is supplied, the source current of MOS devices branches off two main paths. One is the emitter current of parasitic bipolar by body bias, and the other is the normal the source-drain current of MOS. The parasitic bipolar current interrupts rectifying the Vt value of MOS correctly. Thus, the problem sacrifices the performance of circuits that are supplied with the body bias. For example, considering CMOS logic circuits, the optimal Vt value of each MOS devices is defined so that the minimum power consumption is achieved. However, when forward bias is applied to the CMOS logic circuits, the Vt value of the CMOS logic circuits become higher than the defined Vt because of parasitic bipolar. It causes that the delay is slower.

We proposed new monitor circuits to solve the above mentioned problem. Figure 1 shows the schematic of NMOS type Fixed Vt body bias generator including both the conventional circuits (a) and our proposed circuits (b). This body bias generator keeps Vt (VrefN) of NMOS fixed regardless of the variation of both temperature and process. It is controlled by body bias for NMOS (BN) so that the drain voltage of M-N becomes the same value as power supply voltage (VDD1) used in the CMOS logic circuits. The voltage value of VDD3 is larger than that of VDD1. In the conventional circuits, the current source (Io) of the NMOS monitor circuits (M-N) is used only the dc current generation circuit based on the reference voltage from BGR. In the proposed circuits, the current source is added another current mirror type of sourcing the drain current of the dummy NMOS monitor circuits (D-N) whose gate is connected to VSS. If forward bias is supplied the substrate of NMOS on both M-N and D-N, parasitic bipolar current (Ic) will flow. The quantity of the parasitic bipolar current of D-N is added to the current source of M-N. The parasitic bipolar current factor which flows in M-N is cancelable with this added amount of current. Therefore, the current sources become possible to provide the accurate source-drain current value which sets up the defined Vt value of M-N.

Figure 2 shows the layout structure (a) and the equivalent circuits (b) in the proposed monitor circuits. As shown in Figure 2 (a), the layout structure of D-N is the same as M-N. In addition, the each PWELL on both D-N and M-N is surrounded by NWELL. The area and the distance of base, collector and emitter of parasitic lateral bipolar in D-N are also the same as parasitism lateral bipolar of M-N. Therefore, the each parasitic lateral bipolar is served similarly as shown in Figure 2 (b).




**(a) The layout structure.**




**(b) The equivalent circuits.**

**Figure 2. Proposed NMOS Monitor Circuits.**

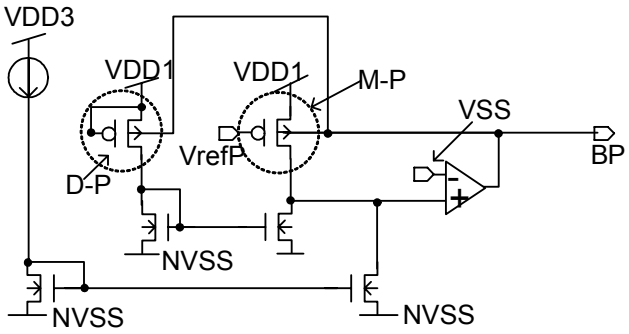
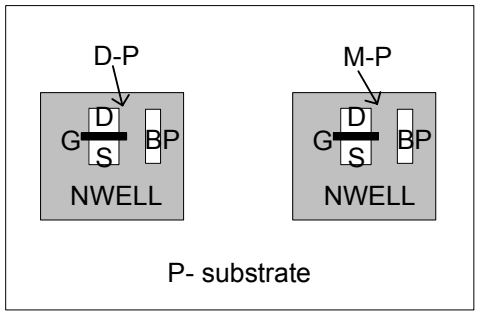
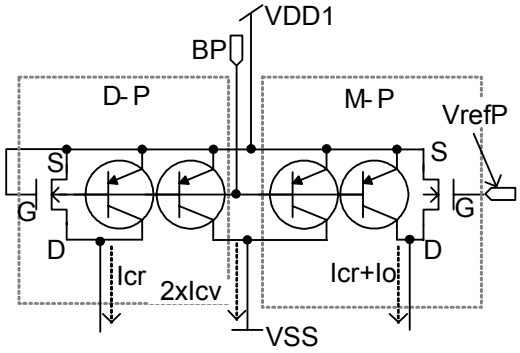



**Figure 3. PMOS type Fixed Vt Body Bias Generator.**




**(a) The layout structure.**




**(b) The equivalent circuits.**
**Figure 4. Proposed PMOS Monitor Circuits.**

Figure 3 shows the schematic of PMOS type Fixed Vt body bias generator. This body bias generator keeps Vt (VrefP) of PMOS fixed regardless of the variation of both temperature and process. It is controlled by BP so that the drain voltage of M-P becomes the same value as ground level voltage (VSS) used in the CMOS logic circuits. The voltage value of NVSS is smaller than that of VSS. In the proposed circuits, the current source is added another current mirror type of sourcing the cut off current of the dummy PMOS monitor circuits (D-P). If forward bias is supplied the body of PMOS on both D-P and M-P, parasitic bipolar current will flow. The quantity of the parasitic bipolar current on D-P is added to the current source of M-P. The parasitic bipolar current factor which flows in M-P is cancelable with this added amount of current. Therefore, it becomes possible to secure from the the same current value of the current source as the source-drain current value which set to the defined Vt value of M-P.

Figure 4 shows the layout structure (a) and the equivalent circuits (b) in the proposed monitor circuits. As shown in Figure 4 (a), the layout structure of D-P is the same as M-P. In addition, the each NWELL of both D-P and M-P is surrounded by P-substrate. The area and the distance of base, collector and emitter of parasitic bipolar in D-P are also the same as two type parasitic bipolar devices of M-P. One is lateral bipolar whose current value is Icr. The other is vertical bipolar whose current value is Icv. Therefore, the each parasitic bipolar is served similarly as shown in Figure 4 (b).

## 2.2 Body Bias Generator for Back Body Bias

Generally, the analog type body bias generators (Figure 1-2) are used to reduce the off current of logic circuits in the standby mode. However, when the body bias generator moves from the active mode to the standby mode, it is difficult to prevent the increase of the leakage current by the leakage scaling effect in the feedback control system of analog type body bias generator [2-4]. It is because a dead lock is caused when a body bias value shifts to a back bias side further rather than the minimum point of leakage current[4].

Figure 5 shows the design challenges of the analog type body bias generators. As shown in Figure 5, in case that the Vt value of MOS on the monitor is higher than the target Vt value at both the process and temperature condition, it is no problem to move from the active mode to the standby mode ("state 1" as shown in Figure 5). However, in case that the Vt value of MOS on the monitor is lower than the target Vt value, when it moves from the active mode to the standby mode (state 2), the deadlock state is caused. Because the polarity of the operational amplifier used in analog type body bias generator is only one side. In order to improve the problem, a fixed body bias voltage value, which realizes the minimum leakage current at a conditions, is sometimes given to the body bias outputted from the body bias generator. However, even if system on chip (SOC) which has a huge number of transistors reduces the leakage current factor with the conventional back bias control method, the issue will still remain.

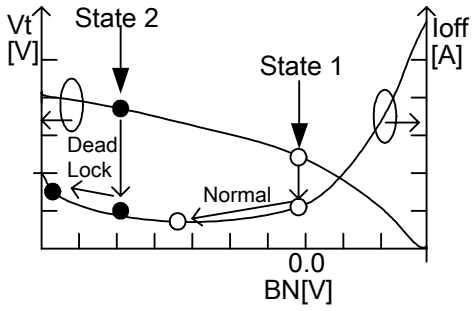



**Figure 5. The design challenges of analog type body bias generator. The each point is each state from the active mode to the standby mode.**

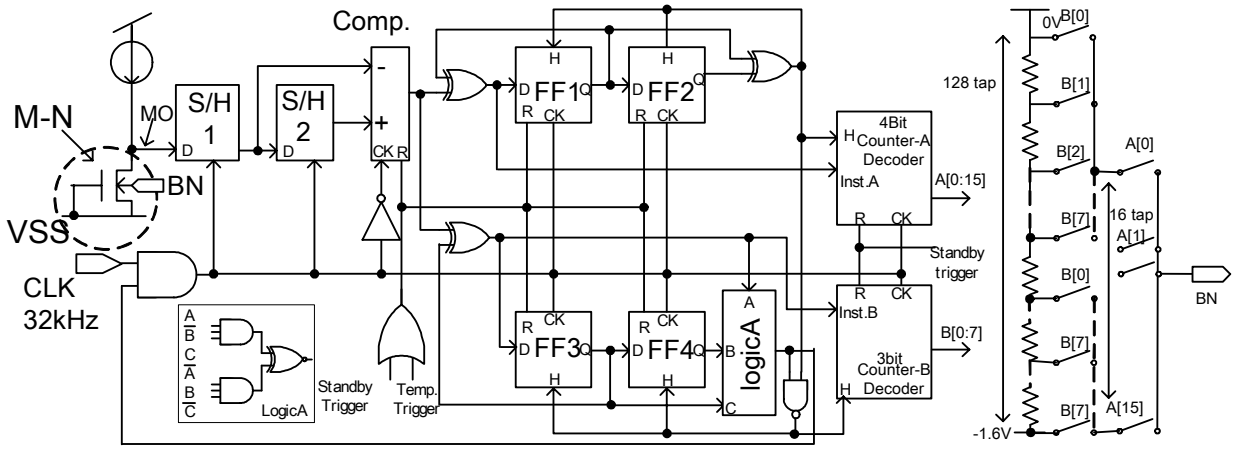



**Figure 6. The block diagram of the low power body bias generation circuits.**

Another method is also proposed[7].The power consumption is large because of many operational amplifiers.

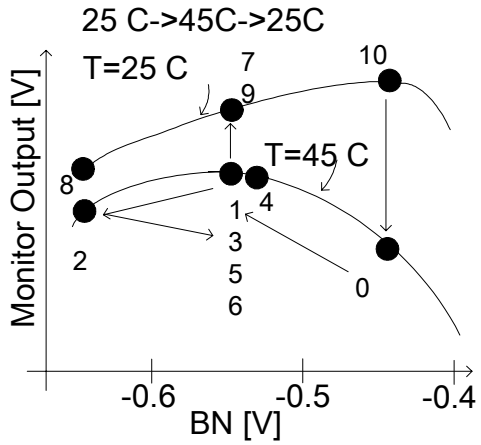



**Figure 7. The relationship between MO and BN.**

**Table 1. The data of both F.F 1,2,3,4 and counter A/B at each state.**

| State | Comp. | FF1FF2 | FF3FF4 | Inst. A | Count A | Inst. B | Count B |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 0 | 0 0 | 0 | 0100 | 0 | 100 |
| 1 | 0 | 0 0 | 0 0 | 0 | 0101 | 0 | 100 |
| 2 | 1 | 0 0 | 0 0 | 1 | 0110 | 0 | 100 |
| 3 | 0 | 1 0 | 0 0 | 1 | 0101 | 1 | 100 |
| 4 | 1 | 1 0 | 1 0 | 0 | 0101 | 0 | 011 |
| 5 | 1 | 1 0 | 0 1 | 0 | 0101 | 1 | 100 |
| 6 | 1 | 1 0 | 0 0 | 0 | 0101 | 1 | 100 |

We propose the low power body bias generation circuits to set the minimum point of the leakage current in CMOS logic circuit. The concept of the body bias generator is the following two points. One is that the body bias generator includes the detector circuit to detect the polarization of differentiation coefficient (di/dt) between the immediate value and previous value of the drain leakage current in the monitor circuit. Thus, even if BTBT current value is main factor of the drain leakage current at the initial state (state 2 as shown in Figure 5), the dead lock is improved by using the polarization of the differentiation coefficient. The other is that the body bias generator can stop the operation of the detector.

Figure 6 shows the proposed the block diagram of the low power body bias generation circuits. The output value (MO) which is carried out the voltage conversion of the drain leakage current value of the NMOS monitor circuits (M-N) is inputted into the sampling and holding circuit (S/H 1). The operating clock frequency of S/H is 32kHz. The mode controller block in both SOCs and processors usually operate at a slower frequency to supervise that an interruption signal is activated during the standby mode. Therefore, it is easy to use low frequency clock. The S/H 2 is latched the output value of the S/H 1. the voltage comparator (Comp.) compares the immediate value and previous value. The output of the comparator is branched. One output is inputted into a Flip-Flop (FF) with load/hold function, and the other output is inputted into two counter circuits with both increment and decrement functions (4bit Counter A, 3bit Counter B). The FF and the counter circuits consist of flip-flop circuits with the function which keeps the value by the holding signal (H). The signals (A[0:15],B[0:7]) outputted from both the 4bit Counter A and 3bit Counter B decoded are changed the branch of the serial resistor at 100mV step or at 12.5mV step and output BN. The voltage range of BN is from -1.6V to 0V.

Figure 7 shows the relationship between MO and BN. As shown in Figure 7, the changing points (0, 1, 2, 3, 4, 5, 6) at each clock cycle is also shown in the maximum voltage point of the MO. Table 1 shows the value of each F.F and each Counter in each clock cycle in which BN changes at the minimum point of leakage current as shown in Figure 7. Once repetition of increase and decrease of BN occur in the neighborhood of minimum leakage current point (State:1->2), the 4bit Counter A stops. At the same time, the 3bit Counter B starts. And then the accuracy of the adjustment value of BN increases 8 times. Furthermore, when a repetition of increase and decrease occurs again, the 3bit Counter B stops and the output value of BN is fixed near the minimum point of the leakage current(State:3-6). Temperature sensor is placed in another block. When the temperature shifts every 20 ℃, the operation of the low power body bias generator is started again. That is, the body bias generator can prevent dead lock and also operate from the normal initial state. In addition, the body

bias generator can reduce the power consumption by gating the detector circuits.

## 3. IMPLEMENTATION

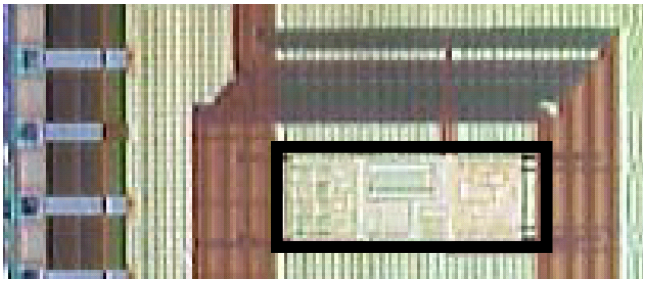


**Figure 8. Chip micrograph**

Figure 8 shows the chip micrograph of the proposed high resolution body bias generation circuit (HRBBG) that can manage both the active mode and the standby mode. The fabricated process is a 130nm CMOS process with six layer of metal and has triple well structure. The HRBBG also includes the BGR. The transistors are used both thin and thick gate oxide. The area size of HRBBG is 0.5mm x 0.2mm.

## 4. MEASUREMENT RESULTS

### 4.1 Body Bias Generator for Forward Body Bias

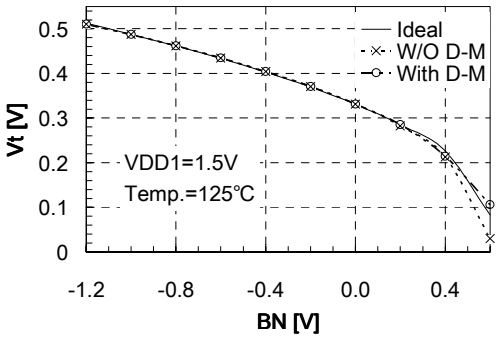



**Figure 9. Measured body bias dependence of NMOS Vt.**

Figure 9 shows the results which measured the body bias dependence of NMOS Vt when D-N is used or not. Figure 10 shows the results which measured the body bias dependence of PMOS Vt when D-P is used or not. The measurement conditions are at VDD1=1.5V, VDD3=3.0V, and T= 125°C to which the bipolar effect tends to happen. As shown in Figure 9, in the range of more than BN=0.4V, the measured result with D-N is pretty closer than the measured result without D-N to the ideal theoretical solid line of Vt. The adjustment accuracy of Vt was improved about 4.1 times of the conventional circuits at BN=0.6V. As shown in Figure 10, at BP=0.9V, the Vtp with D-P is -0.03V. In contrast, the Vtp without D-P is mostly 0V. It is found that the effect of the parasitic bipolar on PMOS devices is smaller than that of NMOS. That is, it turns out that the accurate body bias voltage value for rectifying to the defined Vt is outputted from the proposed circuits. In addition, the circuits are helpful of being stable loop characteristic of the analog feedback.

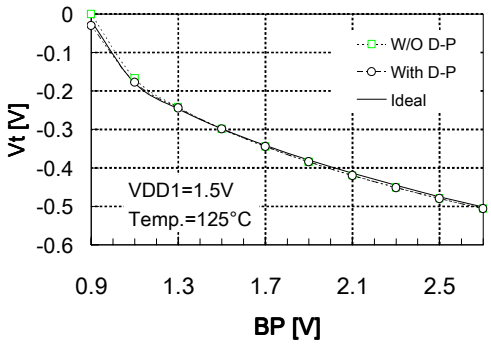



**Figure 10. Measured body bias dependence of PMOS Vt.**

When the proposed body bias is applied to 2-NAND 21-stages chain, the delay was about 10% faster than that of conventional at defined Vt=0.1V Temp.=125°C. Thus, in case of keeping delay of the chain fixed, it is possible to reduce the power consumption by scaling power supply voltage.

### 4.2 Body Bias Generator for Back Body Bias

The measured average current of the low power body bias generator was about 5.4uA (unstable state ;1-5) and 1.5uA (stable; 6) at 27°C and VDD1=1.0V. That is, it is effective when the leakage current of the whole semiconductor integrated circuit is larger than the conventional minimum value.

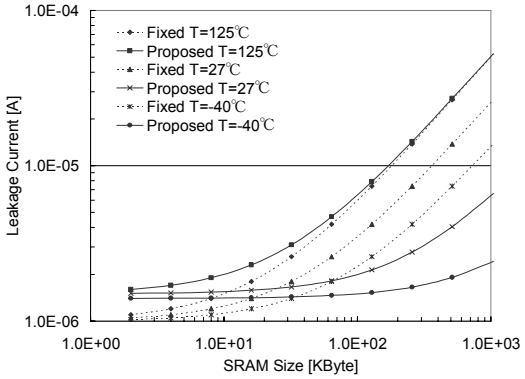



**Figure 11. The measured leakage current versus SRAM size.**

Figure 11 shows the measured leakage current versus the memory size of embedded SRAM at each temperature (T=-40, 27, 125°C VDD1=1.0V) using the low leakage body bias or the conventional fixed back body bias (BN=-1.6V). As shown in Figure 11, when

the low power body bias generator is applied to 22KB SRAM, the operating current overhead of the body bias generator is canceled at T=27°C. In 128KB SRAM, it is found that the leakage current is improved by about 50% compared with from the conventional fixed body bias at T=27°C. Thus, with scaling the CMOS process, the effect of the body bias generator is more significant because of increasing both the variation of MOS devices and the leakage current of BTBT.

## 5. CONCLUSION

The high resolution body bias generator is proposed for managing the power reduction in both active and standby mode. It is fabricated in 130nm CMOS process. By using the body bias generator, the adjustment accuracy of Vt was improved about 4.1 times of the conventional circuits at BN=0.6V. It is possible to reduce the power consumption in the logic circuits by using the body bias generator. In addition, when the low power body bias generator was applied to 128KB SRAM, the leakage current reduced by 50% compared with the conventional fixed back body bias. Thus, the proposed body bias generator is efficient to reduce the power consumption of SOCs in both the active and standby mode.

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