Low Power SRAM Techniques for Handheld Products

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ABSTRACT
SRAM leakage constitutes a significant portion of the standby power budget of modern SoC products for handheld applications such as PDA and cellular phones. NMOS and PMOS reverse bias techniques for leakage reduction are implemented in a 2MByte SRAM testchip built with low power 90nm technology. Sophisticated analog regulators were implemented to precisely control the PMOS and NMOS reverse bias levels. The application of the reverse bias led to a 16X reduction in total array standby leakage and a cell leakage of only 20pA/bit. Excellent data retention for these bias conditions was demonstrated with detailed Vccmin mesurements.

Categories and Subject Descriptors
1.1 Technologies and digital circuits: low power memory circuits

General Terms
Theory and measurement

Keywords
Memory, leakage, back-bias, bitcell

1. INTRODUCTION
Handheld products such as PDA and cellular phones must very aggressively conserve both active and standby power. The energy budget is typically one Lithium Ion battery of 3000mWH (1000mAH). Peak active power must be held under 1W both to conserve power and to keep the thermals manageable. In standby mode it is desirable to save the battery so that it will be available for active mode applications. Techniques such as reverse body biasing to reduce standby leakage power has been reported in the literature [1-4].

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For the 90 nm generation of products, the transistor leakage is higher and thus most circuits must be powered down during standby. The standby power of the system must not consume more than 0.5 to 1.0mW. This power is traditionally divided among the three most power hungry elements in a handheld device: The RF amplifier, the LCD display, and the silicon. Most of the cell phone products in the 90nm node have a budget of ~250uA in standby mode [4]. When the silicon is in standby mode, the highest contributor to the power is from the SRAM arrays in drowsy or the back-bias mode. The memory cell leakage consists of signification contributions from Ioff, Igate, and Ijunc. Ideally, it is desirable to beat the power spec for the array by using reverse bias (drowsy mode) as aggressively as possible to reduce the bitcell leakage even further. This would allow us to have better product power numbers or to keep state in more SRAM arrays. To reduce the leakage even further, we would lower the Vcc and raise the Vss until the bitcell is on the cusp of becoming unstable. This paper uses the 90nm certification SRAM vehicle to characterize and measure SRAM array and bitcell leakage under varying back bias conditions. Data retention under drowsy bias was characterized by extracting Vccmin of the 2MByte array at sort.

2. DROWSY BACK-BIAS SCHEME
The SRAM testchip is a 2MB (256K x 64 bit) SRAM, composed of 16 instances of the 128KB SRAM Module. Each SRAM module is 16K x 64 and contains all needed Drowsy support logic, consisting of drowsy regulators and various power switches. Maximum frequency exceeds 400 MHz at 1.25V. Typical active power is less than 480 mW at 1.4V, 500 MHz.

The block diagram of the 2MByte SRAM is shown in Figure 1. For standby power reduction, the SRAM module design supports back-bias drowsy mode for the memory cells and a non-state retentive power-down mode for non-array logic. A basic power management unit (PMU) controls the power state of each SRAM module. Any one or more SRAM module can be placed in one of three states (Idle, Drowsy, shut-off) from the pads or through JTAG commands. The PMU is designed to allow maximum user

flexibility in drowsy transitioning, even when non-transitioning modules are under test.

Drowsy is a design technique that uses device back-bias to reduce sub-threshold current. The technique is implemented for the 2MByte SRAM for both NMOS and PMOS. In order to reverse bias the NMOS, the Vss of the array is raised to Nch sources while keeping substrate at 0V. The PMOS is reverse biased by raising the Pch N-well bias above Vcc_mem. The bias levels are maintained by voltage regulators. It is necessary to retain the states in the in memory elements during the back bias or the Drowsy

mode. The Drowsy mode is static – no read or write operations are allowed. Specific control sequence is required to move the array in and out of Drowsy. The SRAM test chip supports traditional back-bias drowsy mode only for the SRAM modules. All logic outside the SRAM modules does not support any form of drowsy modes. The SRAM modules have a separate power supply domain (Vcc_mem) from the rest of the chip to allow for SRAM drowsy current measurements.

The SRAM was fabricated using the 90nm low power process technology. The process is tailored to guarantee ultra low leakage. The oxide thickness target was selected for optimized gate leakage, and the tip/halo junctions were optimized for low junction leakage. The Vt was selected for high performance with low leakage and the devices were optimized with minimal Vt and low Cgate to achieve high performance at low voltage down to 0.8V.

The SRAM uses the standard low power 90nm bitcell arrays. The cell employs wide bit topology for better cell device mismatch properties [5-6]. The layout of the bitcell is shown in Figure 2.

2.1 The Bitcell Leakage Components

The SRAM modules have an aggressive drowsy leakage budget of 25pA/cell at 1.3V, 30C. The estimated breakdown of the bitcell leakage under drowsy bias is shown in Figure 3. The various leakage paths of the bitcell are also shown in Figure 3. In order to meet the leakage spec, it is necessary to understand how the various cell leakage components respond to the drowsy back bias. Table 1 shows the bias condition of the individual bitcell devices during drowsy.

3. RESULTS

Extensive device level back bias characterization was done at etest to understand the impact of drowsy on the large SRAM arrays. The subthreshold and the gate leakage responded well to the reverse bias. Process implant conditions were optimized to meet the junction leakage requirements. Idle, drowsy and shut-off current of the array were measured at sort and state retention under drowsy bias was characterized. Vccmin values of the SRAM array were also extracted at sort

3.1 Device Level Characterization of Back Bias

The nmos and pmos gate and sub threshold leakage reduction was accomplished with reverse bias. High gate and channel leakage reduction factor were achieved for both NMOS and PMOS. In order to explore the scalability of the drowsy scheme, the leakage reduction with drowsy back bias was measured as a function of channel length. As channel length is reduced, the subthreshold component of the leakage budget is increased, increasing the effectiveness of the back bias. Even for a drawn channel length down to 75nm, no degradation of the leakage reduction factor was observed. This data shows the scalability of the back bias leakage reduction technique to the 65nm generation of battery powered SRAM circuits.

3.2 Impact of Back Bias on the SRAM

The sort data for the SRAM exhibited two distinct standby current modes: idle and drowsy, as shown in Figure 4. With minimum amount of reverse bias, ~16X reduction of leakage was achieved that led a cell leakage of 20 pA.

Since a key product requirement was to retain state under drowsy bias, detailed retention tests were performed as a function of NMOS and PMOS reverse bias. In the drowsy scheme, the reverse bias is applied to the bitcell NMOS devices by raising the potential of the source or the Vss_mem. Application of the drowsy bias thus cuts down the effective voltage across the bitcell and make it more prone to disturbance. The data retention during the drowsy bias is characterized by extracting the minimum Vcc at sort under various amount of PMOS and NMOS reverse bias. Excellent distribution of Vccmin was obtained under reasonable bias conditions, as shown in Figure 5.

4. CONCLUSIONS

Reverse bias techniques were applied to the 90nm test chip SRAM array to meet the aggressive standby power target of the Intel's handheld products. Detailed device level characterization was performed to understand the impact of back bias on various leakage components. The reverse bias drastically cut down the subthreshold and the gate leakage components. Special process adjustment such as modification of the tip/halo implants were required to rein in the junction leakage component. The scalability of the drowsy back bias technique were established through measurement of leakage reduction as a function of channel

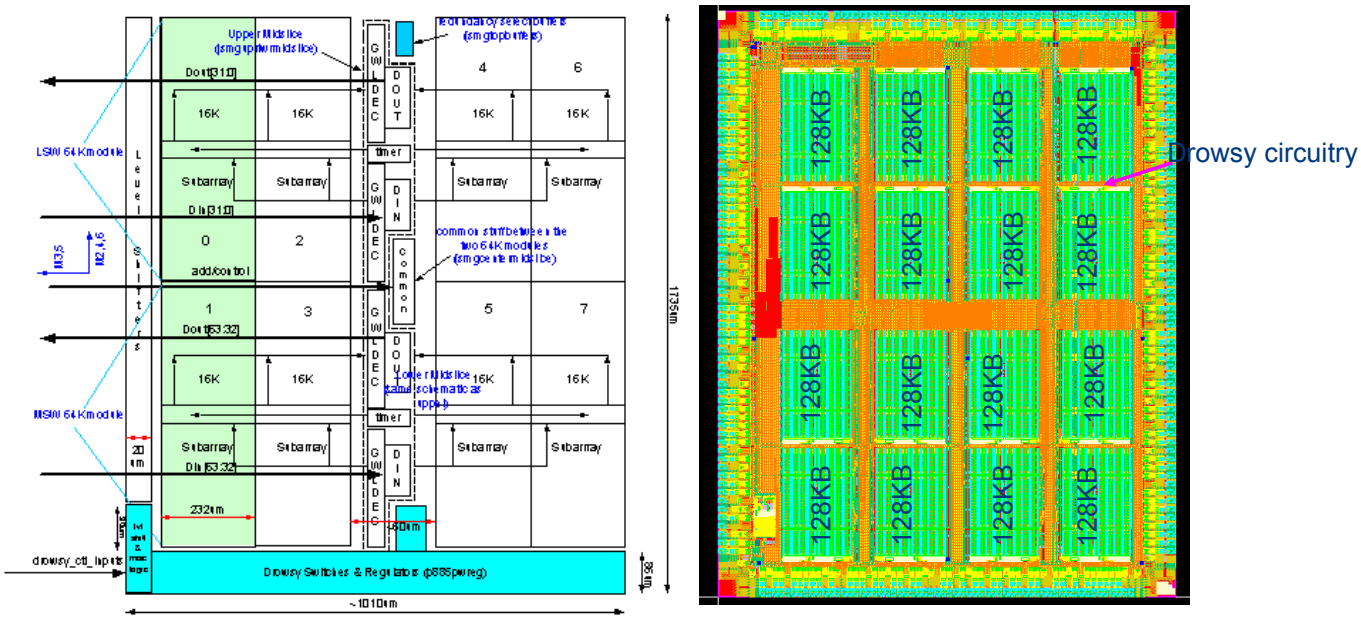

Figure 1: Block diagram and layout of the of the 2MByte SRAM testchip.

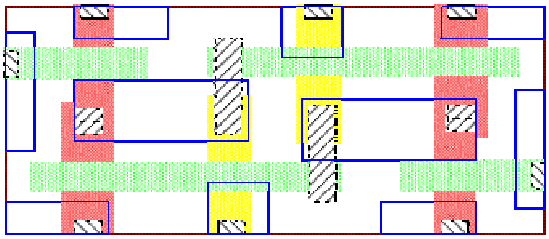

Figure 2: Layout of the wide bit cell.

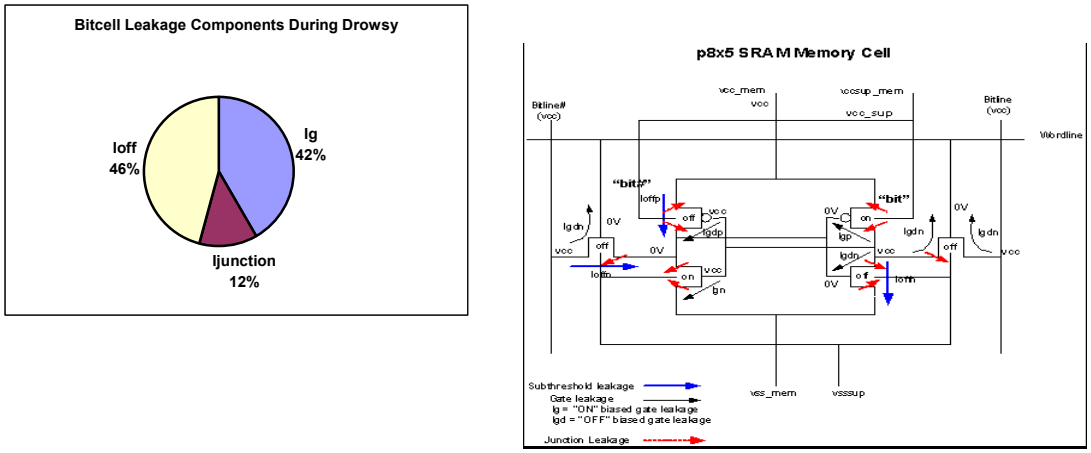

Figure 3: Cell leakage components and leakage paths during drowsy back-bias.

Table 1: Cell transistor biases during drowsy

Device	Vg	Vd	Vs	Vb
pass-gate - off - 0	vnreg	vcc	vnreg	0
pass-gate - off - 1	vnreg	vcc	vcc	0
PD - on - 0	vcc	vnreg	vnreg	0
PD - off - 1	vnreg	vcc	vnreg	0
PU - on - 1	vnreg	vcc	vcc	vpreg
PU - off - 0	vcc	vnreg	vcc	vpreg

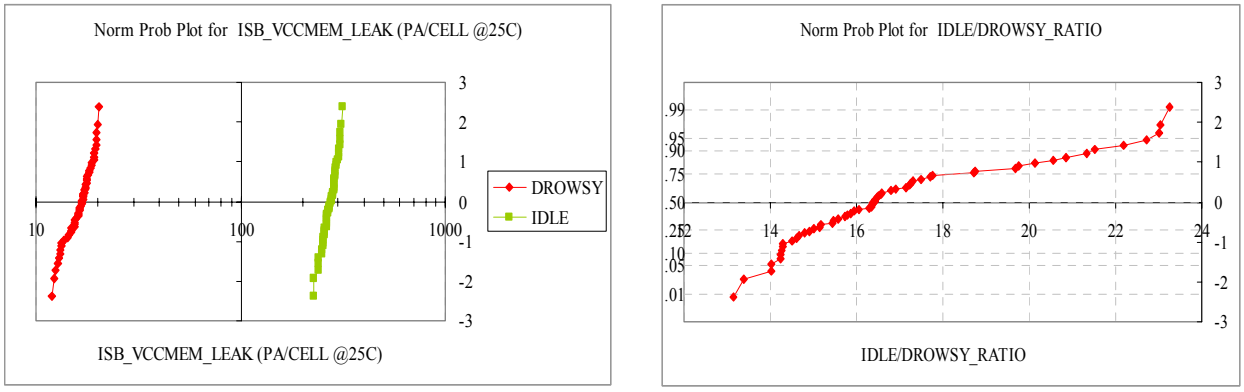

Figure 4: Measured cell leakage during idle and drowsy back bias. The optimized PMOS and NMOS back bias for good retention led to a cell current of only 20pA at 1.3V, 25C. The Measured median Idle/Drowsy leakage ratio is 16.

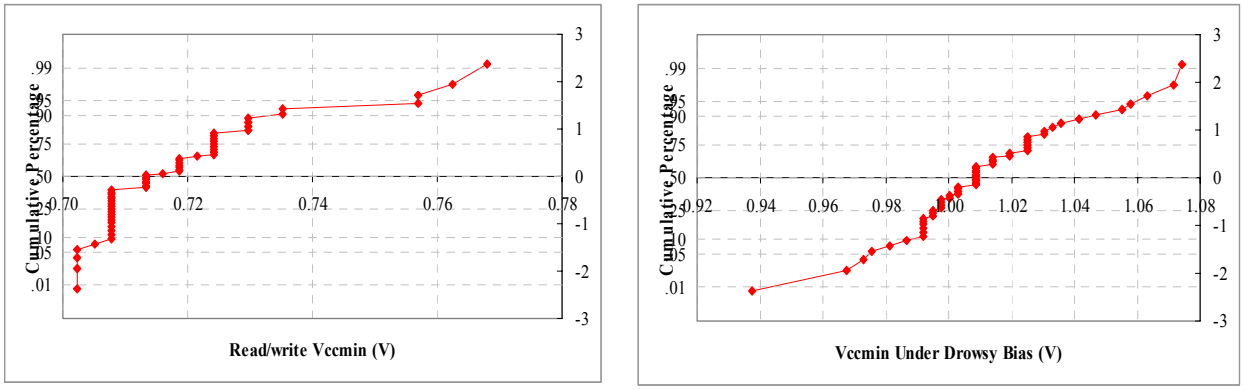

Figure 5: The measured Vccmin with active read and write operation and standby condition with drowsy back bias. Note the Vccmin is higher with drowsy bias. As the Vccmin tracks the high rail supply, the drowsy Vccmin is elevated as the Vss of the cell is raised with back bias.

length. Elaborate voltage regulator designs were implemented to control the NMOS and PMOS reverse bias. With the lowest amount of reverse bias, ~16X reduction in standby leakage for the 2MB array were realized in silicon that amounted to a cell leakage of only 20pA.

5. ACKNOWLEDGEMENTS

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