A Low Power Current Steering Digital To Analog Converter In 0.18 Micron CMOS

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ABSTRACT

This paper discusses a number of circuit techniques which address the DC and AC distortion performance of a low power current steering Digital-to-Analog Converter design. The design provides 14 bit resolution and 200 MSPS conversion rate in a 1P4M 0.18 micron CMOS process, with optional 3.3 volt compatible devices, while operating over a wide 3.6 to 1.8 volt supply range. A power dissipation / conversion rate figure of merit of as low as 0.17 mW/MSPS was achieved for 1.8V operation and as low as 0.28 mW/MSPS at 3.3V. SFDR of 70 dB is achieved at a 50 MHz output frequency.

Categories and Subject Descriptors: B.7.m [Integrated Circuits]: Miscellaneous

General Terms: Design.

Keywords: DAC, Converter, CMOS, Current Mode.

1. INTRODUCTION

Fine line CMOS technologies have become the process of choice for high sample rate switched current DAC design [1-5]. A 14 bit self calibrating DAC from [3] has a 0.2 mW/MSPS FOM but has limited SFDR performance of 50 dB at a 10 MHz output frequency. The DAC presented in [5] has a 0.06 mW/MSPS FOM but is only 10 bits and operates only at 1.5/1.8 volts. The 14 bit DAC presented in [4] has a 0.17 mW/MSPS FOM and does somewhat better in SFDR than [3]. There are important trade-offs to be made between low power consumption and dynamic performance at high output frequencies [3-5]. This design attempts to balance these trade-offs. In this implementation, use of mixed voltage process options allow the analog section to be powered from higher supply voltages than the digital section and thus provide larger output voltage compliance and swing. Many important applications for data converters in this class require output common mode voltages above the ground potential.

The basic structure of this design is shown in figure 1, with 14 bits of overall resolution. The most significant bit segment (5MSBs) is made from 31 unit weighted elements and is thermometer coded. Each unit element consists of a cascoded PMOS current source and a PMOS differential current switch pair. The remaining 9 bits of the DAC are further segmented into 4 thermometer coded intermediate bits with the 5 least significant bits binary coded.

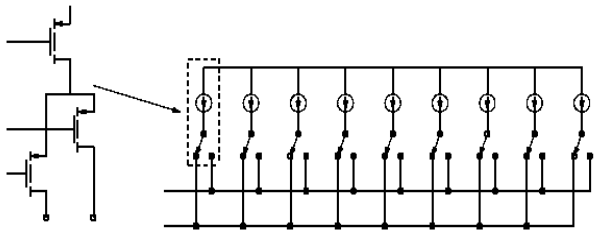

Figure 1. DAC Basic Structure

Power or supply current in a CMOS switch current DAC can be divided into three categories. The first comes from the digital logic and clock section and directly scales with the sample frequency and the data pattern. CMOS has the advantage that the power consumed will benefit from advances in process and supply voltage scaling. The second and third supply current categories are analog in nature. The full scale output current can be a big part of the current in the analog supply and can range from 1mA or less and up to 5mA in this design. The rest of the analog supply current is overhead and comes from the band gap reference and bias circuits.

2. DATA DEPENDENT CLOCK LOADING

A popular latch topology used in [1] is shown in figure 2. True and complements of the data are provided to inputs at D and DB and change only when CLK is low, NMOS transistors MN1,2 are off. When a rising edge transition occurs on the CLK input the value of D is transferred to S2 and DB is transferred to S1. When the CLK signal transitions back to a low state, falling edge, the state of S1 and S2 is held by the positive feedback around weak inverters INV1,2.

Due to the mixed-signal nature of a DAC, it is very likely that digital data activity on the die will cause interference in the analog and clock sections of the device. This becomes a more important performance issue as the signal power scales. An important special case of data pattern dependent interference comes from the varying load seen by the final clock buffer which drives the rank of final re-timing latches in the DAC. All latches to some extent present a load to the buffer driving the clock input of the latch that depends on if the state of the latch is changing or not. Given the finite strength of the buffer, the rise time of the clock waveform will be a function of the number of latches connected to this common clock buffer changing their state on a given clock edge. This results in a shift in time of the output samples which is a function of the

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absolute value of the rate of change of the waveform and thus gives rise to odd order distortions mainly third order.

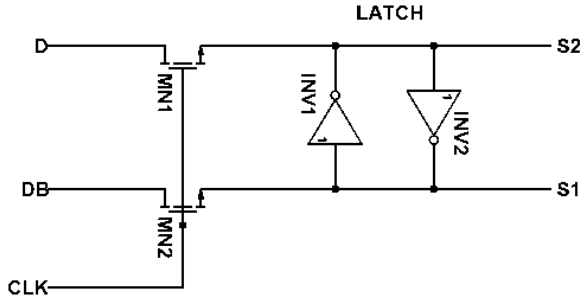

Figure 2. Final Latch Circuit

An example of this effect is shown in figure 3. The clock voltage waveform, normalized to time zero when the rising edge of the clock signal crosses mid supply (1.25 V), is plotted for the case of a single latch when the input data is and is not changing. This simulation shows a 2pSec difference. This effect is magnified when a large number of latches are driven by the same common clock buffer. In the case of thermometer coded data the number of data bits changing is proportional to the rate of change of the output waveform.

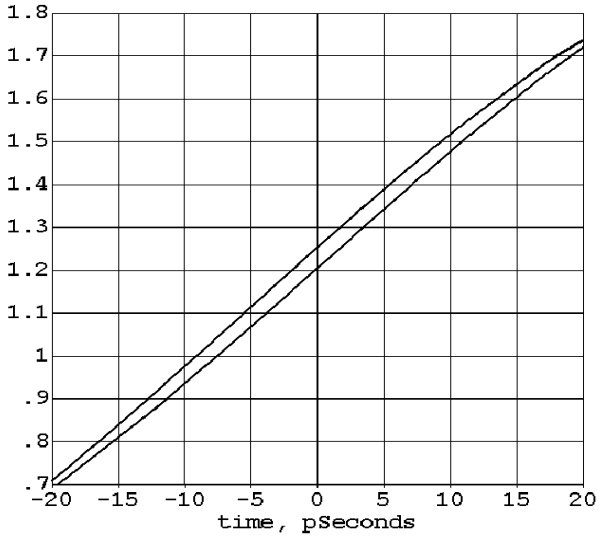

Figure 3. Data dependent clock delay

A modified version of the latch from [1] which addresses this problem is shown in figure 4 [6]. The top portion, which includes transistors MN1,2 and INV1,2 is the standard latch from fig. 2. The bottom portion is the compensating load which provides, through NMOS transistors MN3,4, a load which varies in a way opposite to the load provided by MN1,2.

The gate current that the buffer driving CLK needs to supply to transistor MN1 is a function of the relative voltage levels present at input D and output S2. If the voltage on D is the same as on S2 a slightly smaller amount of charge is needed to turn on MN1 than if D is not equal to S2. MN3 shares a drain connection with MN1 at input D, but the source is connected to the output of INV6. The voltage on the output of INV6 will be opposite INV1 because INV6's input is from INV3, an inverted version of output S1, the input of INV1. INV6 is a gated inverter and the output will be in a high impedance state when CLK is high and will be driven high or low when CLK is low.

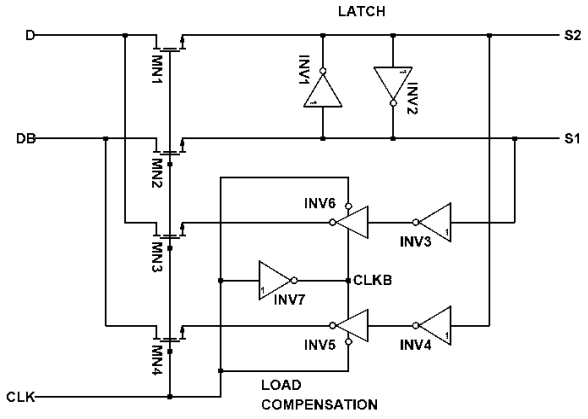

Figure 4. Constant Load Latch

It is clear that, for all possible combinations of the inputs and current state of the latch, of the four switches MN1,2,3,4 one will have high to low across S-D, one will have low to high across S-D, one will have high to high across S-D and one will have low to low across S-D. Therefore, as far as the charge that is needed to be supplied by the clock driver to turn on these four switches, it should be invariant with the data pattern.

Shortly after the CLK line goes high the latch formed by cross connected INV1 and INV2 will have regenerated making the signals levels across MN1,2 the same and INV5,6 will now be in tri-state equalizing the voltages across MN3,4. When CLK returns low MN1-4 turn off and INV5,6 come out of tri-state and the cycle is ready to start over again. The delay to switching INV5,6 into tri-state is about the same as the regeneration time of the latch. It is necessary to balance the relative strengths of the weak inverters, INV1,2, used in the latch, with the gated inverters INV5,6 to insure data independent loading on the clock driver.

3. SWITCH GATE DRIVE

The crossing point for the gate drive signals of the output current switch pair (from figure 1) needs to be optimized. The circuit that drives the differential switch should ensure that the current from the current source is always flowing at a constant value. For PMOS switches the low value of the gate drive waveform controls the on transistor. Where the gate signals cross each other should be higher than this low value by the Vgs of the switch device when all of the current is flowing in one device minus the Vgs with 1/2 of the current is flowing in each side of the switch. This minimizes the excursion of the voltage on the switch common source node during a transition and it should be symmetric around the nominal DC value. It is also important to point out that it is not necessary to bring the gates of the switch devices any higher than the voltage on the source when turning off the device (Vgs = 0). This reduces any

feed through of the gate drive signals to the outputs or the common source node.

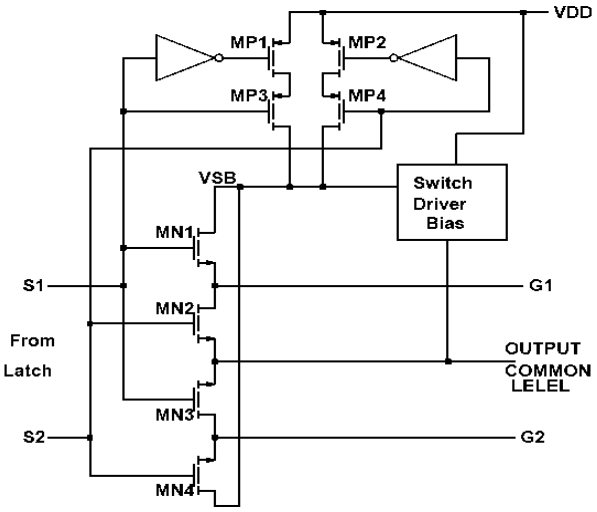

Figure 5. Output Switch Gate Driver

The circuit which produces the appropriate signals at the gates is shown in figure 5. The full supply rail swing outputs from the final latch, S1,S2 figure. 4, are used to turn on and off NMOS devices MN1-4 which connect the two outputs G1 and G2 to either the output common level or node VSB. The output common level is most often ground but in this design can be adjusted, external to the die, to accommodate interfacing to other circuits which may require that the common mode voltage be as much as 1.2V such as a mixer or modulator. The VBS node is driven to a voltage approximately the Vgs of the output switches above the output common level.

For each transition of the data a large narrow spike of current is drawn from the VSB node by devices MN1-4. Normally the switch driver bias block would need to be designed to supply this current and have sufficiently low impedance to settle back to its nominal value within one clock cycle. This often requires considerable static DC current, increasing the power consumed in the circuit. PMOS devices MP1-4 have been added to supply a similar narrow spike of current from the VDD power supply when a data transition occurs. This allows the switch driver bias block to be designed with much smaller static current. The power consumed by the circuit is now much more a function of the clock frequency and the data pattern. Two of the inverters, INV3,4, in figure 4 can also serve as the two inverters which drive the gates of MP1,2 in figure 5.

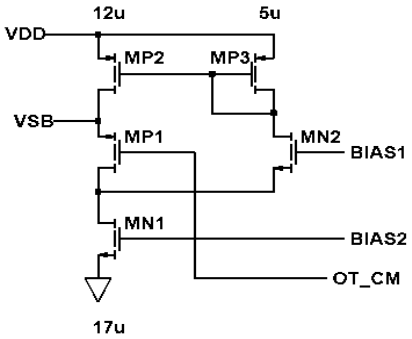

Figure 6. Switch Driver Bias Circuit

The switch driver bias generator is shown in figure 6. PMOS device MP1 is scaled to mimic one of the output switches. The voltage on node VSB will be equal to the voltage on node OT_CM (output common level from figure 5), plus MP1's Vgs. NMOS device MN1 determines the current level. A portion of MN1's current is diverted by MN2 and through the mirror gain of MP3 to MP2 supplies the current to the source of MP1. This feedback provides some degree of regulation and lowers the dynamic impedance at node VSB.

4. STATIC LINEARITY AND CALIBRATION

A foreground self calibration capability based on work previously reported in [2] has been implemented. Foreground calibration means that the DAC output can not be used during a self calibration cycle. In this approach, (figure 7), the current source to be calibrated, MP1, is measured against a master reference current from MP7 and the difference adjusted as close to zero as possible through the successive approximation register (SAR) logic and a CAL DAC which injects a small correction current in parallel with the main current source MP1.

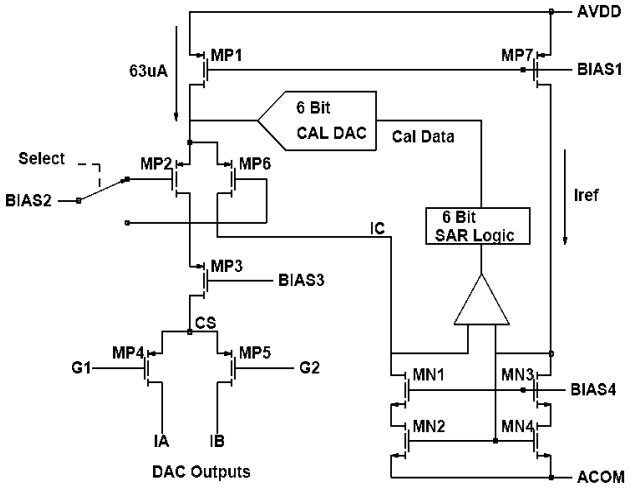

Figure 7. Static digital storage correction.

The switches MP2 and MP6, which redirect the current either to the output node or the calibration hardware act as first cascode devices. The gates are alternately switched to voltage BIAS2 which will fix the drain voltage of the main current source device, MP1, to be the same, within the matching of the Vgs of the two cascode switches, in both cases. This can result in a very accurate calibration. The additional circuitry used for the calibration is static and not clocked during normal operation and does not consume power or inject noise into the main signal path.

5. ACTIVE SECOND CASCODE

Operation over a wide range of supply voltages is an important feature of this design. The sensitivity of MOS threshold voltage, Vt, to the amount of reverse bias on the backgate with respect to the source is a significant effect in this process. The Nwells of all of the PMOS devices are connected to the positive supply, AVDD, as indicated in fig. 8. The gate bias, MASTER, for the main current source MP1, and the gate bias, FCAS, for the first cascode, MP2 are both generated with

respect to AVDD. The amount of backgate bias is fixed for these devices as AVDD varies. The gate of cascode MP3 and signals G1,G2 for output switches MP4,5 are generated with respect to ground or ACOM thus the Vgs of these devices, MP3-5, will vary strongly with the supply voltage. A second active cascode was incorporated as shown in figure 8. A scaled version of the unit cell, MP6-8 is used to generate the ACAS bias level which is common to all the unit cells. The Vgs of MP8 will track that of switches MP4, 5 as the voltage on AVDD varies. The gate of the active cascode MP3 will be driven optimally such that the Vds of MP3 is maintained just sufficiently in saturation for any value of AVDD. The lower limit on the supply voltage is reached when the Vds of the first cascode MP2 drops below its saturation level. An additional requirement for very high output impedance arises from the increase in the nominal output load resistance to 500 ohms from 50 ohms commonly used for 20 mA full scale currents.

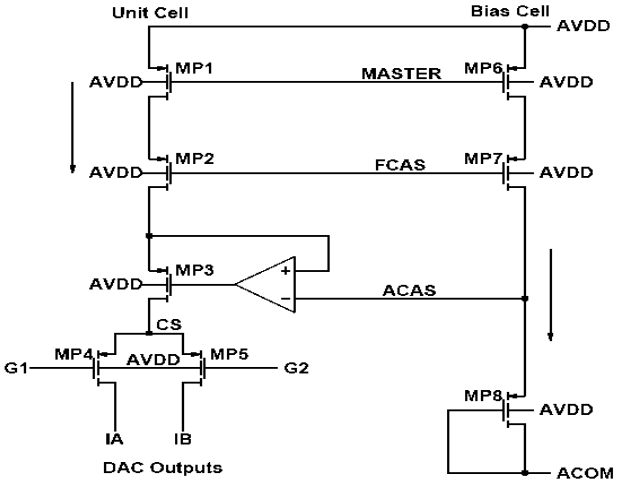

Figure 8. Active Cascode

Figure 9 is the schematic for the amplifier used in the active cascode. The amplifier uses a conventional NMOS input pair driving into a folded PMOS cascode output section. The total current consumed is just over 8uA. A wide signal bandwidth is not needed in this circuit. It is intended to track changes in the supply voltage, but not suppress fast disturbances.

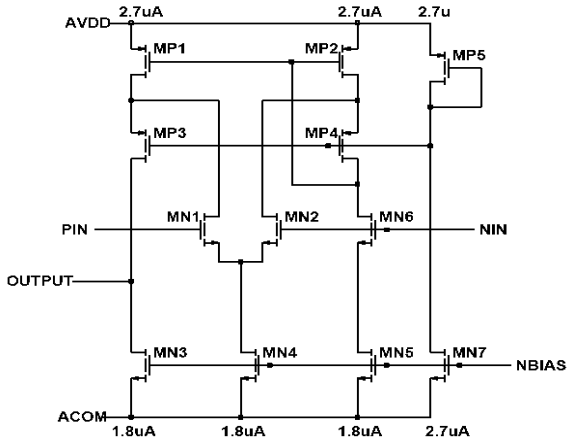

Figure 9. Active Cascode Amplifier

The voltage level at the inputs is the Vgs of MP8 (figure 8) which is sufficient for the Vgs of NMOS pair MN1,MN2 and the Vdsat of current source MN4. The output needs to be able to swing very close to ACOM so no output cascode was used on the NMOS current source MN3.

6. MEASURED RESULTS

The design was fabricated on a standard 0.18 micron, 1 poly, 4 metal CMOS process. A Deep Nwell option allows the use of a fully isolated vertical NPN transistor which was utilized in the on chip, 1.0 volt nominal, band-gap voltage reference. The full die size including bond pads, interface and all supporting blocks was 1.5 mm X 1.5 mm. The overall results are summarized in table 1.

Table 1. Performance Summary

Resolution	14 Bits
Supply range	1.8 V to 3.6 V
Full Scale Current	1-5 mA, 2 mA nominal
Output voltage swing	1 Volt PP
Output Common Mode Range	0 to 1.2 Volts
Max Sample Rate	200 MSPS @ 3.3 V 80 MSPS @ 1.8 V
INL / DNL uncalibrated	+/- 3 LSB , +/- 2.5 LSB
INL / DNL self-calibrated	+/- 0.6 LSB , +/- 0.9 LSB
SFDR	> 70 dB @ 50 MHz Fout
IMD (two tone)	> 75 dB @ 70 MHz Fout
Current - Analog section	2.5 mA + I full scale
Current – Digital/clock section	22 uA / MSPS @ 1.8V 56 uA / MSPS @ 3.3V
Process Technology	0.18 micron 1P4M CMOS
Die Size (including pads)	1.5 mm X 1.5 mm

The power vs. clock frequency is plotted in figure 10 for a fixed Fout/Fclk = 1/10. The output current was set at the nominal level of 2mA. The supply voltage is set at 1.8V. The analog portion of the power is relatively independent of the clock frequency where the power for the digital and clock portions scales linearly with the clock frequency. The design has been shown to operate successfully down to 1.5 volts when the full scale current is lowered to 1mA.

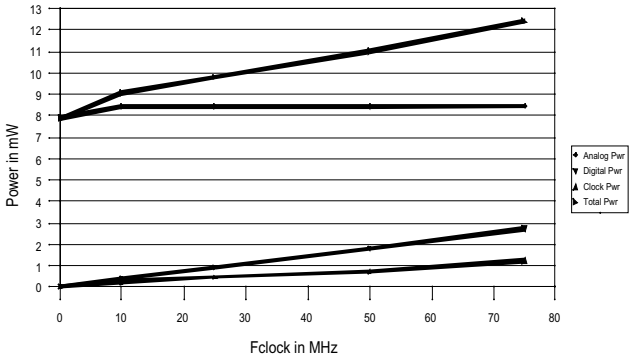

Figure 10. Power vs. Clock Frequency

Careful layout of the devices in the main current sources resulted in the uncalibrated INL and DNL for a typical device as plotted in figures 11 and 12. The INL is +3/-2, 14 bit LSBs.

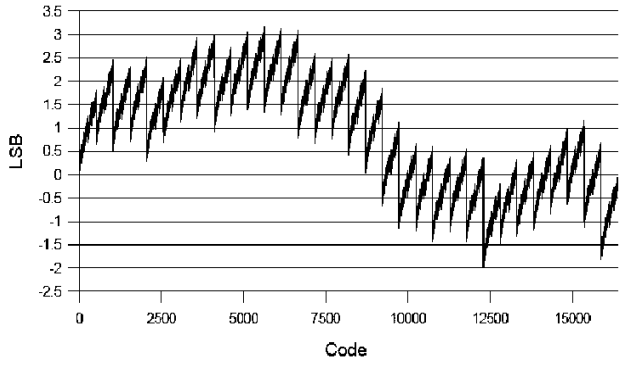

Figure 11. Uncalibrated INL (14 bits)

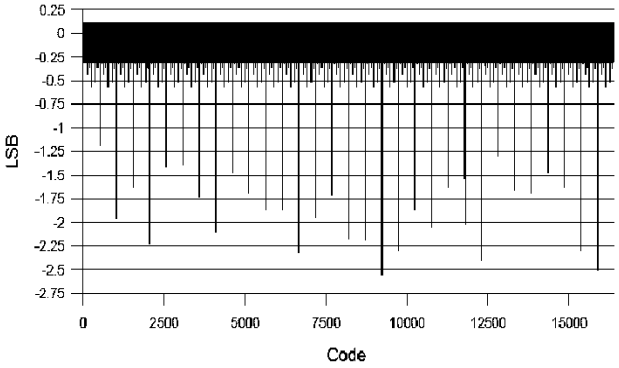

Figure 12. Uncalibrated DNL (14 bits)

The INL and DNL after running the on-chip self calibration cycle is plotted in figures 13 and 14. The INL has been improved to 0.6, 14 bit LSBs and the DNL has been improved to less than 1 14 bit LSB from more than 2.5 LSBs uncalibrated (figure 14) and the DAC is now monotonic at the 14 bit level

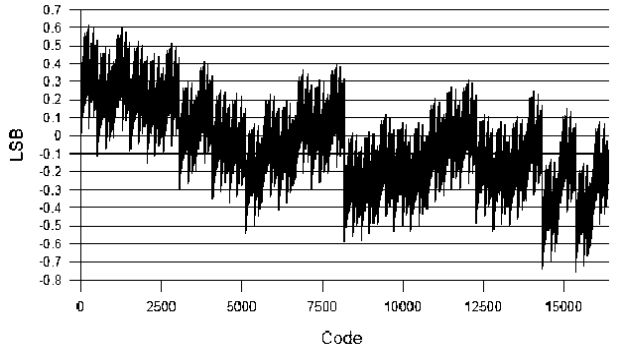

Figure 13. Calibrated INL (14 Bits)

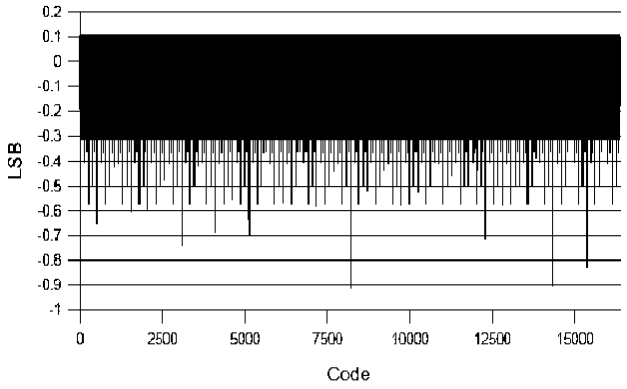

Figure 14. Calibrated DNL (14 bits)

A representative output spectrum for a single tone at 10 MHz and 125 MSPS is shown in figure 15. The HD2 and HD3 are -77 dBc and -78 dBc respectively.

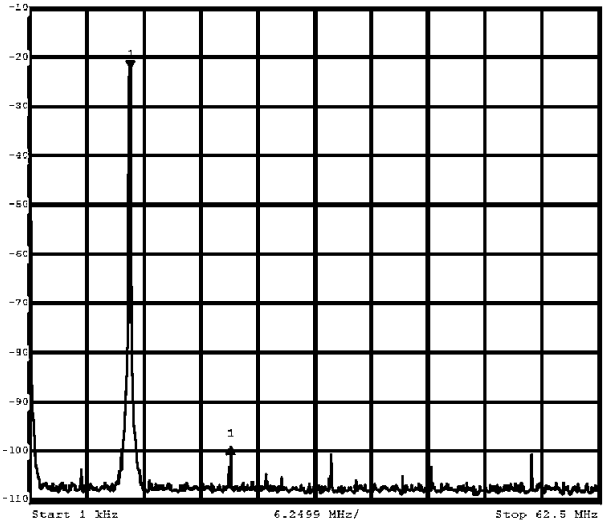

Figure 15. Single Tone output spectrum

A plot of the SFDR vs. output frequency at 200 MSPS and 3.3 Volt power supply is shown in figure 16. The DC linearity limited performance of 85 dB starts to fall off as the dynamic effects start to dominate at higher frequencies. The SFDR maintains approximately 60 dB at 90 MHz.

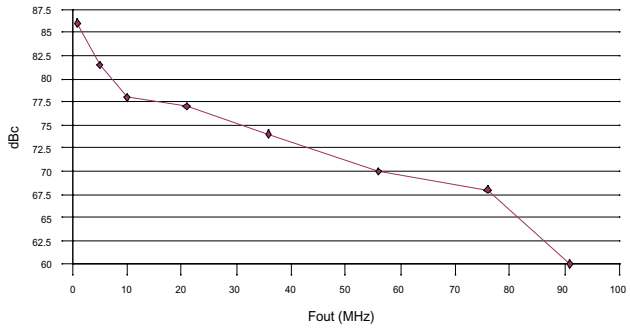

Figure 16. SFDR 2mA I full scale, 3.3 V, 200 MSPS

Two Tone intermodulation distortion is an important performance measure. The effect of the data dependent clock loading is evident mainly at higher output frequencies. Two cases are shown in the next figures where the 3rd order IMD spurs can be seen without the compensating loads, (figure17) vs. when the clock compensating loads are included in the circuit (figure 18).

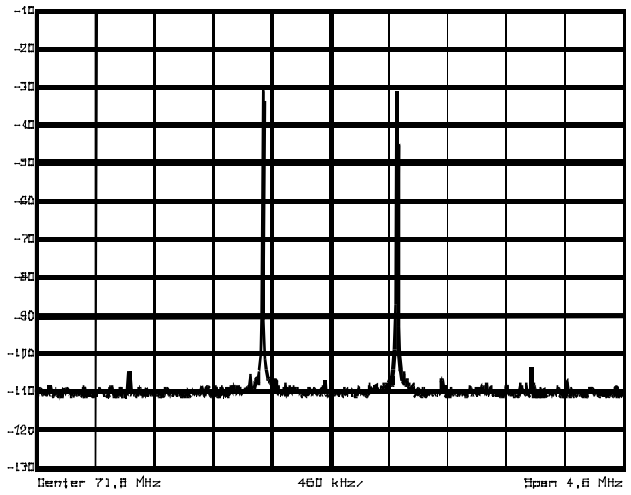

Figure 17. Two Tone spectrum, constant clock load disabled

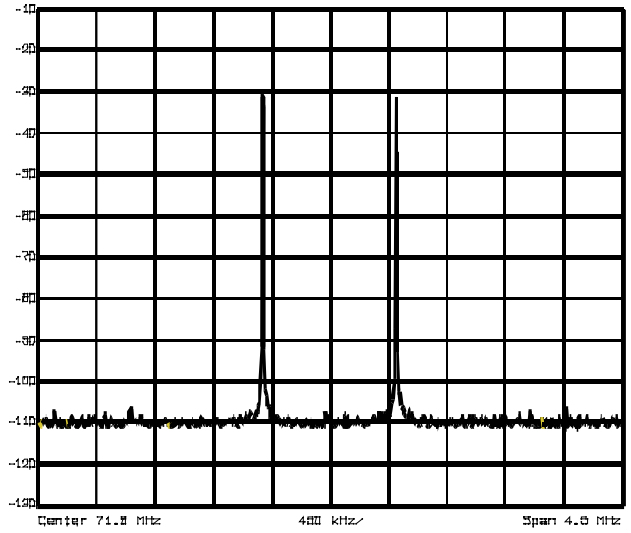

Figure 18. Two Tone spectrum, constant clock load enabled

The two tones are spaced 1 MHz apart centered on 71.8 MHz at a sample rate of 175 MSPS. The 3rd order IMD improves 7 dB with the new clock load compensating circuit

The photo of the 1.5mm X 1.5mm prototype die is shown in figure 19. The die was evaluated in a 32 pin 5mm X 5mm LFCSP package.

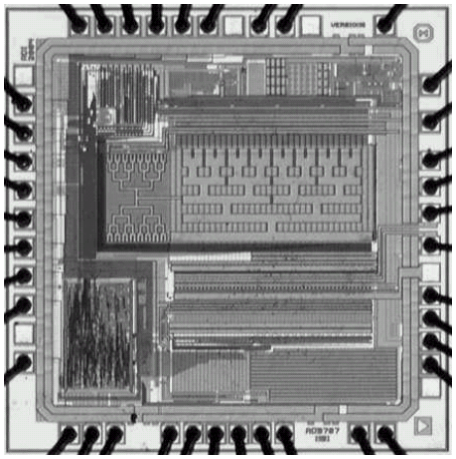

Figure 19. Die Photo

7. CONCLUSIONS

A low power, wide supply range, 14 bit switched current DAC has been implemented in a 0.18 micron standard CMOS process. An on chip self calibration structure was used to achieve true 14 bit accuracy. Novel circuit techniques were used which resulted in AC distortion performance equal to high power DACs with dissipation as much as 10 times larger. Use of mixed voltage process options allows the flexibility to interface with other parts of the signal chain which may require that the output signal common mode voltage be as much as 1.2 volts with 3.3 volt supply operation.

8. ACKNOWLEDGMENTS

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