# A 9.5mW 4GHz WCDMA Frequency Synthesizer in 0.13µm CMOS

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## ABSTRACT
A 4GHz integer-N frequency synthesizer is realized in a 0.13µm CMOS technology. It has a 400kHz reference frequency and 40kHz loop bandwidth such that 2GHz quadrature LO signals can be generated after a divide-by-two, with channel raster of 200kHz. The measured in-band phase noise is -74dBc/Hz @4kHz offset. A self-regulated charge pump is proposed to improve matching as well as charge sharing. Reference spurs are thereby kept below -55dBc over the VCO tuning voltage from rail to rail. The requirements for UMTS transceiver have been fulfilled with an overall power consumption of 9.5mW, which is the lowest reported to date. Core area of the chip is as small as 0.2mm$^2$.

## Categories and Subject Descriptors
B.7.0 [**Integrated Circuits**]: General

**General Terms:** Design, Verification

**Keywords:** WCDMA, Frequency Synthesizer, Phase-Locked Loop, Low Power, CMOS

## 1. INTRODUCTION
Third-generation (3G) cellular radio services based on the wideband code division multiple access (WCDMA) standard have finally been launched in more than twenty countries and the market for such mobile terminals are forecast to grow significantly in the next few years. The digital baseband chips for WCDMA transceivers are being developed in CMOS technologies of 130nm gate length or below to limit the cost and power consumption while coping with substantially higher amount of signal processing than earlier generations of cellular standards. There is a strong argument for realizing the RF transceiver chip in the same fine-line technologies [1,2] despite challenges in low voltage analogue and RF design, and the feasibility to do so in 130nm CMOS has been demonstrated for both the RF receiver [1] and transmitter [2]. This contribution describes the first WCDMA frequency synthesizer in 130nm CMOS, with an emphasis on low power.


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In contrast to GSM, where in TDMA mode of operation a lower duty cycle helps curtail power consumption, the FDD WCDMA standard requires both the receiver and transmitter to operate continuously. Power consumption is therefore one of the limiting factors in the potential success of 3G cellular services and low power design has never been more important for the RF receiver, transmitter and frequency synthesizers of the mobile terminal. In the past few years, remarkable progress has been made in WCDMA RF CMOS receivers and transmitters to bring down their power consumption to 50mW and 70mW [1-4], respectively, which brings the relatively high synthesizer consumption into sharper relief. To limit the overall RF transceiver power to 150mW, for example, the consumption of each synthesizer needs to be below 15mW. The majority of published CMOS synthesizers are well above such a level.

## 2. FREQUENCY SYNTHESIZER ARCHITECTURE
The most appropriate architecture of an RF synthesizer for a given cellular application is determined by a variety of requirements, chief among them phase noise, spurs at the reference or other frequencies, switching time, tuning step and range, as well as resilience to frequency pulling by the transmitter or another synthesizer. Both the close-in phase noise, which affects the error vector magnitude (EVM), and the switching time improve with a wider bandwidth for the loop filter in a PLL-based synthesizer, but stability considerations and the presence of reference spurs limit the loop bandwidth to a small fraction of the reference frequency.

Fractional-N synthesizer architectures have received much attention recently as they allow the reference frequency to be significantly higher than the minimum frequency resolution of the synthesizer. The increase in reference frequency is meant to allow the bandwidth of the loop filter to increase, so that frequency switching takes place faster, and the EVM of the receiver or transmitter can improve with reduced close-in noise of the synthesizer. ΣΔ modulation is however typically needed for the frequency division to mitigate the fractional spurs associated with such synthesizers, which introduces high frequency quantization noise into the phase-locked loop. In theory such noise can be suppressed by the loop filter, but since the latter's order is limited by the stability of the loop, most fractional-N synthesizers end up using narrow filter bandwidths anyway in order to achieve sufficient removal of quantization noise. Better suppression of reference spurs remains an advantage for the fractional-N synthesizer, but fractional spurs arise as a problem, especially in

synthesizers where both the reference frequency and the loop bandwidth are high relative to the channel spacing, so that residual reference spurs both in-band and in the adjacent channels do not get the full benefit of loop filtering [5]. From the standpoint of power, the presence of high frequency quantization noise imposes tougher requirements on the building blocks of the PLL. To avoid folding the high frequency noise, which increases the close-in or in-band portion of the phase noise floor, high linearity is needed for each circuit in the loop through which the quantization noise passes. This typically entails high power consumption.

In a fully integrated WCDMA transceiver the issue of isolation between the transmitter, the synthesizers and the receiver is already complicated. Two fractional-N synthesizers will both require complex digital circuitry, which introduces further uncertainties in terms of cross-coupling interferences within a single chip context.

Given the above considerations, we came to the conclusion that the integer-N PLL architecture, shown in Figure 1, represents an equally attractive alternative to the fractional-N PLL in terms of satisfying WCDMA requirements, facilitating a single chip implementation, and, above all, achieving the lowest power consumption, provided that reference spurs can be kept under control through careful design.

To facilitate quadrature generation for a direct conversion transceiver, we operate the VCO at round 4GHz, twice the desired LO frequency. This makes it less vulnerable to pulling by the transmitter, and enables the reference frequency of the PLL to be doubled to 400kHz, twice the channel raster. This also allows the loop bandwidth to be doubled from 20kHz to 40kHz, so that close-in noise floor is 6dB lower and switching time is halved.

Referring to the block diagram in Figure 1, the frequency synthesizer implemented in this work is based on a charge-pump phase-locked loop architecture. The 4GHz VCO directly drives a dual-modulus divide-by-64/65 prescaler. The feedback frequency divider is formed by the prescaler, a 7-bit programmable swallow counter and an 8-bit programmable accumulate counter, which provides full programmability to the overall division ratio N. A 7-bit programmable reference divider supports external crystal oscillators with different frequencies including industry standard 26MHz or 19.2MHz.

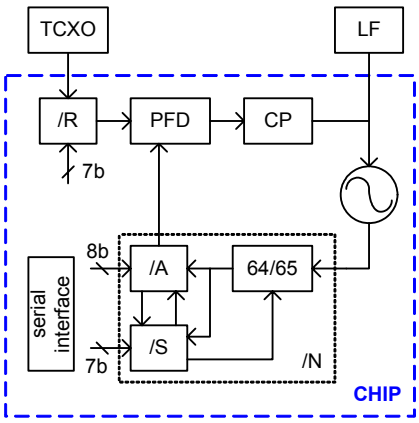



**Figure 1. Frequency synthesizer block diagram**

# 3. SYNTHESIZER REQUIREMENTS

The UMTS synthesizer requirements are summarized in Table 1. The phase noise of -130dBc/Hz at 15MHz offset, which causes reciprocal mixing, is derived from the in-band blocking test case. Thanks to the doubling of loop bandwidth, 200µs switching time becomes easier to achieve and the close-in noise floor is relaxed by 6dB to -75dBc/Hz. Phase noise related EVM degradation is limited to 3%, which is a small fraction of the overall 17.5% permitted.

Because the overall division ratio between the VCO output and the reference frequency is very high in an integer-N synthesizer for WCDMA (~10'000), the noise requirement for the base-band circuitry is very stringent. Referring the –75dBc/Hz output noise to the point of frequency comparison of the PLL, the requirement can be expressed alternatively as the synthesizer phase noise floor, which identifies the noise contributed by the digital dividers and switches in the phase-frequency detector (PFD) and the charge pump: $PN_{floor} = PN_{in\_band} - 10\log(f_{comp}) - 20\log(N)$

where $f_{comp}$ is the PFD comparison frequency and $N$ is the overall division ratio ($f_{VCO}/f_{comp}$). In order to achieve an in-band noise of $PN_{in\_band}$ = -75dBc/Hz, the synthesizer should have a noise floor lower than -211dBc/Hz, which requires state-of-the-art design for all digital blocks.

Inside the 1.94MHz band, the reference spurs need to be under –50dBc, to limit EVM degradation in the receiver and ACLR degradation in the transmitter. To ensure that the synthesizer is sufficiently fast for the compressed mode and extendable to DCS operation in a WCDMA/ DCS dual-mode operation, the switching time is set to less than 200µs.

**Table 1. UMTS synthesizer requirements**

| | | |
|---|---|---|
| VCO tuning range | > 10% | 3% necessary plus margin for process tolerance |
| Frequency resolution | 200kHz | Channel raster |
| Phase noise | < -130dBc/Hz @ 15MHz from 4GHz carrier[*1] | Due to reciprocal mixing |
| In-band noise floor | < -75dBc/Hz from 4GHz carrier[*1] | 40kHz loop bandwidth[*2] |
| Spurs | < -50dBc | In-band (offset < 1.94MHz) |
| Switching time | < 200µs | Compatible with DCS 1800 |
| Power consumption | < 15mW | As low as possible |
| Die area | < 0.5mm$^2$ | As small as possible |

[*1] 6dB lower when referred to 2GHz carrier

[*2] With 40kHz loop bandwidth, 3% EVM due to integrated phase noise (EVM must <17.5% for a complete transmitter)

# 4. CIRCUIT DESIGN

## 4.1 Voltage-Controlled Oscillator

The voltage-controlled oscillator (VCO) is the most critical building block in a frequency synthesizer. The schematic of our

implementation is shown in Figure 2. In order to mitigate the limitation of the output swing due to low supply voltage, the oscillation nodes are biased at 1.2V VDD. The resonator consists of a differential spiral inductor and two accumulation-mode MOS varactors. A relatively large inductance of 4nH has been chosen for high L/C ratio, to achieve low phase noise. The inductor is optimized for a good quality factor (Q) as well as a small dimension to reduce parasitic capacitances. It consists of 3 stacked layers connected in series, the first layer being the thick top metal (M6) and the other two layers each consisting of two levels of metal in parallel (M5//M4 and M3//M2). Inductor dimensions are thus minimized, measuring only 120µm by 120µm. At 4GHz, a Q of 8 is achieved, according to HPADS Momentum simulation. MOS varactors are used in this design for their wide tuning range and high linearity. The tuning range should cover both the range required for selecting the RF channels (3%) and the VCO frequency tolerance due to process variations of the inductors and parasitic capacitances. A good linearity makes loop characteristics more predictable, which is beneficial to the robustness of the PLL design. The varactors are made of thick-oxide transistors and the VCO tuning voltage centers at 1.2V.

To fully exploit the MOS varactor tuning range, the charge pump needs to provide a tuning voltage higher than 1.2V. The charge pump is therefore constructed with thick oxide transistors and runs off 2.5V, at only 1mA bias current. The VCO amplitude is designed to be 800mV (differential) with just 2mA bias current.

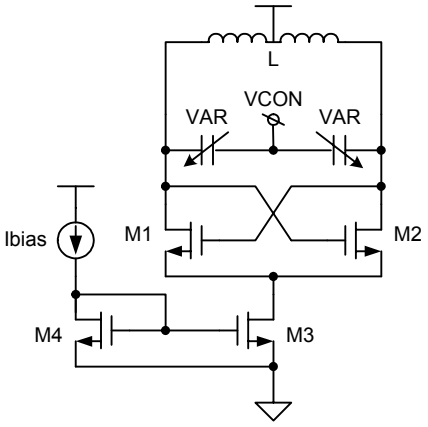



**Figure 2. Schematic of the implemented VCO**

## 4.2 Prescaler-by-64/65

The prescaler-by-64/65 is implemented in current mode logic (CML) and its block diagram is shown in Figure 3. NAND and OR gates are incorporated into synchronous flip-flops to save power [6]. Sine the supply is limited to 1.2V, the internal swing of each stage is set to be 200mV (single-ended peak voltage), and all stages are DC coupled without level converters. The bias current of each stage is scaled according to the frequency at which the stage operates. Special attention has been paid to layout to minimize wiring capacitance and thereby power consumption. The prescaler input sensitivity curve is simulated with extracted parasitic capacitances as shown in Figure 4. It shows that for an input signal with a (differential) swing of 400mV, the prescaler operates robustly up to 8GHz for only 5mW power consumption.

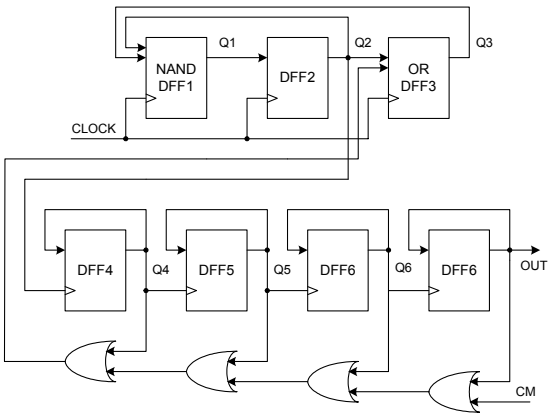



**Figure 3. Prescaler block diagram**

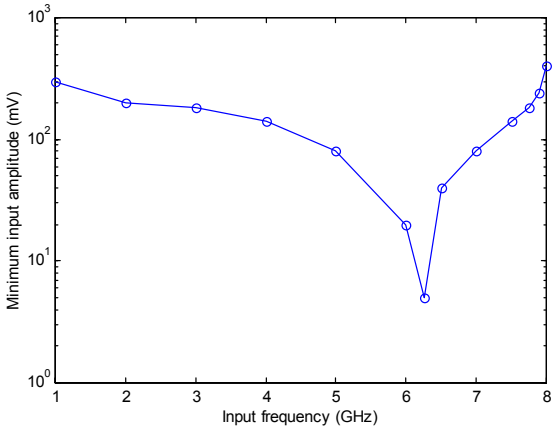



**Figure 4. Prescaler input sensitivity**

## 4.3 Digital Programmable Counters

The asynchronous digital programmable dividers (reference divider, swallow counter and accumulate counter) are implemented with standard cells. The outputs of the swallow counter (S counter) and accumulate counter (A counter) are resynchronized by the prescaler output with fully custom-designed flip-flops (as shown in Fig. 5) to prevent jitter accumulation and thereby reduce the PLL in-band noise floor.

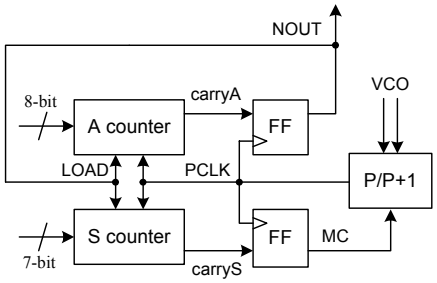



**Figure 5. Resynchronization of the digital counters**

## 4.4 PFD and Charge Pump

A commonly used tri-state phase-frequency-detector consists of two flip-flops and one AND-gate, as shown in Figure 6. The purpose of adding a reset path delay is to eliminate dead-zone and maintain PFD linearity. This delay, on one hand, should be long

enough to remove any dead-zone, while on the other hand, should be as short as possible to guarantee low charge pump noise and low spurs. Thus the PFD critical paths should have sharp rising and falling edges so that the minimum reset delay is achievable. As standard cells are not fast enough, the PFD is a full-custom design based on the structure proposed in reference [7].

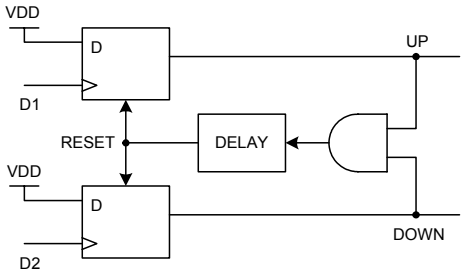
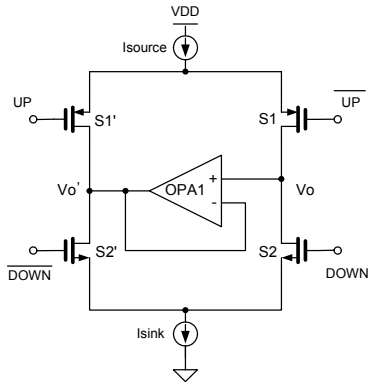


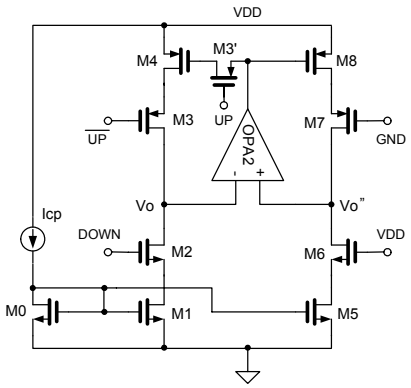

**Figure 6. Simplified schematic of the tri-state PFD**

High performance charge pump with good matching between the two current sources $I_{sink}$ and $I_{source}$ is critical to achieving low PLL reference spurs. Traditionally, high output impedance should be guaranteed for $I_{sink}$ and $I_{source}$ by long transistors or cascode structures to provide good matching. Even so, good matching over the full tuning voltage is difficult because of the large voltage excursion of the current sources. Figure 7 shows approaches that can be used to improve matching. Figure 7(a) shows that a unit-gain buffer based on a rail-to-rail operational amplifier (OPA1), together with dummy switches S1' and S2', can reduce charge sharing during switching transients, but does not guarantee $I_{sink}$ to be the same as $I_{source}$ for the full range of $V_o$. To improve matching under large voltage excursion a novel self-regulated charge pump circuitry is introduced, as shown in Figure 7(b). The regulating amplifier (OPA2) improves the matching between $I_{sink}$ and $I_{source}$ against tuning voltage variations through a replica bias branch, but does not fully address charge sharing. A comparison of matching performance between such an implementation and a traditional charge pump is shown in Figure 7(c). Since the up-switches are only on for very brief moments during steady-state operation switch M3', introduced to prevent OPA2 from having a partial positive feedback loop, is not strictly necessary. Experiments show that the PLL operation is stable even with the gate of M4 permanently connected to the output of OPA2. To address both charge sharing and matching of current sources, the techniques in Figure 7(a) and 7(b) can be combined, resulting in the charge pump schematic shown in Figure 7(d). Free of charge sharing and current source mismatch, the reference spurs are substantially improved. The charge pump is supplied from a 2.5V source and its main current sources are set to 500μA, in order to keep loop filter noise moderate. To save power, the replica branch current is scaled down by a factor of 5 to 100μA and reused by the second stage of OPA2. The current consumption of the complete charge pump, including the amplifiers, is less than 1mA.

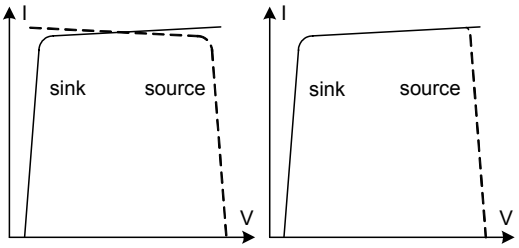
The 1.2V-to-2.5V level-converter and the buffer driving the charge pump switches are carefully designed for high speed. Simulation of the PFD-CP-LF combination shows that minimum turn-on time of 0.2ns is achieved without harming linearity. Such short turn-on time also helps to reduce the noise contribution of the charge pump current sources to the PLL.



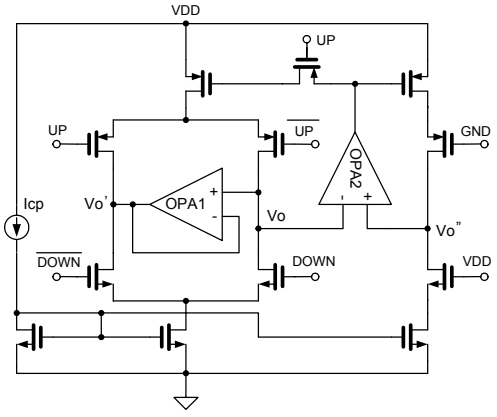

**(a) Unit gain buffer and dummy switches (S1' and S2') reducing charge sharing**




**(b) Replica branch and regulating amplifier improving current sources static matching**




**(c) Matching performance comparison between traditional and proposed charge pump in (b)**




**(d) Combination of the two techniques in (a) and (b)**

**Figure 7. Schematic of the proposed charge pump**

## 5. EXPERIMENTAL RESULTS

The synthesizer chip has been fabricated in a 6-metal/1-poly 0.13µm CMOS technology with MIM capacitor option. Its die micrograph is shown in Figure 8. The area is pad-limited (1mm$^2$ including pads, ESD protection, and decoupling capacitors) and the core area is just 0.2mm$^2$, which is among the smallest reported to date.

All measurements have been performed in closed-loop, with an external 19.2MHz reference crystal oscillator and a second-order loop filter. The loop bandwidth is calculated to be slightly higher than 40kHz.

The VCO can be locked without modifying the loop filter over the entire tuning range. The measured tuning curve is shown in Figure 9. The nominal frequency is a little too high due to over-estimation of the wiring parasitic capacitance. This has been corrected in the transceiver in which the synthesizer is incorporated.

The 10% tuning range is enough to cover either the intended UMTS receive or transmit band (120MHz, 3%) with sufficient margin without switched capacitor band switching. The tuning curve is very linear and a relatively constant VCO gain of 350MHz/V has been measured over most part of the tuning range.

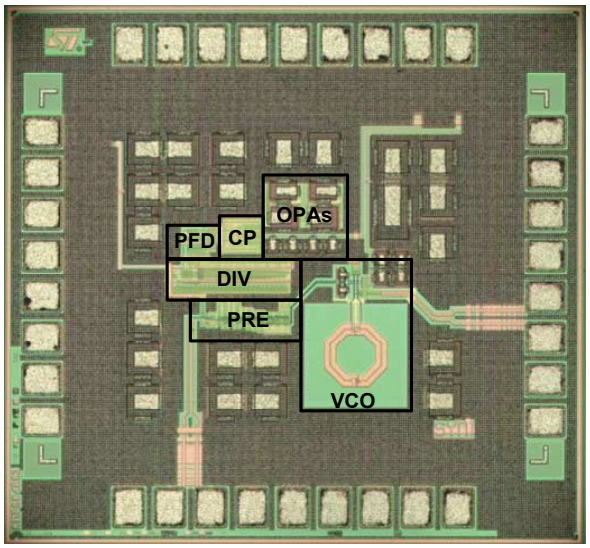



**Figure 8. Synthesizer chip die micrograph**

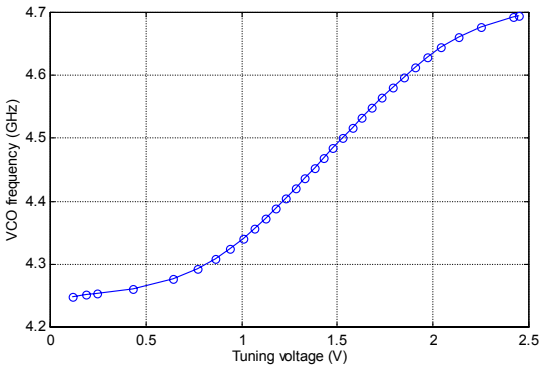



**Figure 9. VCO tuning curve**

The measured closed-loop synthesizer phase noise is shown in Figure 10. The phase noise is -136dBc/Hz at 15MHz offset from 4.4GHz carrier, which is dominated by the VCO. This satisfies the UMTS requirement with 6dB margin. Due to intrinsically high flicker noise of our 0.13µm gate-length transistors, the VCO suffers from flicker noise up-conversion at low offset frequencies, which increases the PLL in-band noise by a few decibels. The measured in-band noise density remains nonetheless between -70 and -74dBc/Hz, which yields a synthesizer noise floor as low as -210dBc/Hz. The integrated noise from 1kHz to 1.92MHz is -21dBc, or -27dBc when referred to the 2GHz carrier. The resulting transmitter EVM degradation is 4.5%, slightly higher than planned but satisfying UMTS requirement with a large margin.

Measured reference spurs (Figure 11) are below -55dBc even when the VCO tuning voltage is close to VDD or GND, which validates the proposed charge pump circuit. Considering the fact that the reference frequency is relatively close to the loop bandwidth (400kHz/40kHz), one can infer that the charge pump performance is superior to many recent designs in which the reference frequency to loop bandwidth ratio is much higher.

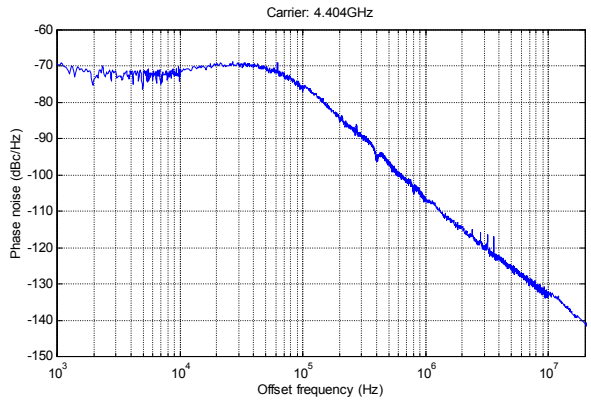



**Figure 10. Synthesizer phase noise**

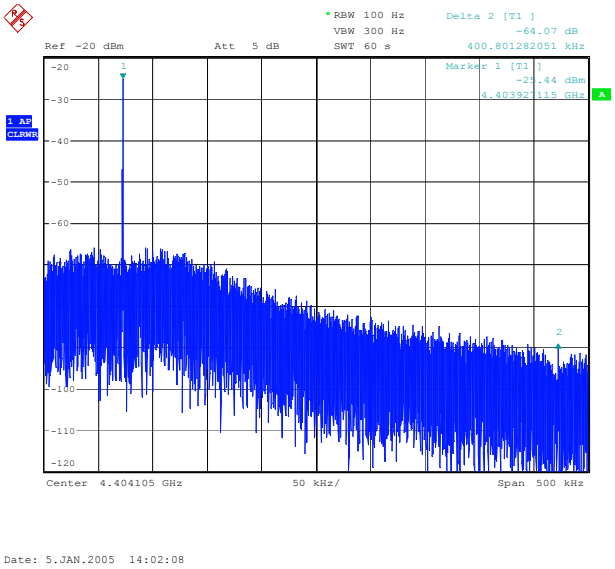



**Figure 11. Synthesizer reference spur measurement**

# 6. CONCLUSIONS

A 4GHz integer-N frequency synthesizer, including an on-chip VCO, has been successfully implemented in a 0.13µm standard CMOS technology. With the proposed self-regulated charge pump improving current matching, reference spurs that tend to be problematic in integer-N synthesizers have been reduced to appropriate levels, even with a relatively wide loop bandwidth. The overall performance, summarized in Table 2, meets UMTS specifications with a low power consumption of 9.5mW, which is by far the lowest reported to date.

The low power aspect has been taken into consideration during each design stage. Power consumption has therefore been minimized for all critical circuit blocks, including the VCO, prescaler and charge pump. With compact layout the chip occupies a core area of less than 0.2mm$^2$, which is a favorable attribute for a single chip UMTS transceiver.

**Table 2. Synthesizer performance summary**

| | |
|---|---|
| Technology | 0.13µm standard CMOS |
| Architecture | Integer-N |
| VCO tuning range | 4.24 ~ 4.7GHz (~10%) |
| PFD frequency | 400kHz |
| Frequency resolution | 200kHz |
| Loop filter | 2$^{nd}$-order, external<br>42 pF, 390 pF and 22 kΩ |
| Loop bandwidth | 40kHz |
| Phase noise | -74dBc/Hz @4kHz<br>-136dBc/Hz @15MHz<br>from 4.4GHz carrier |
| Integrated noise | -27dBc referred to 2GHz carrier |
| Reference spurs | < -55dBc |
| Settling time | < 120µs (120MHz step, settle to 0.1ppm accuracy)* |
| Supply voltage | 1.2V & 2.5V (charge pump) |
| Power consumption | 9.5mW (VCO 2.4mW, Prescaler 5mW, charge pump 2mW) |
| Die area (core) | 0.2mm$^2$ |

* Estimated from 40kHz loop bandwidth

In table 3, some recently published fully integrated CMOS VCOs are listed. It is clearly seen that our VCO has a state-of-the-art figure of merit (FOM) performance, as defined in [8], with extremely low supply voltage and low power consumption.

**Table 3. Performance of some recently published fully integrated CMOS VCOs (phase noise is recalculated to 4.4GHz at 15MHz offset)**

| VCO | Tech. [µm] | Supply [V] | Power [mW] | PN [dBc/Hz] | FOM [dBc/Hz] |
|---|---|---|---|---|---|
| [8] | 0.25 | 2.5 | 20 | -149 | -188.5 |
| [9] | 0.25 | 1.5 | 24 | -138 | -174.1 |
| [4] | 0.18 | 1.8 | 3.6 | -128 | -171.9 |
| This | 0.13 | 1.2 | 2.4 | -136 | -181.6 |

Table 4 compares some WCDMA frequency synthesizers in terms of technology and power consumption. It indicates this design has made a remarkable progress towards the low cost and low power implementation of WCDMA RF transceivers.

**Table 4. Performance of some published WCDMA frequency synthesizers**

| Design | Technology | Power | On-chip VCO |
|---|---|---|---|
| [10] | 0.5µm BiCMOS | 17mW | No |
| [11] | 0.5µm BiCMOS | 55mW | Yes |
| [5] | 0.18µm CMOS | 28mW | Yes |
| This | 0.13µm CMOS | 9.5mW | Yes |

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