Measurements and Modeling of Intrinsic Fluctuations in MOSFET Threshold Voltage

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ABSTRACT

Fluctuations in intrinsic linear V_T, free of impact of parasitics, are measured for large arrays of NMOS and PMOS devices on a testchip in a 150nm logic technology. Local intrinsic σV_T, free of extrinsic process, length and width variations, is random, and worsens with reverse body bias. Although the traditional area-dependent component is dominant, a significant component of the fluctuations in small devices depends only on device width or length.

Categories & Subject Description

B.7.0 Integrated Circuits, B.8.0 Performance and Reliability

General Terms

Design, Measurements, Performance, Theory

Keywords

CMOS, Integrated Circuits, Transistors, Variation, Threshold Voltage, Vt, Vt Variation, Threshold Voltage Variation, Process Variation, Random Dopant Variation, Body Bias, Mismatch, Transistor Mismatch, Transistor threshold voltage mismatch, Vt Mismatch

1. Introduction

Local intrinsic variations and mismatches of MOSFET threshold voltages (V_T), dictated by device physics rather than manufacturing process control, are emerging as key limiters to SRAM cell area and overall density scaling in high-performance CMOS logic technology [1].

In this paper, we describe measurement, extraction and modeling of different extrinsic and intrinsic components of V_T fluctuations from a testchip (Figs. 1 & 2) implemented in a 150nm high performance logic process technology. The testchip contains six NMOS and six PMOS device arrays for measuring statistical I-V variations. Isolated device structures are also included adjacent to the arrays for more detailed electrical characterizations of individual devices. Each 650µm X 150µm array contains 4096 transistors (16 rows X 256 columns) along with (1) decoder circuits to select and measure full I-V characteristics of any device in the array, (2) facilities to apply forward and reverse body bias to the devices, and (3) gate-underdrive leakage control circuits to reduce impact of the leakage currents of the unselected devices on I-V measurement of a selected device in the same row. In addition, a differential current measurement procedure (Fig. 1) is used to minimize impact of parasitic leakages of unselected devices on measurement accuracy.

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2. Intrinsic linear V_T Measurements

Several drawn lengths (L) and widths (W) are used for a set of small target NMOS and PMOS devices (Fig. 2) to cover a sufficiently large range of active device area. For each small target device in an array with a specific W & L, corresponding square, narrow and short device structures are implemented in the same array (Fig. 2) to examine dependence of V_T variations on device dimensions around the target value. In any array, 1024 devices of identical drawn dimensions are implemented in 4 rows, each containing 256 devices, to allow robust computation of local variation statistics for a large number of devices in a relatively small area. Dummy transistors are placed around all rows to achieve smooth transition of layout patterns between device rows with different drawn dimensions and thus, eliminate any variations introduced by abrupt layout pattern changes at row boundaries. *Intrinsic linear* V_T, which is free of impacts from (1) parasitic source-drain and metal resistances and (2) vertical field induced mobility degradation in the inversion layer (unlike the traditional peak-gm V_T), and (3) asymmetry of source/drain doping (unlike saturation V_T), is extracted for each device at different body bias values from the measured I-V data (Fig.

3). Intrinsic V_T is ~100mV higher than the peak-gm V_T for a typical device. This extraction is performed self-consistently with electrical channel length to width ratio (Le/We) and effective parasitic resistance (Ri), using a new algorithm (Fig. 4) that also accounts for extraction difficulties introduced by halo doping. I-V measurements on large square (1.5μm) devices across different body bias values are used to extract the required low-field channel mobility values.

3. Extrinsic and Intrinsic V_T Fluctuations

Statistical analysis for σV_T computation is performed on the measured data using "order statistics" and "robust σ"-based outlier filtering to eliminate defective transistors and those impacted by strains generated by pressure under the probe pads during measurements. Components of extrinsic variations in linear V_T due to (1) distance-dependent process variations (baseline), (2) length variations (caused by short-channel effects or SCE) and (3) width variations (caused by narrow-width effects or NWE) are extracted out from the total measured σV_T for each row of identically drawn devices. Remainder of the variations is intrinsic in nature. As shown in Fig. 5, while baseline variations represent 10-17% of the total in large square devices, SCE and NWE contribute to 18-60% of variations in small target devices. The remaining intrinsic variations constitute 20-90% of the total across the four device types. These intrinsic variations, measured as both σV_T and $\sigma V_T/V_{Tmean}$, show significant deviation from the conventional $1/\sqrt{(We*Le)}$ behavior [2-4] for both NMOS & PMOS, especially for small devices, across different body bias values (Figs. 6 & 7). For these devices, intrinsic σV_T increases from 13mV to 14mV for NMOS and from 10mV to 13mV for PMOS with 0.5V reverse body bias (RBB), while the $\sigma V_T/V_{Tmean}$ remains unchanged at a maximum of 3% for both NMOS and PMOS. Thus, percentage variation of drain current due to intrinsic V_T fluctuations worsens with RBB.

Dependence of these intrinsic V_T fluctuations on We, Le and We*Le (area) are modeled for different body bias values by using a minimum-AIC regression method, so as to produce the best fit to data without modeling data noise. The models are shown to fit well to the data across a large range of device dimensions and body bias (Figs. 8 & 9). Although the intrinsic V_T fluctuations have a large amount of area-dependent component, as expected from random dopant fluctuations [2-4], 20-60% of the variations depend only on width or length in narrow, short and small target devices (Fig. 10), in spite of the fact that components due to SCE and NWE have been removed. However, comparisons of the σ of V_T mismatch (ΔV_T) of neighboring devices in an ensemble to the σV_T of these same devices demonstrate that these intrinsic fluctuations, including components not dependent on area, are *random* across the entire range of device dimensions and body bias values, for both NMOS and PMOS (Figs. 11 & 12).

4. Conclusions

Fluctuations in intrinsic linear V_T, free of impact of parasitics, are measured for large arrays of NMOS and PMOS devices in a small area on a testchip in a 150nm logic technology. Extrinsic components of V_T variations due to process, length and width variations are extracted out to obtain the local intrinsic fluctuations. We show that the intrinsic σV_T is random, and worsens with reverse body bias (RBB). Although the traditional area-dependent component is dominant, there exist significant intrinsic fluctuation components in small devices that depend only on device width or length, even though variations due to short-channel and narrow-width effects have been extracted out.

5. Acknowledgments

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6. References

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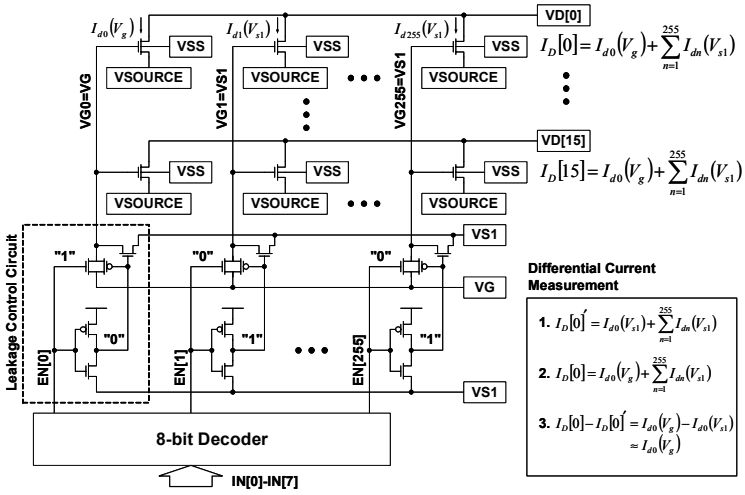
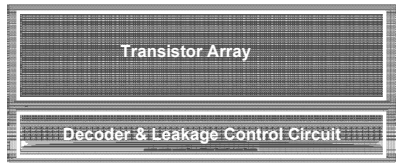


Figure 1 Single array circuit schematics with under-drive leakage control circuitry and body bias transistor hooks. Array contains independent transistor drain row lines while decoder select the gate column line.



W (um)	0.3	0.3	0.34	0.34	0.5	1.2
L (um)	0.16	0.2	0.16	0.2	0.24	0.24

Transistor	W (um)	L (um)
Square	1.5	1.5
Narrow	W	1.5
Short (Wide)	1.5	L
Traget (Small)	W	L

Figure 2 Chip micrograph of the array and transistor sizes both for multiple transistor arrays and in a single array.

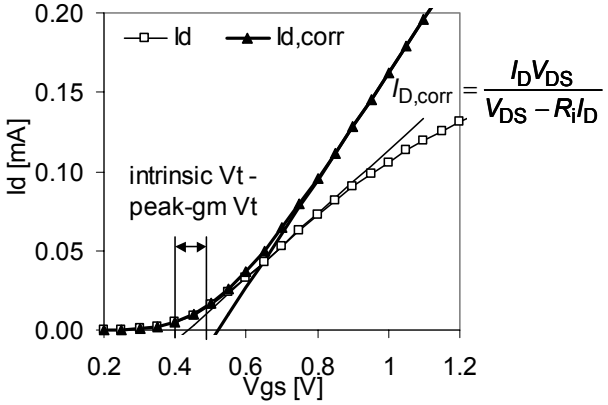


Figure 3 Intrinsic V_T extraction considering roles of series resistance and weak inversion.

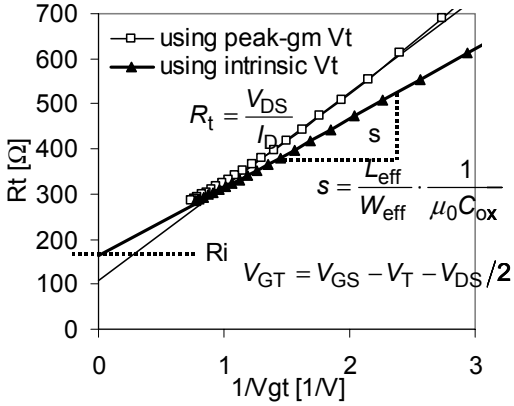


Figure 4 Extractions of intercept resistance R_i .

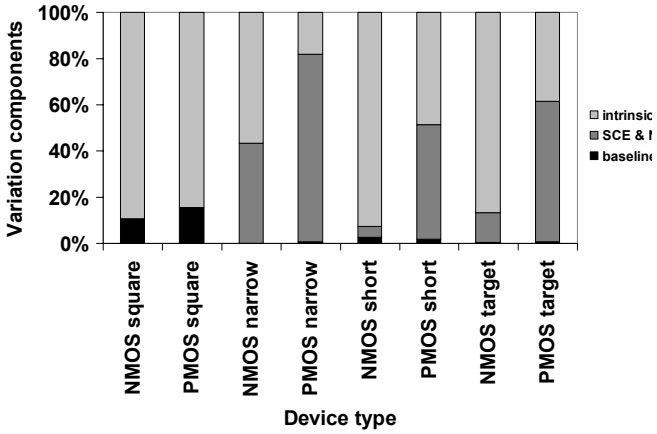


Figure 5 Contribution of baseline, SCE, NWE, and intrinsic components to threshold variation of NMOS and PMOS transistors.

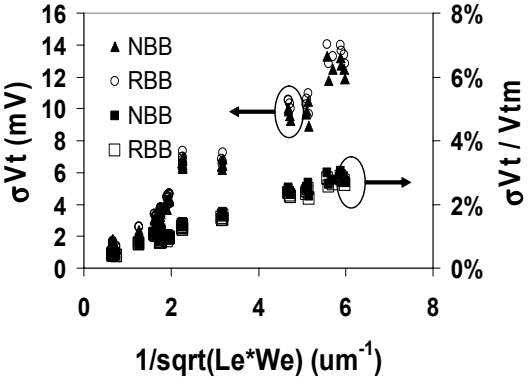


Figure 6 NMOS threshold variations (both sigma and sigma over mean) as a function of transistor area with respect to body bias i.e. for no body bias (NBB) and 0.5V reverse body bias (RBB).

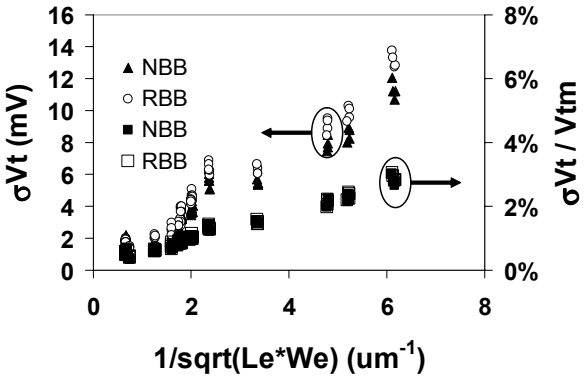


Figure 7 PMOS threshold variations (both sigma and sigma over mean) as a function of transistor area with respect to body bias i.e. for no body bias (NBB) and 0.5V reverse body bias (RBB).

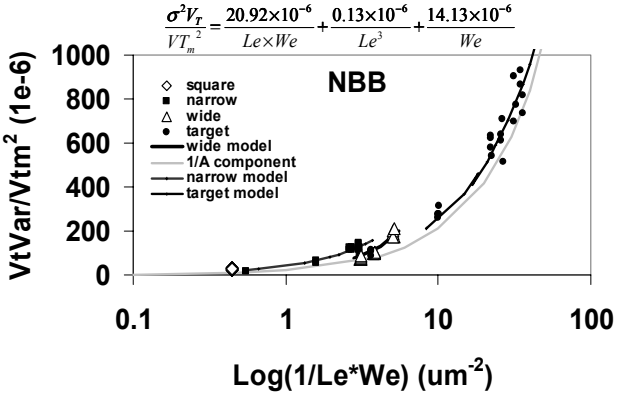


Figure 8 Actual data and model of NMOS threshold voltage variance over mean squared of threshold voltage as a function of transistor area for no body bias.

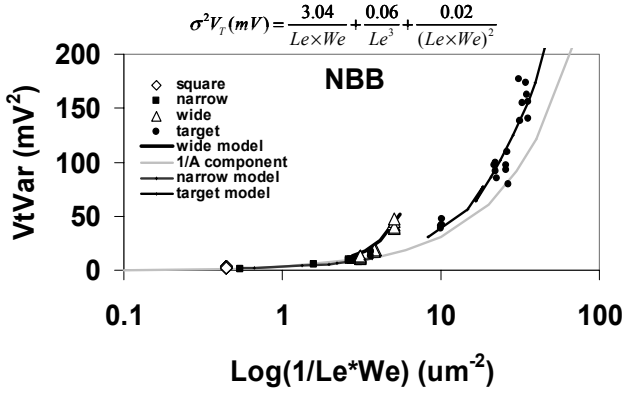


Figure 9 Actual data and model of NMOS threshold voltage variance as a function of transistor area for no body bias.

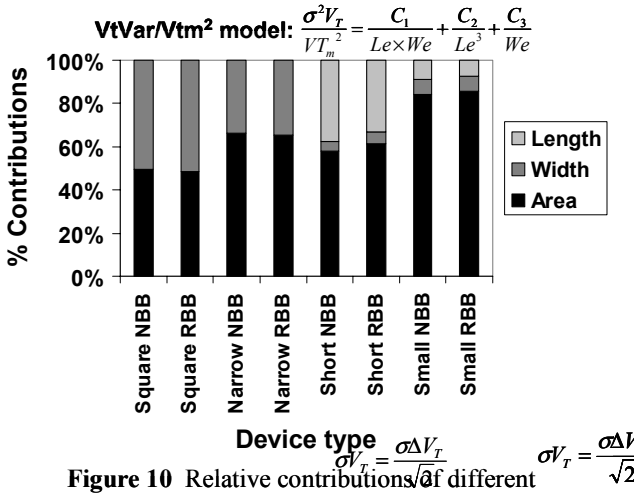


Figure 10 Relative contributions of different components of threshold voltage variance over square of mean threshold voltage model for different transistor sizes as a function of body bias.

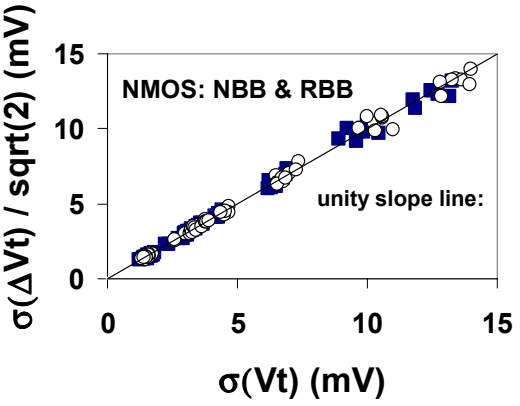


Figure 11 Sigma of threshold voltage mismatch of the neighboring NMOS devices versus sigma of the threshold of the same devices suggests intrinsic variations are random for NBB & RBB.

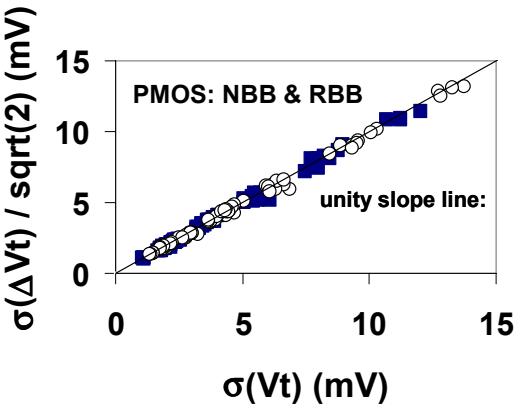


Figure 12 Sigma of threshold voltage mismatch of the neighboring PMOS devices versus sigma of the threshold of the same devices suggests intrinsic variations are random for NBB & RBB.