FinFET-Based SRAM Design

Zheng Guo, Sriram Balasubramanian, Radu Zlatanovici, Tsu-Jae King, Borivoje Nikolić
Department of Electrical Engineering and Computer Sciences,
University of California, Berkeley, CA 94720, USA

{zhengguo,bsriram,zradu,tking,bora}@eecs.berkeley.edu

ABSTRACT
Intrinsic variations and challenging leakage control in today's bulk-Si MOSFETs limit the scaling of SRAM. Design tradeoffs in six-transistor (6-T) and four-transistor (4-T) SRAM cells are presented in this work. It is found that 6-T and 4-T FinFET-based SRAM cells designed with built-in feedback achieve significant improvements in the cell static noise margin (SNM) without area penalty. Up to 2x improvement in SNM can be achieved in 6-T FinFET-based SRAM cells. A 4-T FinFET-based SRAM cell with built-in feedback can achieve sub-100pA per-cell standby current and offer the similar improvements in SNM as the 6-T cell with feedback, making them attractive for low-power, low-voltage applications.

Categories and Subject Descriptors
B.3.1 [**Memory Structures**]: Semiconductor Memories – *Static memory (SRAM)*; B.7.1 [**Integrated Circuits**]: Types and Design Styles – *Advanced Technologies, Memory Technologies*

General Terms: Design

Keywords: Memory, SRAM, low power, double gate transistors.

1. INTRODUCTION
SRAM arrays occupy a large fraction of the chip area in many of today's designs. As memory will continue to consume a large fraction of many future designs, scaling of memory density must continue to track the scaling trends of logic. Increased transistor leakage and parameter variation present challenges for scaling of conventional six-transistor (6-T) SRAM cells. As MOSFETs are scaled down to the nanoscale regime, statistical dopant fluctuations, oxide thickness variations, and line-edge roughness increase the spread in transistor threshold voltage (V_t) and thus the on- and off- currents. In order to limit static power dissipation in large caches, lower supply voltage can be used [1]; however, a low supply voltage coupled with large transistor variability compromises cell stability, measured as the static noise margin [2].

The FinFET transistor structure has been developed as an alternative to the bulk-Si MOSFET structure for improved scalability [3]. It utilizes a Si fin (rather than a planar Si surface) as the channel/body; the gate electrode straddles the fin. The fin width is the effective body thickness, and the fin height is the effective channel width. In the on state, current flows between the source and drain along the gated sidewall surfaces of the Si fin. Short-channel effects (SCE) are suppressed by utilizing a thin body, *i.e.* by making the fin very narrow, less than the channel length. Heavy channel doping is not required for SCE control and hence can be eliminated to minimize variations due to statistical dopant fluctuation effects. The gates on either side of the fin can be electrically isolated to allow for independent operation, by selectively removing the gate material in the region directly on top of the fin [4]. In double-gate (DG) operating mode the two gates are biased together to switch the FinFET on/off, whereas in back-gate (BG) operating mode they are biased independently – with one gate used to switch the FinFET on/off and the other gate used to adjust the threshold voltage V_t. BG operation offers dynamic performance tunability which can be leveraged to improve tradeoffs in SRAM design. We first analyze the design constraints and tradeoffs for a conventional 6-T SRAM cell, and show how its design can be optimized to meet noise margin and power specifications. Challenges for bulk-Si SRAM technology scaling are then discussed, and FinFET-based SRAM cell designs are presented. It is shown that built-in feedback can be used to achieve dramatic improvements in the cell read margin, while providing very low standby power consumption.

ISLPED'05, August 8–10, 2005, San Diego, California, USA.

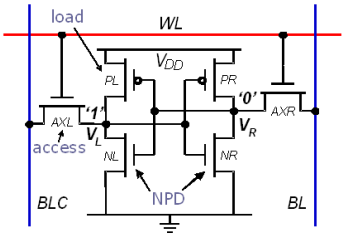

Figure 1. Schematic of a conventional 6-T SRAM cell.

2. 6-T SRAM DESIGN TRADEOFFS
2.1 Area vs. Yield
The functionality and density of a memory array are its most important properties. Functionality is guaranteed for large memory arrays by providing sufficiently large design margins, which are determined by device sizing (channel widths and lengths), the supply voltage and, marginally, by the selection of transistor threshold voltages. Although upsizing the transistors increases the noise margins, it increases the cell area and thus lowers the density.

2.1.1 Hold Margin
In standby mode, the PMOS load transistor (PL) must be strong enough to compensate for the sub-threshold and gate leakage currents of all the NMOS transistors connected to the storage node V_L (Figure 1). This is becoming more of a concern due to the dramatic increase in gate leakage and degradation in I_{ON}/I_{OFF} ratio in recent technology nodes [5]. Coupled with the recent trend [6] to decrease the cell supply voltage during standby to reduce static power consumption, this makes it increasingly more difficult to design robust low-power memory arrays.

Hold stability is commonly quantified by the cell static noise margin (SNM) in standby mode. The SNM of an SRAM cell represents the minimum DC-voltage disturbance necessary to upset the cell state [2], and can be quantified by the length of the side of the maximum square that can fit inside the butterfly curves formed by the cross-coupled inverters.

2.1.2 Read Stability Margin

During a read operation, V_R rises above 0V, to a voltage determined by the resistive voltage divider set up by the access transistor (AXR) and the pull-down transistor (NR) between BL and node V_R (Figure 1). The ratio of the width/length of NR to AXR determines how high V_R will rise and is commonly referred to as the cell β-ratio. If V_R exceeds the trip point of the inverter formed by PL and NL, the cell bit will flip during the read operation, causing a read upset.

Read stability can also be quantified by the cell SNM during a read access. Since AXR operates in parallel to PR and keeps V_R from ever reaching 0V, the gain in the inverter transfer characteristic will decrease [7], causing a reduction in the separation between the butterfly curves and thus in SNM. For this reason, the cell is considered most vulnerable to noise during the read access. The read margin can be increased by upsizing the pull-down transistor, which results in an area penalty and/or increasing the gate length of the access transistor, which increases the WL delay and hurts the write margin.

2.1.3 Write Margin

During a write operation, AXL and PL form a resistive voltage divider between the low-going BLC and node V_L (Figure 1). If the voltage divider pulls V_L below the trip point of the inverter formed by PR and NR, a successful write operation occurs. The write margin can be measured as the maximum BLC voltage that is able to flip the cell state while BL is kept high. The write margin can be improved by keeping the pull-up device minimum sized and upsizing the access transistor W/L at the cost of cell area and the cell read margin.

2.1.4 Access Time

During any read/write access, the WL is raised only for a limited amount of time specified by the cell access time. If either the read or the write operation can not be successfully carried out before the WL is lowered, access failure occurs.

A successful write access occurs when the voltage divider is able to pull V_L below the inverter trip point, after which the positive feedback in the cross-coupled inverters will cause the cell state to flip almost instantaneously.

For the precharged bit-line architecture which employs voltage sensing amplifiers, a successful read access occurs if the pre-specified ΔV (required by the sense amplifier) between the bit-lines can be developed before the WL is discharged [8].

2.2 Power

Large embedded SRAM arrays consume a significant portion of the overall power of an application processor. Power consumption in an SRAM array consists of short active periods and very long idle periods. For large arrays, standby power consumption is a major issue. Therefore, leakage reduction in large memory arrays has become essential for low-power VLSI applications. Cell leakage is commonly suppressed by either using longer channel lengths or higher transistor threshold voltages. Using longer channel lengths negatively impacts the cell area. In addition, the use of longer channel lengths tends to increase WL and BL capacitances, thus increasing access time and active power. Therefore, longer channel lengths are used sparingly (for example on the access transistors, which improves cell stability as well).

Utilizing higher transistor threshold voltages also negatively impacts the access time due to the lower read current. However, they help to improve the read and write margins. While high threshold PMOS loads decrease the inverter trip point, high threshold NMOS pull-down devices (NPD) tend to increase it. Since the current driving ability of the NPD is larger than that of the PMOS load, increasing the threshold voltage of the NMOS transistors tends to have a stronger impact on the trip voltage [9], thus resulting in larger read and write margins. Typically, the maximum standby power of the memory array sets a lower limit (e.g. 0.4-0.5V) for the V_t in a given process. Then the margins are maintained by setting the supply voltage sufficiently high.

There are circuit techniques to reduce memory leakage as well: using sleep transistors and body biasing. However, these reduce density and compromise stability.

2.3 Challenges for Scaling Bulk-Si SRAM

While it is possible to scale the classical bulk-Si MOSFET structure down into the sub-20nm regime, SCE control requires heavy channel doping ($>10^{18}$ cm^{-3}) and heavy super-halo implants to control sub-surface leakage currents. As a result, carrier mobilities are severely degraded due to impurity scattering and a high transverse electric field in the on state. Furthermore, the increased depletion charge density results in a larger depletion capacitance hence a larger sub-threshold slope. Thus, for a given off-state leakage current specification, on-state drive current is degraded. Off-state leakage current is enhanced due to band-to-band tunneling between the body and drain. V_t variability caused by random dopant fluctuations is another concern for nanoscale bulk-Si MOSFETs.

Control of critical dimensions does not track their scaling, thus the ratio of the standard deviation over the average increases. Designing large arrays requires design for 5 or more standard deviations. With increasing variations, it becomes difficult to guarantee near-minimum-sized cell stability for large arrays in embedded, low-power applications. Increasing transistor sizes, on the other hand, is counter to the fundamental reason for scaling in the first place – to increase density. Access time is dependent on wire delays and column height. To speed up arrays, segmentation is commonly employed. With further reductions in bit-line height, the overhead area of sense amplifiers becomes substantial.

2.4 SRAM Cell Layout

Conventional SRAM cells [10] have relatively high aspect ratios (AR) – the ratio of BL-parallel height to BL-orthogonal width. Recently, SRAM cells have been designed with a much smaller AR to allow for straight poly-Si gate lines and active regions. This cell design allows for very precise critical-dimension control, thereby reducing gate-length variations and corner-rounding issues as well as relaxing back-end design rules, making it highly manufacturable [10-12]. Shorter cells along with the more relaxed metal pitch in this design result in a significant reduction in BL capacitance. The accompanying increase in the WL capacitance can be combated by WL segmentation.

3. FINFET DESIGN FOR SRAM

SCE can be effectively suppressed by using a thin-body transistor structure such as the FinFET, which allows for gate-length scaling down to the 10-nm regime [3-4] without the use of heavy channel/body doping. A lightly doped channel gives rise to lower transverse electric field in the on state and negligible impurity scattering, hence higher carrier mobilities. It also allows FinFET devices to have negligible depletion charge and capacitance, which yields a steep sub-threshold slope. In addition, FinFETs have lower parasitic device capacitance because both depletion and junction capacitances are effectively eliminated, which reduces the BL capacitive load. Finally, the elimination of heavy doping in the channel minimizes V_t variations due to statistical dopant fluctuation effects. Therefore, FinFET-based SRAM cells are expected to show enhanced performance over bulk-Si MOSFET SRAM cells.

4. FinFET Design and Modeling

Mixed-mode device simulation using the drift-diffusion model for carrier transport and the density gradient model to account for

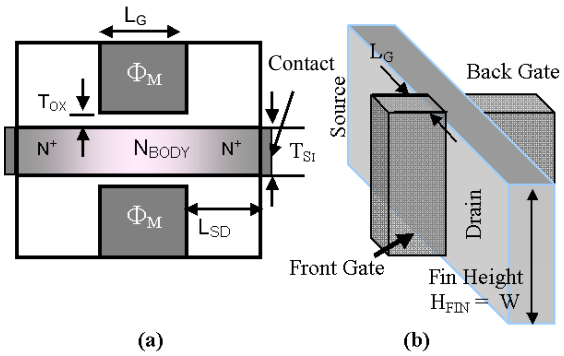

Figure 2. (a) Cross-sectional schematic of double-gate MOSFET structure. (b) The gates of the FinFET can swing together in double-gated operation or can swing independently in back-gated operation.

quantum-mechanical effects in nanoscale MOSFETs is employed to simulate the DC transfer characteristics of SRAM cells under different biasing conditions [13]. Because the high-field transient velocity overshoot effects are ignored, the drain current values may be underestimated. However, the trends and differences between device technologies and their impact on SRAM noise margins should still be valid because they depend on the relative strengths of two transistors and not their absolute I_{ON}. On the other hand, the error in estimating the I_{ON} together with unknown interconnect properties make access time simulations unreliable and they were therefore not performed.

It is expected that the effect of parasitic resistances and capacitances will limit circuit performance in deeply scaled CMOS technologies. Series resistance and extrinsic contact resistance are included in this work, which lessens the improvements associated with the intrinsic device structure. With the control of short-channel effects in bulk devices becoming increasingly difficult at shorter gate lengths, FinFET devices have increasing performance improvements over bulk-Si MOSFETs with technology scaling.

The transistor structures used in this study are shown in Figure 2 and the key design parameters are summarized in Table 1. FinFETs fabricated on a standard (100) wafer have channels on the fin sidewalls that are oriented along (110) planes, for standard layouts. To capture the effect of fin-sidewall surface orientation on FinFET performance, the carrier mobilities in Taurus [13] are calibrated using experimental data for the (110) surface [14].

4.1 FinFET SRAM Cell Designs

4.1.1 Conventional Double-Gated (DG) Designs

The read margin can be improved by increasing the strength of the pull-down transistor relative to the access transistor, either by increasing the size-ratio between NR and AXR (Figure 1) or

Table 1. Device parameters used for Taurus simulations.

Parameters	FinFET	Bulk-Si
L_G (nm)	22	22
L_{SD} (nm)	24	24
T_{ox} (Å)	11	11
T_{Si} (nm)	15	-
V_{DD} (V)	1.0	1.0
Channel Doping, N_{BODY} (cm^{-3})	10^{16}	$4x10^{18}$
H_{FIN} (nm)	30	-
S/D doping gradient (nm/dec)	4	4

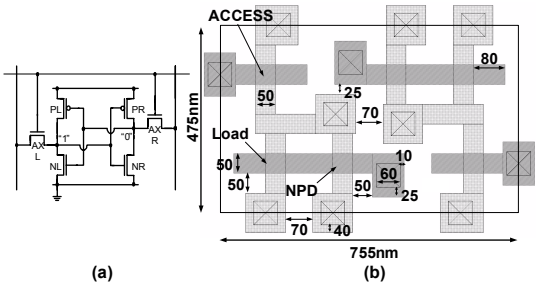

Figure 3. Circuit schematic (a) and layout (b) for a conventional DG 6-T SRAM cell. The outline indicates the area of one memory cell.

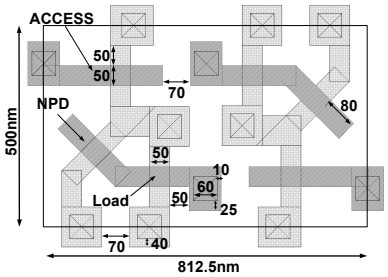

Figure 4. DG 6-T SRAM cell layout with rotated (100) NPD.

enhancing carrier mobility in the pull-down devices. The conventional double-gated (DG) design is first investigated; its schematic and layout are shown in Figure 3. The dashed outline indicates the memory cell boundary. The layout was generated using a linearly scaled version of 90nm node logic design rules.

Electron mobility along (100) planes is higher than along (110). In order to increase the effective cell β-ratio and thus improve the cell read margin, the NMOS pull-down devices (NPD) were rotated to have channel surface along the (100) plane. Unlike cell designs in planar bulk-CMOS, FinFET-based SRAM cells containing transistors with channel surface both along (110) and (100) planes can be easily fabricated by simply rotating the fins by 45° for the (100) fins (Figure 4). As a tradeoff, printing rotated fins may be lithographically more challenging and may result in enhanced process variations.

Greater improvements in read margin can be obtained by upsizing the pull-down transistor (Figure 5) or increasing the length of AXR. Since the channel widths of FinFET devices are determined by the number of fins, only discrete sizing is available [15]. Increasing the access device length has less impact on cell area but increases the WL capacitance and also negatively impacts the read current, resulting in slower access time.

Figure 6 plots the butterfly curves for both the 6-T bulk-Si MOSFET-based SRAM cell and the 6-T FinFET-based SRAM cell (simulated using device parameters from Table 1). As shown, the conventional DG 6-T FinFET-based SRAM with 1-fin achieves a 22% improvement in the read SNM compared to its bulk-Si-based counterpart with β-ratio of 1.5. Moreover, a 15% further improvement in the read SNM, with a 13.3% area penalty, can be achieved by rotating the pull-down transistor; a 36% further improvement in the read SNM, with 16.6% area penalty, can be achieved by upsizing the pull-down transistor by 1-fin. Higher threshold pull-down devices were then used in the FinFET designs, by raising the gate work function of the NMOS and PMOS devices (both to 4.75eV), to suppress leakage and to improve read/write margin. Using a common gate work function also improves manufacturability. The resulting improvements in SNM are shown in Figure 6c. A higher V_t bulk-Si device might not translate to lower leakage due to band-to-band tunneling.

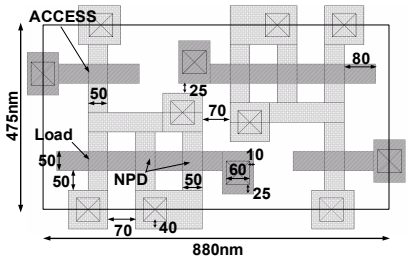

Figure 5. 6-T SRAM cell layout with 2-fin pull-down FETs

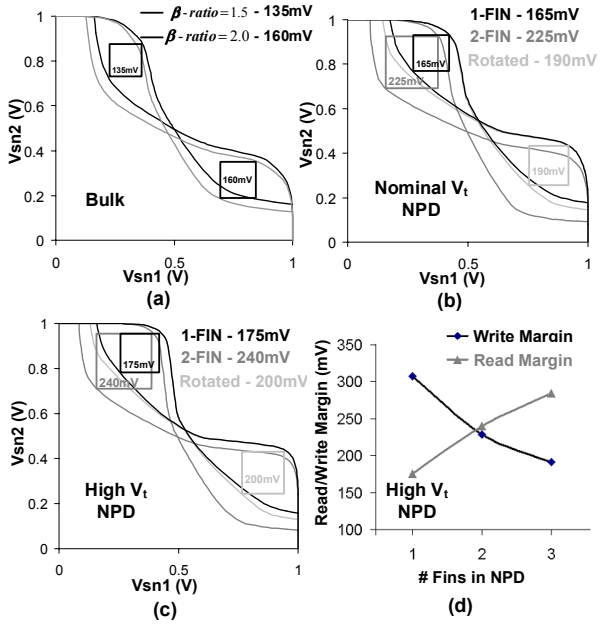

Figure 6. 6-T SRAM read butterfly plots (a) bulk-Si MOSFET SRAM cell with β-ratio = 1.5 (black), 2.0 (gray) and (b-c) FinFET-based SRAM cell with 1-fin (black), 2-fins (dark gray), and rotation (light gray). (d) Impact of adding fins to the NPD on the read- and write-margins.

Whenever the pull-down devices are strengthened, either by adding fins or by rotating the channel surface plane, the cell write margin shrinks – primarily due to the reduction in the write trip voltage. The effects of inserting extra fins on the read and write noise margins are summarized in Figure 6d.

4.1.2 Back-Gated (BG)Designs

Whereas adaptive body biasing becomes less effective with bulk-Si MOSFET scaling [16], back-gate biasing of a thin-body MOSFET remains effective for dynamic control of V_t with transistor scaling, and can provide improved control of short-channel effects as well [17]. The strong back-gate biasing effect can thus be leveraged [18] to optimize the performance of FinFET-based SRAMs through a dynamic adjustment of the effective cell β-ratio.

By connecting the storage node to the back-gate of the access transistor, as shown in Figure 7, the strength of the access transistor can be selectively decreased. For example, if the stored bit is a "0", the back-gate of the corresponding access transistor is biased at 0V, decreasing its strength. This effectively increases the β-ratio during the read cycle and thus improves the read margin. Although the BG access transistor has weaker current driving strength compared to the DG access transistor, the "0" storage node in the 6-T design with feedback stays closer to V_{SS} than the conventional DG design (Figure 8a); thus giving the BG

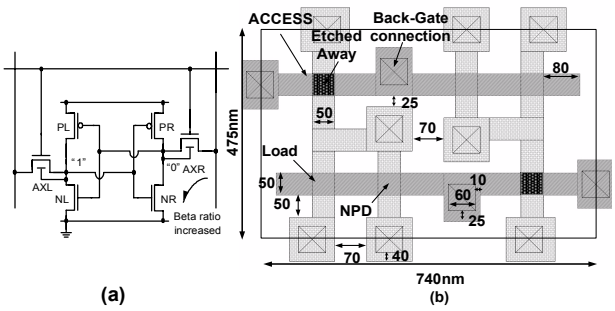

Figure 7. Circuit schematic (a) and layout (b) for a 6-T SRAM cell with back-gate connections to provide dynamic feedback. Note the use of BG-FinFET NMOS access devices involves gate separation as indicated in the layout by a dark layer over their gate electrode.

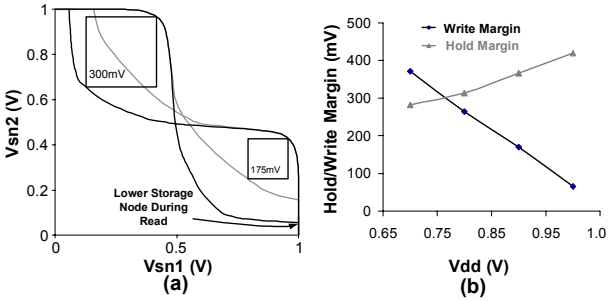

Figure 8. (a) Read SNM plot for a FinFET 6-T cell with feedback. (b) Impact of cell supply on write margin and standby SNM. Approximately 300mV of write margin and standby SNM can be achieved with a cell bias of 0.8V.

access transistors in the 6-T design with feedback more gate overdrive. Therefore, only a small performance hit is incurred by introducing the feedback. A 71% read margin improvement over the DG design is achieved (Figure 8a).

Moreover, this simple back-gate connection incurs no area penalty over the conventional DG 6-T SRAM cell design. The cell area is actually reduced by 2% due to the disappearance of the 80nm gate-poly extension over active (fin) that the DG access device required (Figure 7b).

The main drawback of the 6-T SRAM design with feedback is the reduced write margin because of the reduction in the driving current of the BG access transistor at the '1' storage node as it is pulled low. This can be combated, without major impact on read SNM, by adjusting the strength of the PMOS load devices. The PMOS load devices can be made weaker by either adjusting their threshold voltage or gate length. However, both techniques will only yield a marginal improvement in the write margin. A much more significant improvement in the write margin can be attained by lowering the cell supply voltage during write [19]. This is made possible by adopting the long AR cell layout, since the cell supply can be routed vertically for each column and can be exploited to break the contention between read and write optimization. With the ability for column based biasing, cell supply voltage can be selectively lowered only for the column containing the cell under write access. This keeps the cell stability high for all other cells connected to the same WL. Thus, high read- and write-margins can be independently achieved. Essentially, the contention between read- and write-margins has been replaced by a contention between hold- and write-margins, which offers a much bigger window for optimization. Figure 8b summarizes the enhancement in write margin due to reduced cell supply and the corresponding impact on the hold SNM.

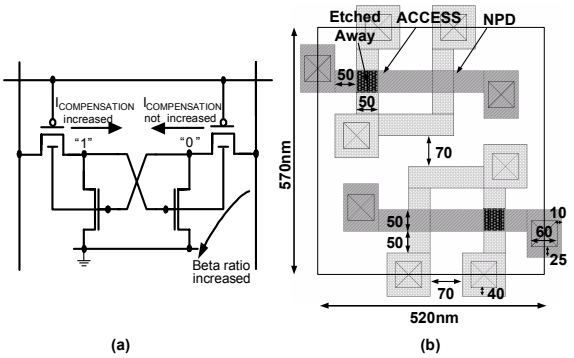

Figure 9. Circuit schematic (a) and layout (b) for a 4-T SRAM cell with back-gate connections to provide dynamic feedback. Note the use of BG-FinFET PMOS access devices, indicated in the layout by a dark layer over their gate electrodes.

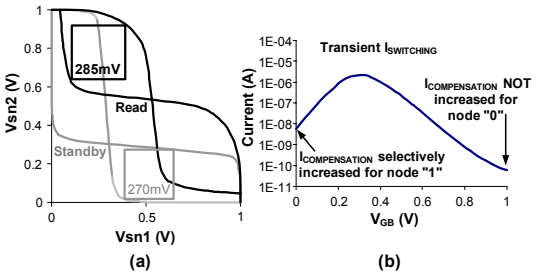

Figure 10. (a) SNM plot for a 4-T cell with feedback during standby (gray) and read (black). (b) Using dynamic feedback, $I_{COMPENSATION}$ is selectively increased to compensate "1" storage node.

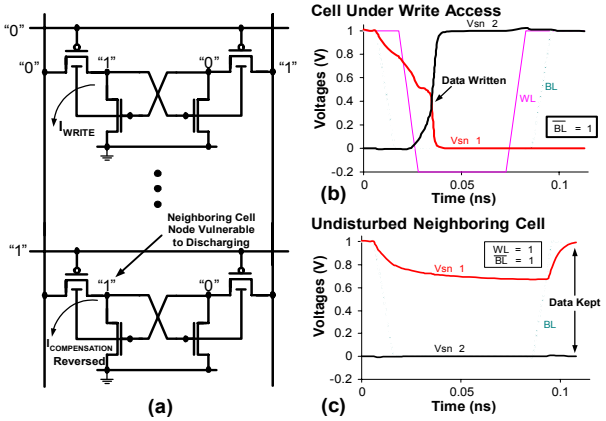

Figure 11. (a) 4-T SRAM neighboring cell write upset set-up. (b) write simulation with word line swing of –200mV to 1 V. (c) write simulation of undisturbed neighboring cell.

4.1.3 4-T Cell Design with Dynamic Feedback

To seek further reduction in cell area, 4-T SRAM designs were investigated. In conventional 4-T SRAM cell designs [18], high-leakage PMOS access transistors are used to compensate for the leakage currents in the pull-down transistors during standby. Although compensation current is only needed for the "1" storage node, both PMOS access transistors draw currents from the bit-lines, resulting in high power dissipation. Dynamic control of the PMOS threshold voltage (Vtp) offers a means for selectively adjusting the compensation leakage current [18], and also provides higher effective β-ratio for the 4-T SRAM cell design.

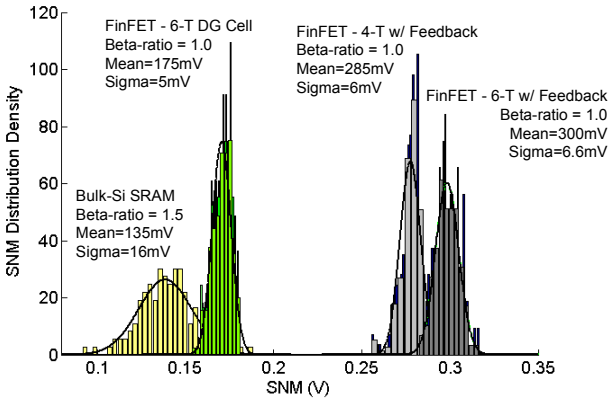

Figure 12. Impact of process variations on SNM. Cell designs with dynamic feedback have improved noise margin than the standard 6-T DG-SRAM. Dopant induced fluctuations cause larger SNM spreads in the bulk devices.

By cross-coupling the storage node to the back-gate of the access transistor on the opposite side, as shown in Figure 9, high compensation current can be selectively injected only into the "1" storage node as seen in Figure 10b. In addition, the β-ratio is increased because the access transistor connected to the "0" storage node is made weaker with its back-gate biased by the "1" storage node. (Note that a "1" back-gate bias lowers the PMOS drive current.) The resulting improvement in read margin is shown in Figure 10a. Compared to the conventional DG 6-T design presented earlier, the 4-T design with feedback achieves a 63% improvement in read margin on top of a 17.4% area savings.

An issue for the conventional 4-T SRAM cell design is the possibility of a bit-flip while a neighboring cell (sharing the same bit-line) is being written: when the bit-lines are set according to the data to be written, the directions of the compensation currents can be reversed in the cells connected to the same bit-lines, potentially flipping those cells and causing a neighboring cell write upset (Figure 11a). This issue can be addressed by noting that the PMOS devices can only pull a "1" storage node down to $|V_{tp}|$; thus, the state of the cell is not flipped if $|V_{tp}|$ is higher than the NMOS threshold voltage, V_{tn}. If this is the case, the storage node voltages will be restored when the bit-lines are recharged after a successful write operation. Since dynamic compensation is employed, high leakage, low-V_{tp}, PMOS access devices are not needed for standby stability. Therefore, neighboring cell write upset can be alleviated by employing high-V_{tp} PMOS and low-V_{tn} NMOS devices (Figure 11b,c). Since high-V_{tp} PMOS devices tend to be relatively weak, PMOS drive current should be increased to improve the write margin. This can be done by using a negative word-line bias voltage.

4.1.4 Process-Induced Variations

Process-induced variations in device parameters cause V_t variations resulting in spread in SRAM SNM distributions. In order to examine the impact of fluctuations in device parameters such as L_G and T_{Si} in FinFETs ($3\sigma L_G = 3\sigma T_{Si} = 10\%\ L_G$) and the impact of random dopant fluctuations in bulk devices [20]. Monte Carlo simulations of SRAM cells were run using mixed-mode simulation in Taurus. The impact of statistical variations in device parameters in FinFETs and bulk devices on the cell read margin is illustrated in Figure 12.

4.2 Array Design Issues

4.2.1 Sleep-mode features

Due to the requirement for low V_{tn} to alleviate neighboring cell write upsets in the 4-T SRAM designs, leakage reduction is

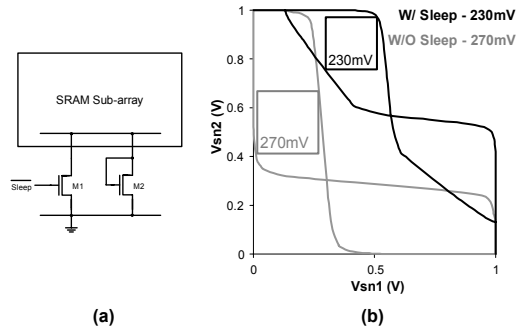

Figure 13. (a) Gated V_{SS} leakage reduction scheme for the 4-T SRAM design. (b) Standby SNM plots for the 4-T SRAM cell with and without gated V_{SS} leakage reduction.

needed to suppress the high standby current. NMOS sleep transistors can be integrated into each sub-array, as shown in Figure 13a, and are turned on/off based on the mode of operation (standby or active). During standby, M1 is turned off and the gated V_{SS} is boosted by the V_{tn} of the diode-connected M2. Figure 13b shows the impact of this leakage reduction scheme on the standby SNM. It is observed that the sleep transistors do incur a small – less than 15% degradation – in the cell standby SNM. The simulated cell standby currents for the 4-T and the 6-T FinFET-based designs are summarized in Table 2. The FinFET cell design is smaller than the one in bulk, because it can do away with the n-well to p-well spacing, and in addition does not need four contacts inside the cell. 6-T FinFET-based SRAM cells, can achieve less than 0.2nA/cell of standby current just by using high Vt devices and the leakage of 4-T FinFET-based SRAM cell can be kept under 80pA/cell by utilizing sleep transistors, while sustaining a 230mV standby SNM.

5. CONCLUSION

6-T and 4-T FinFET-based SRAM cells were analyzed using mixed-mode Taurus simulations. The SNM performance of the FinFET-based SRAM cells were compared to SRAM cells designed in planar bulk-Si MOSFETs. Conventional FinFET-based 6-T DG designs with high V_t provide a read SNM of 175mV – a 30% improvement over that of the bulk-Si MOSFET SRAM cell (β-ratio of 1.5). The cell SNM can be further improved by 71% at little performance and no area penalty through utilizing built-in feedback to dynamically adjust transistor strengths – achieving 300mV SNM, while keeping standby leakage current below 0.2nA/cell. 4-T FinFET-based SRAM cell with built-in feedback can achieve more than 17% area reduction with 285mV SNM during read and 230mV SNM during standby, while providing less than 80pA/cell of leakage current during standby – making it extremely attractive for high-density, low-power cache memory applications.

6. REFERENCES

[1] J. Wuu, D. Weiss, C.Morganti, and M. Dreesen. The Asynchronous 24MB On-chip Level-3 Cache for a Dual-Core Itanium-Family Processor. *ISSCC*, 2005, 488-89.

[2] E. Seevinck, F. J. List and J. Lohstoh. Static-Noise Margin Analysis of MOS SRAM Cells. *JSSC,* 1987, 366-77.

[3] X. Huang et al. Sub-50nm P-Channel FinFET*, IEDM Tech. Dig.,* 1999, 67-70.

[4] L. Mathew et al. CMOS Vertical Multiple Independent Gate Field Effect Transistor (MIGFET). *IEEE SOI Conf. Dig.*, 2004, 187.

[5] H. Pilo. *SRAM Design in the Nanoscale Era. ISSCC*, 2005.

[6] H. Qin, Y. Cao, D. Markovic, A. Vladimirescu and J. Rabaey. SRAM Leakage Suppression by Minimizing Standby Supply Voltage. *ISQED*, 2004.

[7] A. J. Bhavnagarwala, X. Tang and J. Meindl. The Impact of Intrinsic Device Fluctuations on CMOS SRAM Cell Stability. *JSSC*, 2001, 658-665.

[8] S. Mukhopadhyay, H. Mahmoodi and K. Roy. Modeling and Estimation of Failure Probability due to Parameter Variations in Nano-scale SRAMs for Yield Enhancement. *Symp. VLSI Circuits Dig.*, 2004, 64-7.

[9] R.V. Joshi et al. FinFET SRAM for High-Performance Low-Power Applications. *ESSCIRC*, 2004, 211-4.

[10] K. Zhang et al. A Fully Synchronized, Pipelined, and Re-Configurable 50Mb SRAM on 90nm CMOS Technology for Logic Applications. *Symp. VLSI Circuits Dig.*, 2003, 253.

[11] T. Devoivre et al. Validated 90nm CMOS Technology Platform with Low-k Copper Interconnects for Advanced System-on-Chip (SoC). *MTDT,* 2002, 157-62.

[12] M. Ishida et al. A Novel 6T-SRAM Cell Technology Designed With Rectangular Patterns Scalable Beyond 0.18μm Generation and Desirable for Ultra High Speed Operation. *IEDM Tech. Dig.*, 1998, 201-4.

[13] Taurus v.2003.12, Synopsys, Inc.

[14] M. Yang et al. Performance Dependence of CMOS on Silicon Substrate Orientation for Ultrathin Oxynitride and HfO_2 Gate Dielectrics. *IEEE EDL*, Vol. 24 (5), 2004, 339

[15] E. J. Nowak et al. A Functional FinFET-DGCMOS SRAM Cell. *IEDM Tech. Dig.,* 2002, 411-14

[16] A. Keshavarzi et al. Leakage and Process Variation Effects in Current Testing on Future CMOS Circuits. *IEEE Design & Test of Computers*, Vol. 19, Issue 5, 2002, 33.

[17] M. Ieong et al. Experimental Evaluation of Carrier Transport and Device Design for Planar Symmetric/Asymmetric Double-Gate/Ground-Plane CMOSFETs,*IEDM*, 2001, 19.6.1

[18] M. Yamaoka et al. Low Power SRAM Menu for SOC Application Using Yin-Yang-Feedback Memory Cell Technology. *Symp. VLSI Circuits Dig.*, 2004, 288-9.

[19] K. Zhang et al. A 3GHz 70Mb SRAM in 65nm CMOS Technology with Integrated Column-Based Dynamic Power Supply. *ISSCC,* 2005, 474-5.

[20] A. Asenov et al., Simulation of intrinsic parameter fluctuations in decananometer and nanometer-scale MOSFETs , *IEEE TED*, vol. 50(9), 1837.

Table 2. Summary of Bulk and FinFET SRAM characteristics.

Cell Design	Cell Area (μm^2)	Static Noise Margin (mV)	$I_{CELL,\ STANDBY}$ (nA)
6-T DG w/ 1-FIN NPD (high V_t)	0.36	175	0.191
6-T DG w/ 2-FIN NPD (high V_t)	0.42	240	0.26
6-T DG w/ Rotated NPD (high V_t)	0.41	200	0.191
6-T w/ Feedback (high V_t)	0.35	300	0.193
4-T w/o Gated V_{SS}	0.30	285	5.9
4-T w/ Gated V_{SS}	0.30 *	285	0.076

* There is a per column area overhead for this implementation