Design of Audio and Video decoder for the T-DMB Receiver

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ABSTRACT

We present a low-power architectural MPEG-4 part-10 AVC/H.264 video and MPEG-4 BSAC audio decoder chip capable of delivering high-quality and high-compression in wireless multimedia applications such as DMB (digital multimedia broadcasting). This AV decoder chip comprise all units required for T-DMB multimedia decoding such as system demultiplexer, MPEG-4 AVC/H.264 video decoder and MPEG-4 BSAC audio decoder. The proposed Audio/Video decoder has low power consumption and has been implemented using a standard-cell library in 0.18um 1P6M CMOS technology.

I. INTRODUCTION

In Korea, a new national standard for terrestrial digital multimedia broadcasting (T-DMB) has been developed [1]. DMB is the next generation digital broadcasting service for fixed, mobile and portable user. The Korea T-DMB system adopts as its base the European DAB system known as Eurak-147 [2]. The T-DMB system adds to Eureka-147 various coding, networking and error correcting tools to process multimedia contents. In this paper, we introduce the T-DMB receiver with an emphasis on the audio and video decoder parts and present our solution in the design and implementation of the T-DMB receiver.

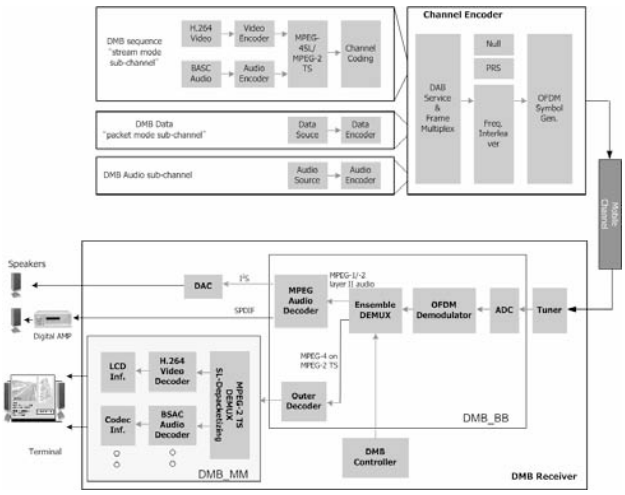

Fig. 1. Concept of T-DMB System

II. SYSTEM OVERVIEW

In order to offer mobile digital TV and multimedia service in T-DMB system, MPEG part-10 AVC/H.264 video and MPEG-4 BSAC audio based DMB system by using the "steam mode sub-channel" is used. As it is shown in Fig.1, first, we multiplex H.264 and BSAC encoded audio and video elementary steams into a MPEG-4 sync layer and MPEG-2 transport stream. Secondly we improve the error protection channel coding by additional blocks like scrambler, RS coder and convolutional interleaver. [3] And then, packetized Audio/Video stream in the MPEG-2 TS flows into Eureka-147 system.

1) Transport Stream Specification

MPEG-2 transport stream layer multiplexes video, audio and auxiliary data to form a single program. It uses PCR for system clock recovery. MPEG-4 system layer provides synchronization among ESs using OCR, CTS, and DTS together with the PCR described above. It uses the SL packetization.

- PAT (Program Association Table) : 1 program, ≤ 500 ms.
- PMT (Program Map Table) : includes IOD_descriptor, SL_descriptor and ≤ 500 ms.
- transmission period of PCR : ≤ 100 ms
- transmission period of OCR : ≤ 700 ms
- transmission period of CTS : ≤ 700 ms

2) Video Object

Video objects are based on ITU-T Rec.H.264 | ISO/IEC 14496-10 [3].

- Comply with the "Baseline Profile and Level 1.3"
- "Arbitary slice order" shall not be allowed
- "Picture Parameter Sets," num_slice_groups_minus1 =0
- "Picture Parameter Sets," redundant-pic_present_flag =0
- "Sequence Parameter Sets," pic_order_cnt_type =2
- "Sequence Parameter Sets," num_ref_frames =3
- Resolutions supported : the formats listed in table 2
- Vertical MV component range : [-64,+63.75]
- Max frame rate : 30 fps
- MaxDPB shall be 445.5kbytes at maximum.

Table 1 Resolution supported

Format	PicWidthinMbs	FrameHeightinMb	PicSizeInMbs
QCIF	11	9	99
QVGA	20	15	300

WDF	24	14	336
CIF	22	18	396

3) Audio Object

Audio object specification conforms to the standard relevant to the ER BSAC Audio Object Type with ObjectType ID 22 defined in ISO/IEC IS 14496-3[4]. Audio object bitstream has the following restrictions.

- In AudioSpecificConfig(), epConfig =0
- In GASpecificConfig(),frame lengthFlag =0
- In bsac_header, sba_mod = 0, no error resilience tool
- In general_header(),ltp_data_present = 0

The restrictions in Table 2 shall be applied.

Table 2. Restriction on audio objects

Items	Value
Sampling Rate	24KHz, 44.1KHz, 48KHz
Number of channels	1, 2
Number of objects	1
Maximum bit rates	128kbps

III. AUDIO/VIDEO DECODER ARCHITECTURE

We developed a SoC to implement the low-power, high performance Audio/Video decoder for T-DMB receiver. Fig. 2 shows the major function units of the audio/video decoder of T-DMB receiver. (we call it "DMB_MM")

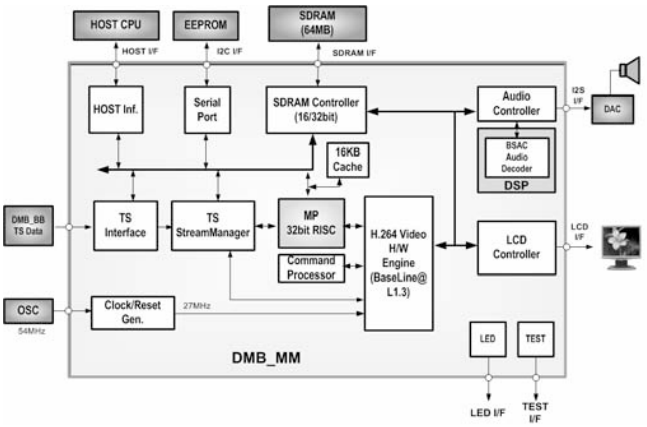

Fig2. Audio/Video decoder block diagram

The functional blocks are divided into largely 3 parts system demultiplex, video decoding and audio decoding. System demultiplex part consists of TS interface and TS manager, RISC processor, and parser logic that connect to SDRAM controller. System demultiplex part receives transport stream and demultiplex T-DMB stream and store the parsed elementary stream into SDRAM.

Video decoder part decodes the video stream stored in SDRAM and writes the decoded pictures in SDRAM. The video decoder is capable of decoding MPEG-4 AVC/H.264 with constraint parameter set. Its architecture is based on dedicated hardware for variable length decoding, inverse DCT, dequantization and intra/inter prediction, video display and RISC video processor. RISC processor unit decodes the sequence parameter set, picture parameter set and slice layer header information of the H.264 video stream.

Audio decoder part decodes the audio stream stored in SDRAM and writes the PCM audio data to audio codec by I2S interface. Implemented BSAC audio decoder has compatibility in MPEG-4 ER BSAC audio object type of ISO/IEC 14496-3.

All blocks are inter-communicated using two major buses: a 32-bit register bus (R-Bus) and 32bit memory bus (M-bus). In addition to the above 3 major blocks, the I2C interface provides boot loading of EEPROM. Clock and reset generator block provides clocking for all internal blocks and also external memory. Given an input 54/27MHz clocks, all internal components operate at 27MHz except external memory interface and audio engine (ADSP). SDRAM controller block operates at 54/27MHz because of reducing I/O power of 16/32bit data SDRAM interface and DSP block operates at 81MHz.

1) System Demultiplexer

In T-DMB system, audio-visual elementary streams and MPEG-4 system data are encapsulated into MPEG-2 TS after the packetization of MPEG-4 sync layer (SL) packets according to the ISO/IEC 13818-1 framework. System demultiplexer decapsulates packet data stream into section data and PES streams. Each PES packet stream is parsed into each SL packet and section data is parsed into IOD/OD/BIFS. [6]

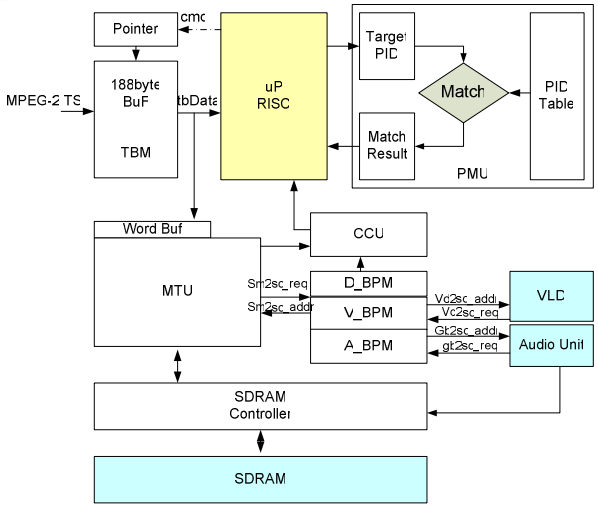

Fig.3. System demultiplexer block diagram

Fig.3. shows system demultiplexer hardware block diagram. 188byte MPEG-2 TS is stored in TBM module and several PIDs are found in RISC processor. After searching PID, audio, video and data elementary bitstreams are transfered into SDRAM by the MTU block. It includes each bitbuffer control block and it can control the overflow and underflow buffer memories.

2) Video Decoding

The basic H.264 functional elements in out design include variable length decoder, intra/inter prediction, inverse transform, inverse quantization and video display engine. (Fig.5)

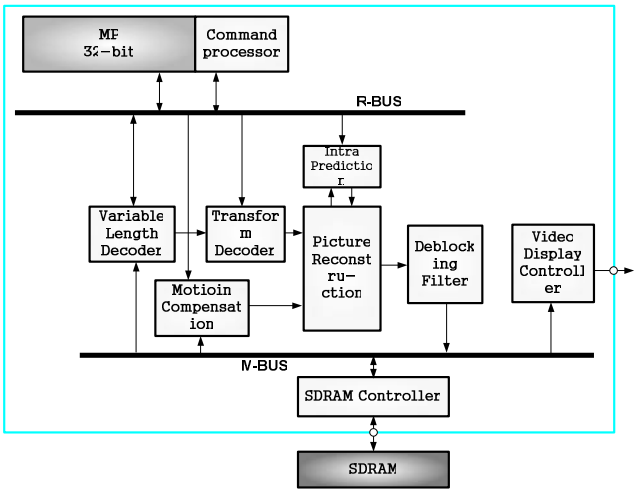

Fig5. Video decoding engine block diagram

After system demultiplexing, video elementary stream is stored in video bit-buffer region in SDRAM. In the 32-bit microprocessor (MP), video elementary stream is analyzed and slice and macro block information is abstracted . MP can control video decoding every video frame synchronization. Fig.6 (a). shows the timing of video decoding.
Video decoding includes sequence parameter set (SPS) and picture parameter set(PPS). VC_pictureL means L-th picture and it has several slice. Fig.6 (b) shows detail timing of slice decoding. This video decoder has hardware command processor (CP) to reduce timing of command processing.

Video Hardware engine has several blocks like as : variable length decoding unit (VLD) reads the CAVLC syntax elements from SDRAM, generates an array of transform coefficient and sends it to the inverse quantization and inverse transformation unit (IQIT) to obtain residual date. The prediction unit reconstructs the image block by commuting intra/inter prediction values and adding to the residue data from the IQIT unit and then deblocking filter unit filters the reconstructed data. The reconstructed data are stored into SDRAM. LCD controller performs functions related to displaying the decoded and reconstructed RGB video images to the LCD screen.

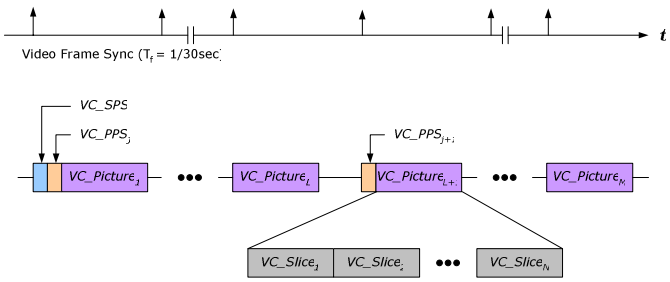

Fig.6. a) overall Timing of video decoding

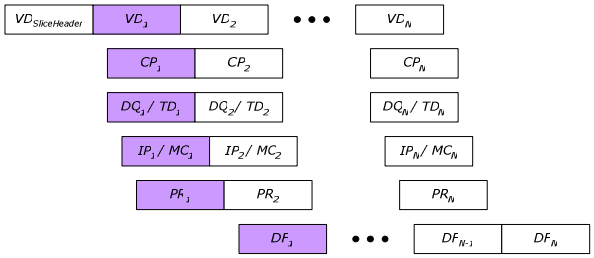

Fig.6. b) detail Timing of slice decoding

3) Audio Decoding

Fig.7. shows the block diagrams of audio decoding. When decoding is start, DSP decodes bsac_header () from audio buffer of SDRAM and writes current frame data size to MMR (Memory mapped register), stream request block requests audio bitstream from SDRAM controller. DSP gets requested audio bitstream from SDRAM and decodes it at every period.

Audio decoding process starts with the audio buffer enable signal of TS Stream manager (SM). The audio bitstream is stored into SDRAM using the System Demux block. When ADSP core sends a request signal for a new frame of audio stream using an interrupts to SDRAM controller, the requested audio stream is delivered to Y-memory. ADSP core then starts processing the input audio stream and decoded audio data is send to the audio controller and transmitted to the D/A converter in a serial format (I2S).

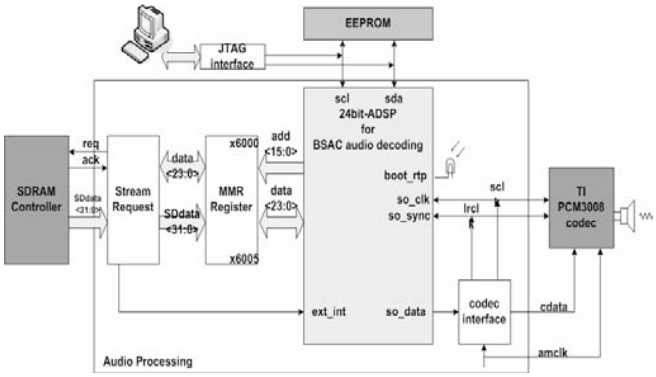

Fig.7. the block diagram of audio decoding

We implemented the audio decoder using ADSP. ADSP is 24bit DSP with a low power consumption level and is optimized for the portable devices. The ADSP core implements most of the audio decoder functions and is equipped with X- , Y-memory and program memory.

IV. TEST AND IMPLEMENTATION

The real-time operation of the AV decoder was verified using different sequences at the bit-rates from 572kbps to 1.2Mbps. We have developed the prototype FPGA board of T-DMB receiver in Fig.8. We tested this test board in real broadcasting environment. The operation frequency of the overall system was set at 54/27MHz. Fig.9. shows the waveform of the result of RTL simulation. As you can see, input is TS packet with 4MHz period and video decoding is performed every 30 frame/s synchronization.

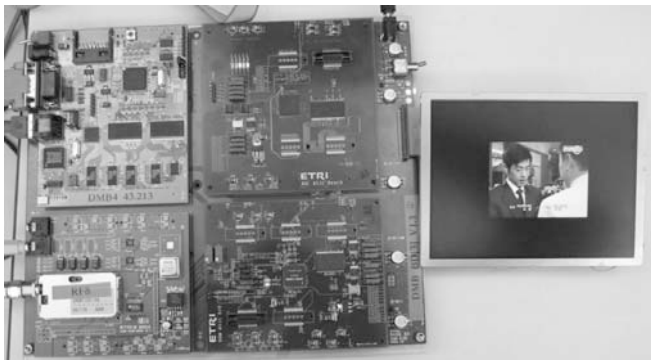

Fig.8 T-DMB Test Receiver Board

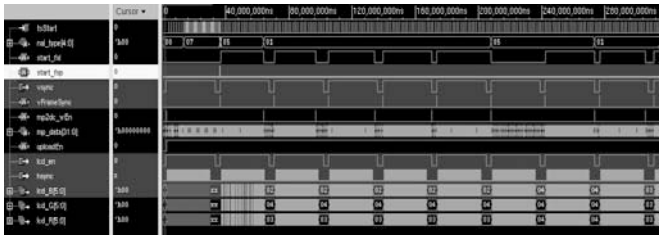

Fig.9. simulation results of RTL coding

After verifying the FPGA prototype T-DMB system, we make Audio/Video Decoder SoC ASIC chip. Fig.10. shows the layout of this SoC ASIC. In table 3, you can see the key feature of audio/video decoder of T-DMB receiver. Our AV decoder chip was implemented using SMIC's 0.18um standard cell library technology. The total gate count with memory was estimated to be 1,860,000 gates. Chips size is about 6mm x 6mm and power consumption is estimated by 120mW.

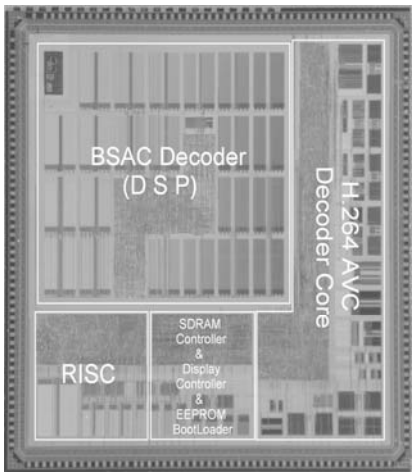

Fig.10. the chip layout of Audio/Video Decoder

Table 3 : Key Features of Audio/Video Decoder Chip

Parameter	*Feature*
Technology	0.18-μm CMOS 6M1P
Chip size	5.8 mm x 5.8 mm
Main Clock	27 MHz
Power supply	3.3 V
Pin	224Pin
Power dissipation	~ 120 mW

V. CONCLUSION

We implemented single chip Audio/Video decoder for the T-DMB receiver. The developed AV decoder chip performed 30 frames/s of CIF at 27MHz in real-time. The AV decoder chips size is 6m x 6m using a standard-cell library in 0.18um CMOS technology. The proposed architecture brings about high cost-effectiveness and low power consumption for the portable T-DMB.

References

[1] The Document of DMB specification, 2004.08
[2] "Radio Broadcasting System: Digital Audio Broadcasting (DAB) to mobile, portable and fixed receivers*," ETSI EN 300 401 v1.3.3,* May, 2003.
[3] Byungjun Bae et al "Design and implementation of the ensemble remultiplexer for DMB service based on Eureka-147" ETRI J. Vol 26 No.4 Aug. 2004
[4] ISO/IEC 14496-10 "Information technology-Coding of audio-visual objects –Part 10: Advanced Video Coding "
[5] ISO/IEC 14496-3 "Information technology-Coding of audio-visual objects –Part 3: Audio"
[6] Bongho Lee at al "A framework for MPEG-4 contents delivery over DMB" ETRI J. Vol 26 No.2 Apr, 2004.