Robust Reconfigurable Filter Design Using Analytic Variability Quantification Techniques

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***Abstract*— In this paper, we develop a variability-aware design methodology for reconfigurable filters used in multi-standard wireless systems. To model the impact of statistical circuit component variations on the predicted manufacturing yield, we implement several different analytic variability quantification techniques based on a double-sided implementation of the first and second order reliability methods (FORM and SORM), which provide several orders of magnitude improvement in computational complexity over statistical sampling methods. Leveraging these efficient analytic variability quantification techniques, we employ an optimization approach using Sequential Quadratic Programming to simultaneously determine the fixed and tunable/switchable circuit element values in an arbitrary-order canonical filter to improve the overall robustness of the filter design when statistical variations are present. The results indicate that reconfigurable filters and impedance matching networks designed using the proposed methodology meet the specified performance requirements with a 26% average absolute yield improvement over circuits designed using deterministic techniques.**

I. Introduction

As wireless applications such as cellular telephones (GSM/CDMA), global positioning systems (GPS), Bluetooth, wireless local area networks (802.11a/b/g and WiMAX), and ultrawideband (UWB) based wireless consumer electronics become increasingly more pervasive, the development of systems that support multiple wireless standards with different operating frequencies is crucial [1]. To reduce both implementation complexity and power consumption, it is desirable to minimize the required hardware for multi-standard RF transceivers by employing reconfigurable circuit blocks for receiving and transmitting the signals associated with the different wireless standards [2]. However, efficiently realizing these reconfigurable multi-standard wireless communication systems poses significant modeling and design challenges [3].

In multi-standard wireless systems, an important challenge is the realization of reconfigurable filters for frequency selection and impedance matching in circuits such as low noise amplifiers, power amplifiers, mixers, and pre-processing filters [4]–[8]. Reconfigurable filters have been physically realized utilizing standard semiconductor-based switches and varactors [9], [10], RF MEMS-based switches and/or tunable capacitors [6]–[8], [11], and varactors implemented using barium-strontium-titanate (BST) dielectrics [12]. In the past, the design of reconfigurable filters has primarily been a manual process that combines well-established design methods for standard non-tunable filters with the specific knowledge of the designer. Recently, we developed an automated design technique for reconfigurable filters leveraging a constraint-relaxation optimization method to generate circuits that deterministically meet the specified design requirements [13]. However, to facilitate the development of low cost multi-standard wireless solutions with greater reliability and manufacturing yield, these deterministic filter design techniques must be augmented with design methods that systematically consider circuit component variations.

In this paper, we develop a variability-aware design methodology for reconfigurable filters used in multi-standard wireless systems. To model the impact of statistical circuit component variations on the predicted manufacturing yield, we implement several different analytic variability quantification techniques based on a double-sided implementation of the first and second order reliability methods (FORM and SORM), which provide several orders of magnitude improvement in computational complexity over statistical sampling methods. Leveraging these efficient analytic variability quantification techniques, we employ an optimization approach using Sequential Quadratic Programming to simultaneously determine the fixed and tunable/switchable circuit element values in an arbitrary-order canonical filter to improve the overall robustness of the filter design when statistical variations are present. The results indicate that reconfigurable filters and impedance matching networks designed using the proposed methodology meet the specified performance requirements with a 26% average absolute yield improvement over circuits designed using deterministic techniques.

II. Modeling and Design of Reconfigurable Filters

Filters have important implications for impedance matching and frequency selectivity, which greatly impact RF receiver performance metrics such as noise, power consumption, and gain. The level of input and output impedance matching, which should be large in the passband of the filter and small in the stopband of the filter, is typically measured using the scattering parameters $|S_{11}|$ and $|S_{22}|$. The insertion loss, which is the attenuation of a signal passing through the filter and is typically measured using $|S_{21}|$, should be minimized in the passband. The filter must also be designed to satisfy the power handling constraints imposed by its circuit elements, which are especially important for tunable/switchable RF MEMS components [14].

Reconfigurable filters are significantly more challenging to design than their fixed valued counterparts since they must provide passband impedance matching and stopband rejection for different sets of frequencies while only modifying a small number of switchable and/or tunable circuit element values. In general, reconfigurable microwave filters in multi-standard wireless applications are realized using either lumped circuit elements or microstrips. Both lumped and microstrip filters are typically designed using canonical lumped filter representations such as the Butterworth/Chebyshev bandpass filter topology displayed in Figure 1 [17], [18] where one or more of the passive components may have multiple tunable/switchable values. Once the fixed and reconfigurable circuit elements in the canonical filter are determined, the filter can be physically synthesized by

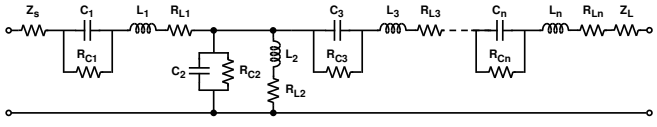

Fig. 1. Canonical bandpass filter topology with order n.

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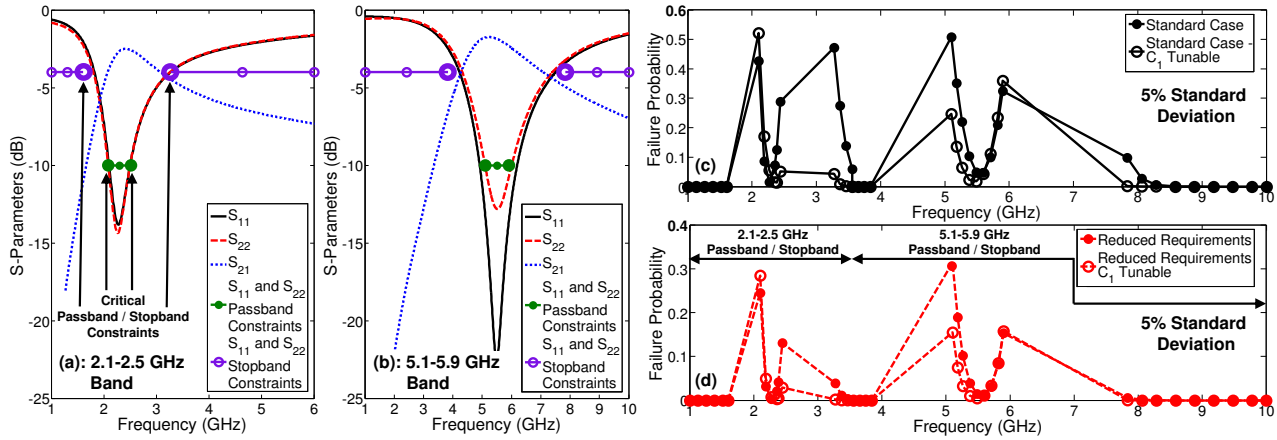

Fig. 2. (a) and (b) – S-parameters for the 3rd order 2-band design (design example 1 listed in Table II) that satisfy the depicted passband and stopband constraints; (c) and (d) – Probability that the 3rd order 2-band design does not meet the performance requirements on $|S_{22}|$ at each of the frequencies in the passband and the stopband for standard ($|S_{22}| \leq -10\ dB$ and $|S_{22}| \geq -4\ dB$) and reduced ($|S_{22}| \leq -9\ dB$ and $|S_{22}| \geq -5\ dB$) design requirements.

employing lumped passive components for each circuit element or by utilizing well-known techniques to transform the lumped circuit elements into their equivalent transmission line representations [17], [18]. Therefore, to develop a generalized technology-independent variability-aware design method to improve the manufacturing yield of reconfigurable filters, we focus on the design of the fixed and tunable/switchable component values in the canonical filter topology displayed in Figure 1 in this paper.

To model the impedance matching and insertion loss associated with the filter topology of order n displayed in Figure 1, we utilize a two-port ABCD parameter formulation, which provides a convenient means for characterizing the cascaded stages of the filter. The S-parameters (S_{11}, S_{21}, S_{22}) of the filter are then determined based on the ABCD parameters using standard 2-port parameter transformations [18]. The parasitic resistances associated with the capacitors and inductors in the filter model are calculated based on the quality factor of the passive components. Given the power handling limitations of certain reconfigurable filter implementation technologies such as RF MEMS [14], we also model the voltage, current, and power at each node in the filter. We provide more details on the filter model in [13]. Leveraging this generalized model, we can efficiently characterize and optimize the yield of reconfigurable filters in multi-standard wireless applications when circuit component variations are present.

III. Variability Quantification for Reconfigurable Filters

A. Impact of Circuit Component Variations

Sources of statistical variation must be considered in during the reconfigurable filter design process in order to generate robust designs with acceptable manufacturing yield. For reconfigurable filters, the sources of statistical variation can include both the uncertainty in the complex electromagnetic models for the implemented lumped and distributed filters as well as process variations during fabrication. The distribution and standard deviation of the manufactured circuit component values will depend on the implementation technology for the filter. For instance, in [15] integrated capacitors implemented using metal finger and metal-insulator-metal topologies have reported standard deviations in capacitance of 0.65% and 0.11%, respectively, while in [16], a standard deviation in effective inductance of up to 5% was theoretically predicted for integrated spiral inductors. Given the technology-dependent nature of the statistical distribution of circuit component values, we consider a wide-range of possible standard deviation values in this paper.

To understand the impact of circuit component variations on reconfigurable filters, we examine the yield of a 3rd order 2-band reconfigurable filter design created using the deterministic design optimization method discussed in [13]. The design and its specifications correspond to design example 1 listed in Table II in Section V. The filter is implemented with fixed capacitor values of $[C_1, C_2, C_3] = [0.964, 1.155, 0.921]$ pF and with fixed inductor values of $[L_1, L_3] = [0.1, 0.1]$ nH. The 2-bands are selected using a switchable inductor with values of $L_2 = [2.001, 0.552]$ nH, which correspond to the 2.1-2.5 GHz and 5.1-5.9 GHz bands, respectively. The performance characteristics of the 2-band reconfigurable filter are depicted in Figures 2a and 2b, respectively. As displayed in the figures, each operating band has a range of passband and stopband constraints with the *critical passband constraints* defined as the constraints on the S-parameters at the frequencies at the edge of the passband and the *critical stopband constraints* defined as the constraints on the S-parameters at the frequencies in the stopband closest to the passband.

To assess the yield implications of circuit component variations, we simulated the probability of a constraint violation for $|S_{22}|$ at several discrete frequencies in the passband and the stopband using Monte Carlo sampling. Figure 2c depicts this point-wise constraint violation probability for independent normally distributed circuit component values with standard deviations of 5%. Note that the constraint violation probabilities associated with $|S_{11}|$ and $|S_{21}|$ produce similar results. Within a given continuous passband or stopband frequency region, the critical passband and stopband constraints have the largest point-wise constraint violation probability, and these probabilities are highly correlated with the constraint violation probabilities at nearby frequencies. Therefore, the critical passband and stopband constraints will typically have the most impact on the overall yield of the reconfigurable filter. To reduce the probability of a constraint violation, we can exploit the post-fabrication reconfigurability provided by additional tunable circuit elements in the filter design. The results depicted in Figure 2c demonstrates that the point-wise constraint violation probability is substantially reduced if tunable circuit elements are added to increase the yield. Reducing the aggressiveness of the passband and stopband design requirements to $|S_{22}| \leq -9\ dB$ and $|S_{22}| \geq -5\ dB$ also decreases the probability of a constraint violation as displayed in Figure 2d.

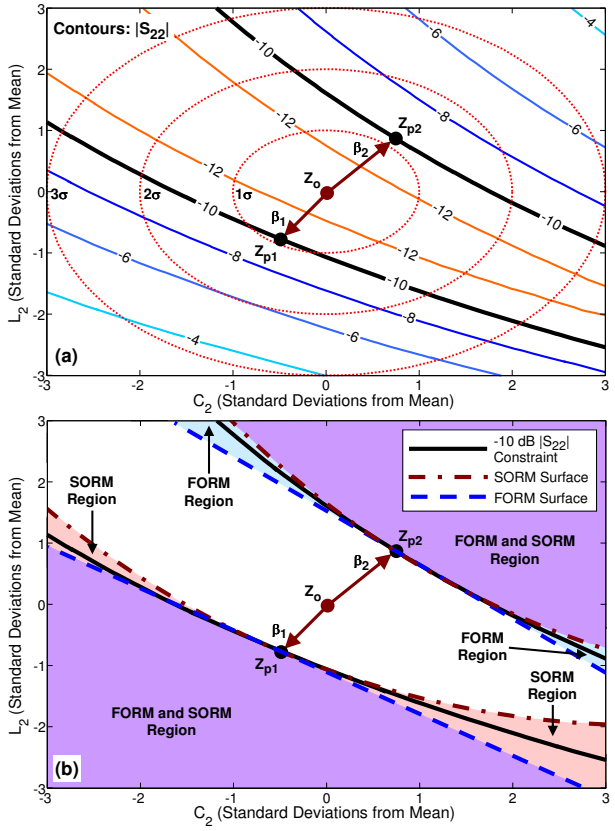

Fig. 3. (a) $|S_{22}|$ contours for the 3rd order 2-band design (band 2 at 5.5 GHz) in the z-plane where the statistical distributions of C_2 and L_2 have been converted to independent normal random variables with standard deviations of 1. (b) Regions of integration corresponding to the DS-FORM and DS-SORM analytic variability quantification methods.

B. Methods for Variability Quantification

To effectively optimize the design of the reconfigurable filter, we must be able to efficiently characterize the performance impact of statistical component variations. Random sampling using Monte Carlo simulation is the traditional approach for determining the statistical distribution of a given performance metric resulting from circuit component variations. The number of samples ($N_{samples}$) required to achieve a level of accuracy (a) for a given failure probability (P_f) for a Monte Carlo simulation can be approximated by $N_{samples} = (1-P_f)/(a^2 P_f)$ [19]. To obtain an accuracy level of $a = 0.01$ (1%) when using Monte Carlo simulation, 10^4 samples are needed when P_f is 0.5, and approximately 10^6 samples are needed when P_f is 0.01. While more sophisticated techniques such as Latin Hypercube Sampling and Importance Sampling can reduce the required number of samples by an order of magnitude [20], [21], the required number of samples is still too computationally demanding for optimization problems where the statistical model must be evaluated hundreds of times for a large number of performance constraints. Furthermore, for gradient-based nonlinear optimization techniques, the random nature of sampling techniques will cause numerical stability problems during the computation of finite-difference gradients.

In contrast to sampling techniques, analytic variability quantification methods deterministically calculate the failure probability without random sampling based on

$$P_f = P[g(\overrightarrow{x_v}) \geq g_c] = \int_{g(\overrightarrow{x_v}) \geq g_c} f(\overrightarrow{x_v}) d\overrightarrow{x_v} \qquad (1)$$

where $g(\overrightarrow{x_v})$ and g_c correspond to a given performance metric and its associated constraint, respectively. The vector $\overrightarrow{x_v}$ contains the circuit component random variables, and $f(\overrightarrow{x_v})$ is the joint probability density function of the circuit component value distribution [22]. In general, directly computing the integral in (1) requires computationally complex numerical methods. Consequently, efficient techniques for approximating (1) are needed.

C. Analytic Variability Quantification with FORM and SORM

The first and second order reliability methods (FORM and SORM) have been developed to efficiently approximate (1) in order to determine P_f with respect to a particular performance requirement [22]–[24]. The general process for these analytic variability quantification techniques typically consists of the following steps [23]:

1) Map the set of random variables $\overrightarrow{x_v}$ (x-space) with their arbitrary statistical distributions to a set of normal random variables $\overrightarrow{z_v}$ (z-space) with a mean of 0 and a standard deviation of 1 using standard methods such as the Rosenblatt or Nataf transformations [23];
2) Determine the most probable points (MPP) of failure associated with each performance constraint in z-space;
3) Compute a first or second order approximation of the constraint surface at the MPPs and use the approximation to estimate P_f.

Steps 2 and 3 are explained in detail in the following sections.

1) MPP Calculation: The MPP is defined as the closest point in z-space to the origin where the performance constraint is violated. This corresponds to the point in the z-plane where the highest probability of a constraint violation occurs based on the jointly normal distribution of the transformed design variables. To locate the MPP for a given performance constraint, we solve the following nonlinear optimization problem:

$$\begin{aligned} \textbf{Minimize} \quad & \| \overrightarrow{z_v} \|_2 \\ \textbf{Subject to} \quad & g_z(\overrightarrow{z_v}) \geq g_c \\ & -\sigma_z \leq \overrightarrow{z_v} \leq \sigma_z \end{aligned} \qquad (2)$$

where $g_z(\overrightarrow{z_v})$ is a given performance constraint function mapped to the z-plane variables, and σ_z is a bound on the space of the statistically significantly standard deviations in which to search for the MPP. We set $\sigma_z = 3$ in this study. Figure 3a displays the $|S_{22}|$ contours for the 3rd order 2-band design (band 2 at 5.5 GHz) in the z-plane where the statistical distributions of C_2 and L_2 have been converted to independent normal random variables with a standard deviation of 1. In this case, the performance constraint is $|S_{22}| \leq -10\ dB$. The first MPP associated with the two design variables is indicated by the point $\overrightarrow{z_{p1}}$.

While in many applications only one MPP is statistically significant, for typical filter performance constraints on the S-parameters at certain frequencies, only a narrow range of circuit component values will meet the specified performance requirements. Therefore, in addition to locating the primary MPP by solving (2), we also search for a secondary MPP, $\overrightarrow{z_{p2}}$, by solving (2) with the additional constraint on $\overrightarrow{z_v}$ that the solution must be in the opposite quadrant from the quadrant containing $\overrightarrow{z_{p1}}$. In practice, it typically requires several hundred model evaluations to locate $\overrightarrow{z_{p1}}$ and $\overrightarrow{z_{p2}}$, which is several orders of magnitude less than the number of model evaluations required for Monte Carlo simulations as we discuss in Section III-D.

2) First/Second Order Constraint Surface: Once we have determined the MPPs associated with a particular constraint, we utilize either a first or second order approximation of the constraint surface

TABLE I
COMPARISON BETWEEN ANALYTIC VARIABILITY QUANTIFICATION METHODS FOR THE 3RD ORDER 2-BAND FILTER (DESIGN EXAMPLE 1)

Std. Dev.	Freq. (GHz)	$\|S_{11}\|$ Req. (dB)	Probability of Not Meeting $\|S_{11}\|$ Requirement FORM	DS-FORM	SORM	DS-SORM	Sampling
5%	1.60	≥-4	0	0	0	0	0
	2.10	≤-10	0.402	0.402	0.408	0.408	0.419
	2.30	≤-10	0.018	0.020	0.026	0.028	0.022
	2.50	≤-10	0.500	0.500	0.516	0.516	0.499
	3.27	≥-4	0.471	0.471	0.478	0.478	0.474
	3.84	≥-4	0	0	0	0	0
	5.10	≤-10	0.500	0.500	0.505	0.505	0.513
	5.50	≤-10	0.035	0.046	0.040	0.053	0.048
	5.90	≤-10	0.328	0.328	0.335	0.335	0.328
	7.89	≥-4	0.096	0.096	0.104	0.104	0.098
2%	1.60	≥-4	0	0	0	0	0
	2.10	≤-10	0.267	0.267	0.270	0.270	0.277
	2.30	≤-10	0	0	0	0	0
	2.50	≤-10	0.500	0.500	0.507	0.507	0.495
	3.27	≥-4	0.428	0.428	0.430	0.430	0.424
	3.84	≥-4	0	0	0	0	0
	5.10	≤-10	0.500	0.500	0.502	0.502	0.504
	5.50	≤-10	0	0	0	0	0
	5.90	≤-10	0.132	0.132	0.134	0.134	0.133
	7.89	≥-4	0.001	0.001	0.001	0.001	0.001
Mean Relative Error Between FORM/SORM and Sampling			3.06%	1.42%	2.77%	3.11%	N/A
Mean Absolute Error Between FORM/SORM and Sampling			0.004	0.003	0.005	0.005	N/A
Average CPU Time (s)			0.18	0.22	0.18	0.22	293.34

at the MPPs to determine P_f. We calculate the first order linear approximation of the constraint surface at the MPP using

$$P_{form1} = \Phi(\pm\beta_1) \tag{3}$$

where P_{form1} is the probability of a constraint violation based on the first order information at $\overrightarrow{z_{p1}}$, $\Phi(\cdot)$ is the standard normal cumulative distribution function, $\beta_1 = \| \overrightarrow{z_{p1}} \|_2$, and the sign of β_1 is determined by the type of constraint function [23]. This is known as the first order reliability method (FORM). Based on $\overrightarrow{z_{p2}}$, we also calculate the probability of a constraint violation (P_{form2}) at the secondary MPP using a formulation similar to (3). Figure 3b depicts the region of integration used to determine P_{form1} and P_{form2}. The total probability of failure is $P_f = P_{form1} + P_{form2}$. We refer to this as *double-sided FORM* (DS-FORM).

To provide a second order approximation of the constraint surface at the MPP, more complex formulations are required. In [24], the authors develop an analytic technique to obtain this second order approximation based on a local circular representation of the angle of curvature near the MPP, which is depicted in Figure 3b. This technique is known as the second order reliability method (SORM). Details on a typical method for the calculation of the probability of a constraint violation at a given MPP (P_{sorm1} at $\overrightarrow{z_{p1}}$ or P_{sorm2} at $\overrightarrow{z_{p2}}$) using SORM are provided in [24]. When we use both the primary and secondary MPPs to calculate P_f ($P_f = P_{sorm1} + P_{sorm2}$), we refer to this as *double-sided SORM* (DS-SORM).

D. Accuracy and Speed of FORM and SORM for Filter Design

To assess the accuracy of analytic variability quantification using the FORM and SORM, we compare the probability of a constraint violation computed using these techniques to Monte Carlo simulation results for the 3rd order 2-band reconfigurable filter design discussed in Section III-A with circuit component value variations that are normally distributed with standard deviations of 5% and 2%. The results are listed in Table I. In certain cases, using SORM/DS-SORM over FORM/DS-FORM provides a modest improvement in the accuracy of P_f. However, in other cases, the circular curvature used to approximate the constraint surface using the SORM formulation from [24] overestimates P_f, particularly in the cases where the double-sided methods yield substantially different results from standard FORM/SORM. The DS-FORM technique provides the lowest error (1.42%) on average for the simulated cases with respect to the Monte Carlo simulation results. Furthermore, the DS-FORM method provides three orders of magnitude improvement in runtime over Monte Carlo simulations with enough samples to provide 1% accuracy.

IV. VARIABILITY-AWARE RECONFIGURABLE FILTER DESIGN OPTIMIZATION

We formulate the variability-aware design optimization problem for reconfigurable filters as

$$\begin{aligned} \textbf{Minimize} \quad & P_{ftotal} \\ \textbf{Subject to} \quad & \mathbf{S_{11IT}} \leq \mathbf{S_{11IC}},\ \mathbf{S_{11OT}} \geq \mathbf{S_{11OC}} \\ & \mathbf{S_{22IT}} \leq \mathbf{S_{22IC}},\ \mathbf{S_{22OT}} \geq \mathbf{S_{22OC}} \\ & \mathbf{S_{21IT}} \geq \mathbf{S_{21IC}},\ \mathbf{S_{21OT}} \leq \mathbf{S_{21OC}} \\ & \mathbf{S_{PT}} \leq \mathbf{S_{PC}} \\ & \overrightarrow{x_{min}} \leq \overrightarrow{x} \leq \overrightarrow{x_{max}} \end{aligned} \tag{4}$$

where P_{ftotal} is the summation of the probabilities that each performance metric will fail to meet its required value for the applicable *critical passband constraints* and *critical stopband constraints* on $|S_{11}|$, $|S_{21}|$, and $|S_{22}|$ as well as for the applicable power handling constraints in each of the M frequency bands of the reconfigurable filter. We also probabilistically compute the failure probability associated with the S-parameter constraints that are *active* at the conclusion of the deterministic optimization process. The failure probabilities are calculated using the DS-FORM method described in Section III-C. Note that we continue to deterministically apply the non-critical passband and stopband constraints on $|S_{11}|$, $|S_{21}|$, and $|S_{22}|$ during the optimization process to ensure that the design will continue to meet the specified design requirements.

The design variables in the optimization problem are the individual fixed and tunable/switchable capacitors and inductors in each series and shunt branch of the nth order filter,

$$\overrightarrow{x} = \left[\overrightarrow{C_1}, \overrightarrow{C_2}, \cdots, \overrightarrow{C_n}, \overrightarrow{L_1}, \overrightarrow{L_2}, \cdots, \overrightarrow{L_n}\right]. \tag{5}$$

If $\overrightarrow{C_i}$ or $\overrightarrow{L_i}$ is a switchable or tunable circuit element, the design variable vector contains several component values that span the element value ranges associated with the switchable or tunable states. The deterministic passband constraints on $|S_{11}|$ ($\mathbf{S_{11IT}} \leq \mathbf{S_{11IC}}$), $|S_{22}|$ ($\mathbf{S_{22IT}} \leq \mathbf{S_{22IC}}$) and $|S_{21}|$ ($\mathbf{S_{21IT}} \geq \mathbf{S_{21IC}}$) as well as the deterministic stopband constraints on $|S_{11}|$ ($\mathbf{S_{11OT}} \geq \mathbf{S_{11OC}}$), $|S_{22}|$ ($\mathbf{S_{22OT}} \geq \mathbf{S_{22OC}}$), and $|S_{21}|$ ($\mathbf{S_{21OT}} \leq \mathbf{S_{21OC}}$) are defined in the same manner as those described in [13]. The constraint $\mathbf{S_{PT}} \leq \mathbf{S_{PC}}$ limits the power at each node of the filter to ensure that the power handling capabilities of the circuit components are not exceeded in any of the possible reconfigurable states. The circuit element values are constrained by x_{min} and x_{max} to ensure that their values are suitable for on-chip or in-package integration.

The first step in the proposed variability-aware reconfigurable filter design methodology is to leverage the deterministic automated design method proposed in [13] to create a reconfigurable filter design that provides a suitable start point for the variability-aware design optimization process. We then solve the (4) using Sequential Quadratic

TABLE II

RECONFIGURABLE FILTER DESIGN EXAMPLES FOR THE VARIABILITY-AWARE DESIGN METHODOLOGY

Design Example	Frequency Bands (GHz)	Z_s (Ω)	Z_L (Ω)	S^i_{11min} & S^i_{22min}	S^i_{11max} & S^i_{22max}	R_{Bi} & R_{Ti}	L_{min} (nH)	L_{max} (nH)	C_{min} (pF)	C_{max} (pF)	Quality Factor	S_{PC} (mW)
1 (3rd order)	WCDMA – 802.11b/g (2.1–2.5 GHz) and 802.11a (5.1–5.9 GHz)	50	80	-10 dB	-4 dB	0.300	0.10	10.0	0.01	5.0	20 (L) and 50 (C)	N/A
2 (5th order)	WCDMA (2.11–2.17 GHz) 802.11b/g (2.405–2.484 GHz) 802.11a (5.15–5.35 GHz) 802.11a (5.725–5.825 GHz)	25 to 50	50	-10 dB	-3 dB	0.130	0.05	5.0	0.05	5.0	100 (Resonator)	500

TABLE III

PERCENTAGE YIELD FOR EXAMPLE 1 CREATED WITH AND WITHOUT VARIABILITY-AWARE OPTIMIZATION (VAO)

		Percentage of Designs Meeting Requirements (Yield in %)							
		No Tunable		C_1 Tunable		C_2 Tunable		C_3 Tunable	
Req. Set	Std. Dev.	No VAO	With VAO	No VAO	With VAO	No VAO	With VAO	No VAO	With VAO
1	5.0%	<0.1	<0.1	0.1	0.3	0.1	0.4	<0.1	0.3
	2.0%	<0.1	1.0	0.4	3.5	1.0	6.0	0.2	3.9
	1.0%	0.1	8.3	1.3	15.1	3.4	26.2	0.8	21.6
	0.5%	0.4	31.4	3.5	41.0	8.3	62.0	2.1	62.1
2	5.0%	4.3	8.3	9.9	14.6	25.3	37.8	9.6	16.8
	2.0%	29.2	47.7	45.1	59.4	66.9	87.2	38.7	68.7
	1.0%	68.5	88.7	83.0	93.7	96.4	99.8	80.1	97.7
	0.5%	97.3	>99.9	99.7	>99.9	>99.9	>99.9	99.6	>99.9
3	5.0%	16.6	38.4	27.7	52.4	51.9	86.5	28.5	63.8
	2.0%	69.0	94.3	81.3	97.3	96.6	>99.9	78.3	99.8
	1.0%	98.2	>99.9	99.5	>99.9	>99.9	>99.9	99.2	>99.9
	0.5%	>99.9	>99.9	>99.9	>99.9	>99.9	>99.9	>99.9	>99.9

Requirement Set 1:	Passband $\lvert S_{11}\rvert$ and $\lvert S_{22}\rvert \leq -10\ dB$ Stopband $\lvert S_{11}\rvert$ and $\lvert S_{22}\rvert \geq -4\ dB$
Requirement Set 2:	Passband $\lvert S_{11}\rvert$ and $\lvert S_{22}\rvert \leq -9.5\ dB$ Stopband $\lvert S_{11}\rvert$ and $\lvert S_{22}\rvert \geq -4.5\ dB$
Requirement Set 3:	Passband $\lvert S_{11}\rvert$ and $\lvert S_{22}\rvert \leq -9\ dB$ Stopband $\lvert S_{11}\rvert$ and $\lvert S_{22}\rvert \geq -5\ dB$

Programming (SQP), a gradient-based nonlinear programming technique [25]. Based on the simulations in [13], the reconfigurable filter design problem is convex in the local region around any given point in the design space, and therefore, SQP is well-suited for solving the variability-aware reconfigurable filter optimization problem. The solution to the optimization problem provides the circuit element values for the variability-aware design. Once a final set of circuit values is obtained, we then utilize sampling techniques to determine the yield provided by the design.

Several different runs of the optimization method with different design requirements and circuit configurations can be performed to examine the trade-off between hardware complexity, design requirements, and the desired manufacturing yield when a given level of statistical variation in the circuit component values is present. Specifically, we combine variability-aware optimization with two other complementary design techniques to increase manufacturing yield: (1) replace the fixed circuit elements with tunable components to dynamically compensate for circuit component value variations post-fabrication and (2) relax the design requirements associated with the reconfigurable filter. By applying these design techniques in conjunction with variability-aware optimization, we can produce reconfigurable filter designs with the desired hardware complexity, performance, and yield.

V. RESULTS

To evaluate the yield improvement provided by the variability-aware design methodology for reconfigurable filters, we apply the proposed methodology to two design examples, which are initially created using the deterministic optimization process described in [13] based on the constraints listed in Table II. We assume independent and normally distributed circuit component value variations with standard deviations ranging from 5% to 0.5%. Note that when tunable elements are added for the purposes of variability compensation, we assume that the maximum and minimum values of the tunable elements have a 4-to-1 ratio, which can be attained by both RF MEMS and semiconductor based variable capacitors [9], [26].

In design example 1, we consider filters with the 3 sets of design requirements listed in Table III. We previously discussed the deterministic version of the 3rd order 2-band filter in design example 1 in Section III-A and in Figures 2a and 2b. We also consider the yield of designs with a tunable circuit element replacing either C_1, C_2, or C_3. The average CPU time for generating the cases using the variability-aware optimization method is 18.8 minutes using a MATLAB implementation of the proposed method on a Windows machine with a 2.4 GHz AMD Opteron processor and 2 GB of RAM. In contrast, variability-aware optimization using Monte Carlo simulations would require approximately 17.4 days to complete if the numerical instability associated with the random sampling method for finite-difference derivative calculations could be overcome.

Table III lists the percentage of realized filter implementations meeting the requirements for design example 1. We utilize Monte Carlo simulations to determine the percentage yield for each design. Regardless of the presence of tunable circuit elements and/or relaxed design constraints, the variability-aware design optimization process ("with VAO" in Table III) generates reconfigurable filters that provide substantially greater yield than the designs generated using only deterministic optimization ("no VAO" in Table III). Excluding the cases where the yield for the designs created without variability-aware optimization is less than 0.5% and greater than 95.0%, the average yield improvement provided by the variability-aware design optimization process is 21.5% and 412.6% in absolute and relative terms, respectively. On average, this yield improvement is obtained at the expense of a decrease in passband $|S_{21}|$ of 0.13 dB (7.9%). The increasing yield obtained as the design constraints are relaxed from requirement set 1 to requirement set 3 demonstrates that the proposed methodology provides an effective means for exploring the trade-off between performance and yield.

In the second design example, we generate a 5th order reconfigurable impedance matching network with 4 operating frequency bands corresponding to WCDMA (2.11-2.17 GHz), 802.11b/g (2.405-2.484 GHz), and 802.11a (5.15-5.35 GHz and 5.725-5.825 GHz) [5]. The filter is designed to match Z_s values that range from 25 Ω to 50 Ω. The canonical filter's inductor values are $[L_1, \cdots, L_5]$ = [0.050, 0.595, 0.050, 0.526, 2.853] nH, and the filter's fixed capacitor values are $[C_1, C_5]$ = [2.306, 1.561] pF. The continuously tunable elements C_2 and C_4 have capacitance values ranging from [0.050, 0.367] pF and [1.329, 1.233] pF, respectively, to achieve impedance matching when Z_s varies from 25 Ω to 50 Ω. C_3 is a switchable capacitor with

TABLE IV
PERCENTAGE YIELD FOR EXAMPLE 2 CREATED WITH AND WITHOUT VARIABILITY-AWARE OPTIMIZATION (VAO)

Req. Set	Std. Dev.	Percentage of Designs Meeting Requirements (Yield in %) C_2, C_4 Tunable No VAO	C_2, C_4 Tunable With VAO	C_2–C_4 Tunable No VAO	C_2–C_4 Tunable With VAO	C_1–C_5 Tunable No VAO	C_1–C_5 Tunable With VAO
1	5.0%	<0.1	<0.1	<0.1	4.6	30.7	60.0
	2.0%	<0.1	<0.1	6.6	25.8	72.2	99.5
	1.0%	<0.1	<0.1	27.5	59.3	95.6	>99.9
	0.5%	<0.1	4.9	68.9	91.2	99.9	>99.9
2	5.0%	1.8	>99.9	88.8	>99.9	99.8	>99.9
	2.0%	26.3	>99.9	99.7	>99.9	>99.9	>99.9
	1.0%	73.6	>99.9	>99.9	>99.9	>99.9	>99.9
	0.5%	97.9	>99.9	>99.9	>99.9	>99.9	>99.9

Requirement Set 1:	Passband $\|S_{11}\|$ and $\|S_{22}\| \leq -10\ dB$ Stopband $\|S_{11}\|$ and $\|S_{22}\| \geq -3\ dB$ $S_{PC} \leq 500\ mW$
Requirement Set 2:	Passband $\|S_{11}\|$ and $\|S_{22}\| \leq -9\ dB$ Stopband $\|S_{11}\|$ and $\|S_{22}\| \geq -4\ dB$ $S_{PC} \leq 600\ mW$

four discrete values of [4.209, 3.215, 0.520, 0.322] pF that correspond to the four frequency bands of the filter with increasing frequency.

In design example 2, we consider the percentage yield of the nominal case where C_2 and C_4 are tunable circuit elements and cases where the other circuit elements are tunable. We determine the yield for the nominal and reduced design requirement sets displayed in Table IV. Table IV lists the percentage of realized filter implementations meeting the design requirements for design example 2. Excluding the cases where the yield for the designs created without variability-aware optimization is less than 0.5% and greater than 95.0%, the average yield improvement provided by variability-aware optimization is 31.8% and 632.5% in absolute and relative terms, respectively. On average, this yield improvement is obtained at the expense of a decrease in passband $|S_{21}|$ of 0.04 dB (2.8%).

In both design examples, the yield improvement obtained using the variability-aware optimization method greatly depends on the standard deviation of the circuit element values. When the standard deviation of the circuit element values is relatively large, the yield of the design with the nominal requirements is relatively low. This low yield implies that the original deterministic design has extremely aggressive performance requirements given the relatively large circuit element value variations, and therefore, the variability-aware design optimization method can only provide a modest absolute yield increase. In these large standard deviation cases, the variability-aware design optimization method must be coupled with changes in the design such as tunable circuit elements and/or relaxed design requirements to substantially increase the manufacturing yield. Therefore, the designer must decide how to best trade-off the increase in manufacturing yield with the performance implications of relaxed design requirements and the additional circuit complexity of adding tunable circuit elements. The proposed robust automated design methodology provides the designer with the means to efficiently explore this trade-off for a wide range of desired yield values.

VI. CONCLUSION

In this paper, we develop a variability-aware design methodology for reconfigurable filters used in multi-standard wireless systems. Leveraging efficient analytic variability quantification techniques, the proposed method employs an optimization approach using SQP and utilizes tunable circuit elements to improve the overall robustness of the filter when component variations are present. The results indicate that reconfigurable filters and impedance matching networks designed using the proposed methodology meet the specified performance requirements with a 26% average absolute yield improvement over circuits designed using deterministic techniques. The proposed variability-aware design methodology provides a technology-independent means for creating reconfigurable filters with increased reliability and yield, which is crucial for the cost-effective realization of RF transceivers in multi-standard wireless applications.

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