Abstract - As the industry moves from single- to multi-core processors, the challenges of how to reliably design and analyze power delivery for such systems also arise. We study various workload assignments to cores and their impact on the global power grid noise. We develop metrics to estimate the amount of noise propagated from core to core and propose a power supply noise aware workload assignment method. In our experiments, we show that performance loss can be significant if workload assignment is not properly made.

I. INTRODUCTION

Today, more and more processor chips use multiple cores in an attempt to deliver additional system performance within their power budget. In 2001, IBM introduced POWER4, the first multi-core processor chip [1]. A multi-core design consists of several cores integrated on a single chip to maximize throughput. These systems speed up application performance by dividing the workloads among cores and executing them in parallel. Implementing multi-core designs has several challenges such as connectivity and communication between cores, data/cache coherency, and partitioning tasks among the cores. There are also issues related to the physical design of multi-core devices such as signal integrity, power consumption, heat dissipation, and noise immunity. In this work, we focus on power supply noise.

In a multi-core system, each workload can be processed by a single core and may last for many clock cycles. A power delivery system can be shared among the cores. It is also possible for each core to have its own individual power network. In this paper, we study shared-power-network-based multi-core systems. With such a structure, the cores share decoupling capacitance and have lower inductance paths to the package [4]. Figure 1 shows the shared power grid for a four core system.

Given that workloads can last for many cycles, there are cases in which neighboring cores are simultaneously performing tasks. In a shared power grid system, a working core can induce power supply noise on neighboring working cores. The global grid can act as a medium for noise propagation between the cores. In the open literature, there are no studies addressing the problem of power delivery for multi-cores. An intuitive method for designing a power grid could be to optimize it for all cores operational (i.e. switching) with typical clock frequency and current demand. Despite being optimized for such a scenario, the global grid might experience intolerable power grid noise for some configurations of working cores. The challenge of how to assign workloads to cores for minimum performance loss arises. Various workload assignments may create different noise maps. Without an in-depth study of workload assignment and its effect on the global power grid, we might not be able to determine the optimal performance of a multi-core system.

Throughout this paper, we refer to the power supply noise as the noise generated by the working cores. We investigate the problem of workload assignment to minimize the power supply noise, which is an indicator of the system’s performance loss. The chip/package power distribution network is modeled with an RLC network and the cores are modeled with current sources representing their demands. We are considering flip-chip designs with controlled collapse chip connections (C4s) distributed throughout the grid. When assigning workloads in multi-core systems, we must consider and model the core-to-core interactions. The authors of [4] show chip measurements and observations for POWER6, a dual-core microprocessor. They mention that noise from one core could propagate to the other core, and in the worst case, the noise might arrive when the other core is experiencing a locally produced $V_{dd}$ drop, causing the perfect storm.

The existing literature describes techniques for assigning tasks without considering the core-to-core interactions. The authors of [2] consider task scheduling while improving the system performance by applying different voltage levels to the cores. The authors of [3] propose a task assignment scheme that takes cache behavior into consideration. In [11], the authors examine a multi-core system’s architectural description and discuss its susceptibility to power variability caused by process variations. In contrast, we consider the global power grid integrity when various workload assignments are applied.

In this paper, we analyze the global grid in the transient domain. We estimate the voltage drop on the grid before and after a workload assignment and show that a random
assignment can lead to a significant performance loss. We develop metrics to measure noise propagation from core to core. We propose an assignment technique that takes into account the power supply noise of the core and its induced noise on the neighboring cores. We show that utilizing power supply aware workload assignments provides significant performance savings.

The remainder of the paper is organized as follows. In Section II we describe the models. In Section III we show the motivational experiment. In Section IV we analyze the base, core and global grids. In Section V we describe our workload assignment method, followed by experiments in Section VI and conclusions in Section VII.

II. MODELS

A complete power supply distribution model includes the package and the chip grid equivalent circuits. The package level power distribution model is dominated by inductance. The on-chip power grid is primarily dominated by R and C parasitics. A core is represented by a set of distributed C4s, current sources, and non-switching decaps as shown in Figure 2a.

A non-switching core is represented by the decoupling capacitance, \( C_d \), and the leakage current, \( I_{\text{leakage}} \). The decoupling capacitance includes the capacitance from non-switching circuitry and the intentionally placed decaps. Switching circuits are typically represented by triangular waveforms [5], such as shown in Figure 3a. For simplicity, we refer to various workloads using parameters of the triangular waveform, but in our calculations, we utilize continuous current models. The continuous workload model uses the Weibull distribution function with a period \( T \), peak switching time \( t_s \), peak current \( I_{\text{peak}} \), and leakage current in idle mode \( I_{\text{leakage}} \). Figure 3b illustrates the continuous current waveform model of a workload.

The Weibull distribution function is expressed as:

\[
I_{\text{load}}(t) = \frac{k}{\lambda} \left( \frac{t}{T} \right)^{k-1} e^{-(t/T)^k} + I_{\text{leakage}} \tag{1}
\]

where, \( k \) is the shape parameter that corresponds to \( I_{\text{peak}} \), \( \lambda \) is the scale parameter that corresponds to \( t_s \).

III. MOTIVATIONAL EXPERIMENT

The power supply noise affects the core’s behavior as it causes the performance loss. Various workload distributions in a multi-core system create different power supply noises that result in different performance losses. We demonstrate this by analyzing a 3x3 multi-core system, shown in Figure 2b. Each core is represented by the model presented in Figure 2a.

Each workload is characterized by its current demand, switching frequency, and leakage current. In a multi-core system, the cores may be running similar or different tasks. Some may be high frequency, others may be mid-frequency switching applications. In this experiment, we investigate workloads of various frequencies that represent diverse applications. The workloads available in the SPEC CPU2006 suites [12] exhibit a spectrum of power and performance requirements and correspond to tasks such as video compression, combinatorial optimization, and path-finding algorithms.

We assume that the global power grid of the multi-core system with which we experiment is designed for all cores operational with typical current demand workloads. Parameters of the typical workload (W1) are:

\( \{ T, I_{\text{leakage}}, I_{\text{peak}} \} = \{ 500\text{ps}, 15\text{mA}, 100\text{mA} \} \).

Parameters of the high frequency workload (W2) are:

\( \{ T, I_{\text{leakage}}, I_{\text{peak}} \} = \{ 100\text{ps}, 20\text{mA}, 150\text{mA} \} \).

Parameters of the low frequency workload (W3) are:

\( \{ T, I_{\text{leakage}}, I_{\text{peak}} \} = \{ 3.6\text{ns}, 10\text{mA}, 66\text{mA} \} \).

We estimated the leakage currents to be consistent with the leakage power of each workload.

We measure the distance between cores using the Manhattan metric normalized to the length of the side of a core. The decoupling capacitance available to a core is provided by its neighbors and by the core’s non-switching circuits. We normalize the capacitance to the capacitance provided by an idle core. The core labels correspond to the multi-core system shown in Figure 2b. We use the metric developed in [8] to measure the power supply noise:

\[
PSN_i = \frac{\int_{t_s}^{t_e} (V_{DD} - V_i) \, dt}{t_{e} - t_{s}} \tag{2}
\]

where \( V_i \) is the node voltage and \( t_s \) and \( t_e \) are starting and ending switching times.

First, we investigate the core-core interactions depending on the distance between them. We assign a workload to core 1 and vary the task assigned to the other core. We consider the core-core interaction for high-high, mid-mid, and low-low frequency cores. Figure 4 shows the power supply noise for core-to-core while varying the proximity. We notice that mid-mid frequency workloads have the largest power supply noise, which decreases as the distance between cores increases. Similarly, the power supply noise decreases with proximity for low-low frequency cores. For high-high frequency cores, the power supply noise changes only slightly with proximity. This is due to the parasitic

![Figure 2](image-url)  
(a) Core model and (b) a 3x3 multicore system.

![Figure 3](image-url)  
(a) Discrete triangular-based waveform and (b) continuous Weibull distribution function waveform representations.
effects in the high frequency domain where inductance starts playing an important role. In low frequencies, decaps dominate but their effects are mostly local and rapidly decay when distance between the cores increases.

Next, we investigate the impact of available decap on power supply noise. This experiment is performed using a single operational core at various locations. For example, core 1 has two immediately neighboring cores that can act as decap. Similarly, cores 3, 7, and 9 have two neighbor cores that can act as decap. Cores 2, 4, 6, and 8 have three immediate neighbor cores and core 5 has four neighbor cores to act as decap.

Figure 5 shows the impact of decap on the power supply noise for different frequency workloads. For the same experimental setup we vary the workload frequency and the amount of decap available. The worst case power supply noise always happens at mid frequencies (closer to the resonant frequency), regardless of the amount of decap. The amount of available decap moves the power supply noise curves up or down, as illustrated in Figure 5. From these experiments we draw the following observations:

**Observation 1: Power Supply Noise and Proximity**
Power supply noise (PSN) from one core to the other is inversely proportional to the distance between them. As the proximity between cores increases, the induced PSN decreases, thus the core-core interaction becomes weaker. Additionally, the frequency of the workloads affects the core-core interactions. The power supply noise from two cores, both with high frequency workloads, tends to be the same regardless of their proximity due to the inductive effects present. In low frequencies, the PSN decreases rapidly with increasing proximity due to decap effects. The dependency between PSN and proximity is an important factor in controlling power supply noise during workload assignment. The assignment strategy should take into consideration the proximity between the cores and their operational frequencies.

**Observation 2: PSN and Decaps**
PSN is inversely proportional to the amount of decap. As the amount of decap increases, the power supply noise decreases, thus increasing the noise resilience of the core. This effect is well-known and widely used to suppress the amount of power supply noise. There are various works that investigate decap placement and sizing to control power supply noise on a single core [7]. Figure 5 illustrates this effect. In a multi-core system, the operational core will experience different amounts of decap depending on its location and its neighboring cores’ activities. The neighboring cores can act as decaps to suppress the noise. The assignment strategy should consider these factors.

**Observation 3: PSN and Frequency**
Workload frequency has an impact on power supply noise. We have observed that power supply noise is greater when the workload frequency is closer to the resonant frequency of the system. This is also illustrated in Figure 5. The workloads assigned to cores could differ in their application and switching frequencies, thus some cores will experience greater power supply noise than others. The correlation between the power supply noise and workload frequencies of the cores is shown in Figure 6. For shorter core-to-core distances, in our experiments, for distances less than 2 (normalized Manhattan distance), high-low workload cores have less power supply noise than low-mid workload cores. For distances greater than 2, low-mid workload cores have the least power supply noise. The noise generated by the high-mid and high-low workloads changes slowly with distance due to the inductive effects whereas the noise for low-mid cores decreases more rapidly due to the local decap effects.

We have observed similar effects for several workload assignments with which we have experimented. When all cores are operational with the typical workload $W_t$, the power supply noise is within the allowed margin because the grid was optimized to accommodate such conditions. In the first assignment, cores 1, 2, and 4 are operational. In the second assignment, cores 1, 5, and 9 are operational. We apply various frequencies to the cores and measure their power supply noises on operational cores.

Table 1 shows comparisons of power supply noise for each assignment. Assignment 1 has greater power supply noise
than assignment 2 for the same set of workloads. For example, assignment 1 with workloads \( W_1-W_2-W_3 \) has the greatest power supply noise.

Table 1: Power supply noise comparisons between various assignments and different frequencies.

<table>
<thead>
<tr>
<th>Assignment</th>
<th>Cores Assigned</th>
<th>Workloads</th>
<th>Power Supply Noise (V*ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1-2-4</td>
<td>( W_1-W_2-W_3 )</td>
<td>0.06</td>
</tr>
<tr>
<td></td>
<td>1-2-4</td>
<td>( W_1-W_2-W_3 )</td>
<td>1.98</td>
</tr>
<tr>
<td></td>
<td>1-2-4</td>
<td>( W_1-W_2-W_3 )</td>
<td>2.56</td>
</tr>
<tr>
<td>2</td>
<td>1-5-9</td>
<td>( W_1-W_2-W_3 )</td>
<td>0.06</td>
</tr>
<tr>
<td></td>
<td>1-5-9</td>
<td>( W_1-W_2-W_3 )</td>
<td>1.83</td>
</tr>
</tbody>
</table>

These observations motivate us to study the impact that workload assignments have on the power supply noise and to propose a power supply noise aware assignment strategy to minimize the power supply noise generated.

In the next section, we analyze of the global grid to capture the effects of proximity between cores, available decap, and workload frequency.

IV. GRID ANALYSIS

In this work, we assume that power delivery for a multi-core system consists of a power mesh with C4s, current sources, and decaps distributed on the grid. Each core is replicated many times to model the whole multi-core system structure as shown in figures 2a and 2b.

Each core consists of several blocks. Each block corresponds to a circuit bounded by a rectangle whose corners are C4s. The base grid is a 2x2 grid between the neighboring C4s along with the current sources representing the circuit and decoupling capacitances. The core grid can be viewed as a collection of connected base grids. For example, a core can have many blocks such as cache, cpu, alu and decoders/drivers. We decompose the core grid into smaller grids while maintaining the system’s behavior. Performing such decomposition allows us to analyze each base grid separately and to reuse the results to analyze the core and the whole global grid. Figures 7a and 7b illustrate the base and core grids. The black dots on the grid represent C4s. In this section, we perform detailed analyses of the base, core, and global grids.

IV.1 Base Grid Analysis

In this study, we assume the current sources and decoupling capacitances in a core grid are uniformly distributed over the core nodes. The decoupling capacitances of the base grid are extracted from the corresponding circuits. Decaps are split proportionally among the neighboring bases. Current sources on the boundaries are treated similarly. Our analysis is also valid for non-uniform distribution of decaps and current sources. We assume their uniformity to simplify the explanation.

![Fig. 8. (a) A 2x2 base grid; (b) simplified circuit for analyzing node 5.](image)

For the same reason, we also assume that a core grid includes four connected base grids. This analysis is valid for those cases with more than four base grids per core. We reduce the base grid to a single node. As shown in Figure 8a, the center node, 5 will have the greatest amount of voltage drop. Since our objective is to estimate the grid noise, we are interested in the node voltage on node 5.

The simplified circuit is shown in Figure 8b. Node \( r \) represents the reduced circuit node. The circuit resistance \( R \) is determined from the delta-wye conversion of the impedances of the initial base grid, and \( C_{\text{eff}} \) is the effective capacitance from the neighboring nodes that are seen at node 5. The capacitance \( C \) is the decap available at node 5. To obtain \( C_{\text{eff}} \) we solve the base grid by applying the modified nodal analysis. The node voltages for the actual base grid can be expressed as:

\[
V_{\text{base}} = I_{\text{loads}},
\]

where \( G \) is the conductance matrix for the base grid structure and \( I_{\text{loads}} \) is the vector of current sources on the base grid.

Given that node 5 would have the greatest amount of voltage drop, we have

\[
V_5 = \min(V_{\text{base}}) = \min(G^{-1} \cdot I_{\text{loads}}).
\]

Because we are focusing on capturing the worst case voltage drop, investigating the node voltage at node 5 is sufficient. We introduce a simplified circuit, shown in Figure 8b, where the node voltages at node \( r \) and node 5 in the actual base circuit are equal. The main idea is to have a simplified circuit to represent the worst case voltage drop of the base grid. Thus, in order to maintain the behavior of the actual core in the reduced model for the worst case voltage drop, the node voltage of the reduced circuit must represent the node voltage of the actual circuit, i.e. \( V_5 = V_r \).

The reduced circuit shown in Figure 8b has \( C_{\text{eff}} \) as the only unknown parameter, where \( L \) is the package inductance, \( I_{\text{load}} \) is the extracted current source, and \( C \) is the decap available at node 5. The parameter \( C_{\text{eff}} \) is derived by solving the node voltage equation for node \( r \) in the s-domain:

\[
sC_{\text{eff}} = \frac{I_{\text{load}}}{V_r} \frac{V_r - V_{dd}}{(sL + R)V_r} - sC
\]

where inverse Laplace transforms are taken for \( I_{\text{load}} \) and \( V_{dd} \) to obtain the solution for \( C_{\text{eff}} \). In this manner, we com-
pute the amount of decap that is contributed from the neighboring nodes to the node of interest. We note that $C_{eff}$ will vary in value depending on the workload ($I_{load}$) frequency and switching activity, as shown in figures 9a and 9b. We observe that $C_{eff}$ decreases exponentially with current frequency and linearly with switching activity.

**Figure 9.** (a) $C_{eff}$ as a function of current frequency and (b) $C_{eff}$ as a function of switching activity.

### IV.2 Core Grid Analysis

The core grid consists of several connected base grids. Figure 7b shows a circuit representation of the core grid. We use the models and analysis of the base grid to derive the node voltages of the core grid.

<table>
<thead>
<tr>
<th>Vdd</th>
<th>$R_{base1}$</th>
<th>$R_{12}$</th>
<th>$R_{13}$</th>
<th>$R_{24}$</th>
<th>Vdd</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>L</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Fig. 10. Core model with simplified base models.

The core grid consists of several connected base grids. Each base can be represented by its simplified model, as shown in Figure 8b. Bases are connected through the shortest paths impedances between them. Impedances $R_{12}$, $R_{13}$, $R_{24}$, $R_{34}$ represent the local power grid branches between bases 1, 2, 3, and 4. Such a representation simplifies the core grid structure and its analysis. Figure 10 shows the core grid with the base models. We assume that when a core is operational all its bases are operational with the same frequency as that of the workload assigned to it. We utilize the core model from Figure 10 to derive analytical formulas for the node voltages on the core grid. We express them in terms of the node voltages derived from the base grid analysis. The current for the base grid in the s-domain is as:

$$
V_{base} - V_{dd} = \frac{V_{base}}{sL + R_{base} + 1/(sC_{base})} = I_{load},
$$

where $C_{base} = C_{d} + C_{eff}$, and $R_{base} = R_{ij}$. For a core grid with simplified base grid models, the node voltage at any node can be expressed as:

$$
V_{core} - V_{dd} = \frac{V_{core}}{sL + R_{base} + 1/(sC_{base})} + \frac{V_{core} - V_{core}}{R_{ij} + R_{ik}},
$$

where $i=1$ to $4$.

Combining equations 4 and 5, we express the core node voltage in terms of the base node voltages as follows:

$$
\frac{V_{core}}{sL + R_{base} + 1/(sC_{base})} + \frac{V_{core}}{sL + R_{base} + 1/(sC_{base})} = \frac{V_{base}}{sL + R_{base} + 1/(sC_{base})} + \frac{V_{base}}{sL + R_{base} + 1/(sC_{base})} = I_{load},
$$

where, for a 4-base core, the matrices $A$ and $B$ are of size $4\times4$, and $V_{core}$, $V_{base}$ are $4\times1$ vectors. The matrices $A$ and $B$ represent the conductance parameters for the core and base grids derived from Eq 6. $V_{base}$ is derived as explained in Section IV.1. We have already derived the solution for $V_{base}$, thus, the node voltages on the core are expressed as:

$$
V_{core} = A^{-1} \cdot B \cdot V_{base} = P \cdot V_{base}
$$

This equation is valid assuming that all bases on the same core are operational with the same switching frequency. In the case of various frequencies, we need to apply the superposition of the frequency response for each. We further simplify the core model to include only a single node voltage. To do this, we need to know the amount of decap available on a core. We use the reduction technique described in Subsection IV.1.

The single node represents the minimum node voltage of the core. Thus, $V_{core} = V_{core} = \min(V_{core}) = \min \left\{ \sum_{i=1}^{4} p_{ij} \cdot V_{base} \right\}$, where $i=1$ to 4.

The simplified core model is shown in Figure 11. It has only one current source representing the current demand and frequency of the workload assigned to it. The simplified model has also one decoupling capacitor, which represents the amount of decap available in the core. The package model is represented by the inductance $L$. The impedance $R$ is derived from the delta-wye conversion of the impedances in the circuit illustrated in Figure 10. The only unknown parameter of the model is the amount of decap $C_{d}$ of the core, where $I_{load}$ and $V_{core}$ are known. The $C_{d}$ combines the decap available on a given base and the amount of decap available from the neighboring bases. The $C_{d}$ of the simplified model is derived from analytical equations for the circuit, shown in Figure 11. As described in Subsection IV.1, in order to maintain the same system behavior between the simplified core model and the actual core circuit, we maintain the equality $V_{k} = V_{core}$. From KCL on the simplified core model we have:

$$
\frac{V_{core} - V_{dd}}{sL + R} + \frac{V_{core}}{1/sC_{d}} = I_{load}
$$

From Eq 9, we derive an analytical formula for decap:
We note that inverse Laplace transforms are computed for $I_{\text{load}}$ and $V_{dd}$ in Eq 10 to derive $C_{d}$.

\[
sC_d = \frac{I_{\text{load}}}{V_{\text{core}}} = \frac{V_{\text{core}} - V_{dd}}{(sL + R)V_{\text{core}}}
\]

(10)

We formulate two workload assignment problems.

**Problem 1**: Given $m$ workloads, and a global grid of $n \times n$ cores with all cores initially idle, decide how to assign the workloads such that a minimum PSN is generated.

**Problem 2**: Given $m$ workloads, and a global grid of $n \times n$ cores with an initial assignment of working cores, decide how to assign the $m$ new workloads without reassigning the previously assigned cores and such that a minimum PSN is generated. We propose four assignment strategies.

### IV.3 Global Grid Analysis

We perform global grid analysis considering the base and core node voltages as derived in the previous subsections. We choose to represent the global power grid using Eq 2.

We further utilize the simplified core model for the global grid. The global node voltages are expressed by superposition as:

\[
V_g = V^{\text{wh}}_g + V^{\text{wm}}_g + V^{\text{wl}}_g + V^o
\]

(12)

where $V^o$ is the initial condition voltage. Eq 12 can be as:

\[
V_g = H^{\text{wh}}U^{\text{wh}} + H^{\text{wm}}U^{\text{wm}} + H^{\text{wl}}U^{\text{wl}} + V^o
\]

(13)

where $H^{\text{wh}} = (Q^{\text{wh}})^{-1}$, $H^{\text{wm}} = (Q^{\text{wm}})^{-1}$, $H^{\text{wl}} = (Q^{\text{wl}})^{-1}$.

For each individual core, the global voltage is expressed as:

\[
V_{gi} = \sum_{j=1}^{n} h^{\text{wh}}_{ij}V^{\text{wh}}_j + \sum_{j=1}^{n} h^{\text{wm}}_{ij}V^{\text{wm}}_j + \sum_{j=1}^{n} h^{\text{wl}}_{ij}V^{\text{wl}}_j + V^o
\]

(14)

Using Eq 14, we are able to express the core voltage in terms of the frequency response for each frequency group. Coefficients $h_{ij}$ capture the impact that core $i$ has on core $j$ at any of the frequency groups, $\text{wh}$, $\text{wm}$, or $\text{wl}$. We use these coefficients in deciding how to assign workloads to minimize the power supply noise caused by the core-to-core interaction. Even though applying the frequency grouping would introduce some inaccuracy in the frequency response of the multi-core system, the analytical formulas provide sufficient accuracy and capture the trends of the frequency response and the generated power supply noise. The node voltage equations for the global grid can also be expressed in terms of the base and core node voltages as derived in the previous subsections. We choose to represent the global node voltages in terms of the current sources such that we derive $h_{ij}$ coefficients that effectively capture the core-to-core interactions.

The simplified core model for global grid analysis significantly reduces the complexity of the problem. The size of the matrix that needs to be solved for the global grid analysis is directly proportional to the number of cores. We measure the amount of power supply noise on the global grid using Eq 2.
V.I Simulated-Annealing-Based Assignment

Both problems can be solved using a simulated-annealing-based algorithm. Simulated annealing is a well-known optimization technique widely used for various applications. We apply simulated annealing to explore the trade-offs between power supply noise, performance, and workload assignments. The assignment vector \( x_i \) for problem 1 has all its elements as variables, whereas in problem 2, the vector \( x_i \) has some fixed elements due to the initial, existing assignment. The evaluation function is the power supply noise obtained by using the node voltages expressed by Eq 14 and the noise metric given by Eq2; the cooling rate is set as \( T_{k+1} = T_k \cdot CR^2 - 1 \), where \( CR=0.92 \) and \( k \) is the cooling step in the loop. For each temperature step, equilibrium is reached if there is no more change in the power supply noise for a perturbed assignment configuration.

VII Assignment Heuristics

We utilize our observations and analyses to formulate the workload assignment algorithms based on quantitative reasoning. Based on our observations of several examples, we have the following classifications and rules:

1. There are three kinds of workloads -- \( H \) for high frequency, \( M \) for mid frequency, and \( L \) for low frequency.
2. Based on their switching activities we further refine the workloads as \( \{H_1,H_2,H_3\} \), where each of them represents the switching activities of 0.2, 0.3, and 0.4, respectively. A switching activity of 0.3 means that, on average, in every clock cycle 30% of the core’s transistors switch. Similarly, we define \( \{M_1,M_2,M_3\} \) and \( \{L_1,L_2,L_3\} \).
3. We first assign the mid, then the high, and finally the low frequency workloads based on the amount of power supply noise they generate.
4. The core-core interactions are ordered from the strongest to the weakest as \( H-M, M-M, M-L, H-L, H-H, \) and \( L-L \). Thus, high and mid frequency workloads should be placed further apart to reduce their interactions whereas the low-low frequency workloads can be placed close to each other without a significant power supply noise penalty.

The quantitative assignment (QA) strategy summarized as:

1. Place \( \{M\} \) workloads far apart from each other to weaken M-M core interactions
2. Place \( \{H\} \) workloads far away from previous workloads to weaken H-M core interactions
3. Place \( \{L\} \) workloads far away from previous workloads to weaken M-L core interactions

Fig. 14. Quantitative assignment.

We also introduce two other assignment algorithms based on geometric distance and the amount of current consumed by the cores. In geometric assignment (GA), the summation of inter-core distances is maximized. Current demand-based assignment (CDA) is based on the amount of current drawn by the cores. Cores with large current workloads are assigned far away from each other to minimize the core-core interaction.

VI. RESULTS

We have implemented the assignment algorithms and tested them on a set of circuits. The circuit parameter values were taken from [9]. We consider the power delivery in 90 nm technology with \( V_{dd} = 1 \) V. We compare our simulated-annealing-based assignment (SABA) with the QA, GA, and CDA algorithms in terms of power supply noise. The initial global power grid is designed to satisfy the voltage drop and current density constraints when all cores are operational with their current demand \( I_{average} \). In this work, we assume that all the cores are identical and any workload can be assigned to any core. We study the assignment problem for different workload distributions and grid configurations. In our experiments, we assumed that up to 50% of the cores can be operational at any time.

1. Impact of core granularity

Several 3x3, 4x4, 5x5, and 10x10 multi-cores were tested for the same workloads to study the effects of core granularity on the assignment. The assignment was tested on problems 1 and 2 described in Section V. Table 2a shows the results for problem 1 and Table 2b shows the results for problem 2. In all tables, the percentages of PSN describe the power supply noise increase for the GA, CDA and QA algorithms with respect to the SABA algorithm.

<table>
<thead>
<tr>
<th>Core Granularity</th>
<th>Power Supply Noise*</th>
<th>% PSN Increase</th>
</tr>
</thead>
<tbody>
<tr>
<td>GA CDASAQA GA CDASAQA GA CDASAQA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( 3 \times 3 )</td>
<td>1.90 2.3 2.44 2.27</td>
<td>31.65% 30.53% 19.47%</td>
</tr>
<tr>
<td>( 5 \times 5 )</td>
<td>3.19 3.58 3.3</td>
<td>36.76% 36.01% 15.45%</td>
</tr>
<tr>
<td>( 7 \times 7 )</td>
<td>2.4 2.76 2.62</td>
<td>31.66% 29.77% 12.34%</td>
</tr>
<tr>
<td>( 10 \times 10 )</td>
<td>2.2 2.28 2.54</td>
<td>22.73% 20.81% 9.45%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Core Granularity</th>
<th>Power Supply Noise*</th>
<th>% PSN Increase</th>
</tr>
</thead>
<tbody>
<tr>
<td>GA CDASAQA GA CDASAQA GA CDASAQA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( 3 \times 3 )</td>
<td>2.0 2.47 2.60 2.49</td>
<td>23.30% 24% 22.35%</td>
</tr>
<tr>
<td>( 5 \times 5 )</td>
<td>2.06 2.65 2.64 2.62</td>
<td>27.49% 26.54% 26.44%</td>
</tr>
<tr>
<td>( 7 \times 7 )</td>
<td>2.25 2.30 2.30 2.30</td>
<td>31.84% 27.32% 20.44%</td>
</tr>
<tr>
<td>( 10 \times 10 )</td>
<td>2.31 2.34 2.34 2.31</td>
<td>33.75% 33.17% 27.82%</td>
</tr>
</tbody>
</table>

2. Impact of workloads

Several workloads were tested to study their impact on the noise. The workloads have different current demands and switching frequencies. We experimented with the workloads \( W_1, W_2, W_3 \) described in Section II. The results are shown in Table 2c.

3. Impact of core size

We study three different core sizes: a small, medium, and large. In our experiment, a small core consists of a single base grid, a medium sized core consists of four base grids, and a large core consists of nine base grids. We apply the
same workload to each core. We assume that execution of a workload consumes the same amount of charge regardless of the core size. The base grids are the same for all core sizes. Figures 15a and 15b show the power supply noise versus frequency and switching activity for various core sizes. Large core sizes lead to less performance loss due to available decap.

We observed that CDA algorithm results in the greatest power supply noise. We also observed that QA gives better results than GA and CDA. This is because QA takes into account the frequency and proximity between cores. QA does not capture all the nuances of core-core interactions and is not as good as SABA. However, QA can be a good starting point for further optimization. We also observed that the initial assignment of working cores plays a significant role in the power supply noise of the system. The power supply noise of a multi-core system with no initial assignment is less than when an initial assignment exist. This is because an initial assignment provides restrictions on the possible placements of workloads. Such differences can be observed in Tables 2a and 2b. The simulated-annealing-based optimization method produces much less power noise as it takes into consideration decap availability and noise propagation between the cores. The GA algorithm considers only the geometric distance that reduces noise propagation but it cannot utilize possible trade-offs. We also observe that the amount of charge consumed by simultaneously executed workloads has an impact on performance loss. Larger and more frequent current demands create greater noise. In Figure 16a, we show the best workload assignments for a 5x5 multi-core system determined by each algorithm. To calibrate the quality of solutions determined by each of the algorithms, we show the power supply noise for all configurations in Figure 16b. On the x-axis are all possible assignment configurations sorted by increasing grid noise. We observe that power supply noise for the SABA algorithm indeed produces a high quality solution whereas other algorithms are quite far from the optimum.

VII. CONCLUSIONS

In this paper, we demonstrated that workload assignment affects the system’s overall performance. Workload frequency, core activity and the amount of decap play an important role on the amount of power supply noise. We developed metrics to capture the power supply noise, effective capacitance, and core-to-core noise propagation. We developed a power supply noise aware assignment strategy and show that our algorithm is efficient and achieves better results than those obtained by geometric, current dependency, and quantitative assignment algorithm.

VIII. ACKNOWLEDGEMENT

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REFERENCES


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