Abstract—This paper describes an alternate method to Monte Carlo for calculating circuit node voltage and branch current variances due to random process variability. Recent results show that the complex models traditionally used to describe random process variations of a transistor can be replaced by a single independent current noise source with a variance dependent on the transistor’s size and operating points. As a result, each transistor affected by random process variability can be modeled as a deterministic device in parallel with a current noise source. By replacing all the transistors in a circuit with this model, the spatial voltage variances of circuit nodes can be calculated through linear small-signal analysis. The idea is presented in this paper and a tool implemented for Berkeley SPICE is described. The results of the variability SPICE tool match the results from Monte Carlo run in SPECTRE, with an accuracy determined by the accuracy of the random process variability model. For example, the standard deviations computed by the tool are within a 5.0% accuracy of those calculated through measured silicon data which has a fitting error of 5.4%. The Monte Carlo method computes node variances in a time proportional to the number of circuit nodes and the number of iterations, whereas the computation time required by the variability tool is only a function of the number of circuit nodes. For large analog designs this results in a significant speed-up in the amount of time required to calculate circuit node variances.

I. INTRODUCTION

In present literature, almost all statistical information about the effects of random process variability on circuit performance is obtained through Monte Carlo simulations [1], [2]. Monte Carlo works by repeatedly running the same simulation with varied parameter values chosen from a user-specified distribution. The results of Monte Carlo are stochastic and in order to obtain statistical accuracy one needs to run upwards of thousands of simulations which can be very time-inefficient. In recent years some non-Monte-Carlo based methods for analyzing the effects of random process variability have been made in the analog space using the PNOISE function in RF simulators [3] and in the digital space through Stastical Static Timing Analysis. Similarly, for applications where the variable of interest is the voltage or current variance due to random process variability, a simple and fast noise analysis method can be employed to calculate the variance.

The method we will describe models the DC effects of random process variability on individual transistors, exhibited as DC current variation, as an independent random variable described by a Gaussian distribution. A small-signal analysis is then performed to calculate the effects of the variability noise generated by each transistor on the output node. This analysis linearizes the circuit about a bias point and calculates the transfer function from the input of the noise source to the desired output node. Under the assumption that the RMS values of the variability noise sources are smaller than the maximum amplitude allowed to maintain linearity of the circuit, linearization is a valid technique for calculating the output variance. Due to the independence of the variability noise sources the output variance can be computed by summing the contribution of each transistor’s random process variability noise source. The computed variance does not describe the variance of a unique fabrication of a circuit over time but rather describes the variance of multiple instances of a circuit over space as random process variability results in spatial rather than temporal differences.

We have developed an add-on variability analysis for Berkeley SPICE [4] that calculates the standard deviation of desired node voltages and branch currents due to random process variability. A comparison of measured silicon results from a 65-nm bulk CMOS process to calculated results from the SPICE simulation tool shows that for a fixed-current device, a topology of many small transistors in parallel results in less variance than a single large transistor. This is contrary to the $1/\sqrt{WE}$ generalization that equates larger transistors with smaller standard deviations. As another design example we will study design tradeoffs for a standard differential pair amplifier and compare the variances computed by the Monte Carlo method to the results of the SPICE simulator. The variability noise simulator predicts the voltage variances of the differential amplifier with an error of 5.6% at the high-gain node in a fraction of the computation time required by Monte Carlo.

This paper is organized as follows. Section II formally introduces what we refer to in this paper as variability noise. The model to describe the noise source is presented. Section III is an overview of the changes made to SPICE to accommodate the variability analysis. Section IV presents two design examples and the paper concludes with Section V.

II. VARIABILITY NOISE MODEL

Within the design community the term “noise” typically refers to electrical noise in integrated circuits such as shot noise or thermal noise. A method to calculate the effects of these electrical noise sources has been established and used in analog design for decades [5]. With the appropriate modeling, these pre-existing noise calculation techniques can also be used to analyze the DC effects of random process variability on a circuit. The requirements on the model used to describe the random process variability are that the sources of variability must be completely expressed as a combination of current and voltage sources and these generators must describe the current variation with high fidelity. This section describes how
transistor variation due to random process variability can be interpreted as a single current noise source. In this paper, the noise will be referred to as variability noise.

The underlying mechanisms that cause random process variability have been studied for decades [6], [7]. Some physical explanations for the stochastic nature of transistors are fluctuations in the doping of the channel and gate, in the surface-roughness scattering, and in the oxide charge. These microscopic physical events manifest themselves as a difference in transistor DC current as measured over space. Conventionally, variations in transistor current measurements are used to quantify the assumed Gaussian distribution of variation-dominant transistor model parameters $V_T$, $L$, and $\mu_0$ [8]. This commonly used description of current variation has a disadvantage for noise analysis in that it is not in a form that can be naturally converted to equivalent voltage and current sources.

A new method of modeling random process variability based solely on measured current points was introduced in [9] and was shown to model the current variations with high accuracy. Our approach was to model the current variation due to random process variability as a single independent current source. The key idea behind this new model is that the distribution of current in the linear and saturation operating regions are tested with high probability to have come from a Gaussian distribution. This allows the current variations due to random process variability to be easily modeled without curve-fitting I-V points. The current can be described by an average current ($I_{avg}$) equation and a variance current equation. The equation for $I_{avg}$ can be chosen based on the accuracy needs of the application.

The complete current variance equation is,

$$\sigma^2 = \frac{\Delta I_{avg}^2}{I_{avg}^2} = \left( \frac{A}{W^{\alpha}L^{\beta}V_{gs}^{\eta}V_{ds}^{\zeta}} \right)^2$$

Fig. 1. $\mu$ measured vs. modeled for transistors of different sizes. The widths range from 120 - 500nm and the lengths from 60 - 120nm. Operating points range from 0.5 V $\leq V_{gs} \leq$ 1.0 V and 0.2 V $\leq V_{ds} \leq$ 1.0 V.

and $\alpha$, $\beta$, $\eta$, $\zeta$, the exponents of the design variables, $W$, $L$, $V_{gs}$, and $V_{ds}$, are necessary to describe the current variance of all operating points in the linear and saturation region. With this simple equation, it is possible to describe the variability noise as a single current noise source between the transistor drain and source with a RMS value equal to the square root of the cumulative form of the standard deviation of DC current of Eq. (1) multiplied by the average current. While there is no concrete physical explanation for the form of the model, this model has exhibited high accuracy when compared to measured silicon results from a 65-nm bulk process as it fits the current variations of more than 200,000 transistors from across 60 dies with a 5.4% RMS error as shown in Fig. 1. For the measured data the exponents associated with the design variables $W$, $L$, $V_{gs}$ and $V_{ds}$ are $\alpha = 0.3$, $\beta = 0.8$, $\eta = 2.1$ and $\zeta = 0.15$, respectively. This model is a cumulative description of the effects of all the process parameters which can be classified as spatial “white noise” variations. We know that these parameters have a standard deviation dependent on $\sqrt{W/L}$ [7]. Given that DC current is not solely a linear function of spatial “white noise” parameters we expect that the cumulative form of the standard deviation of DC current will exhibit different exponents for the size and operating point variables when compared to the conventional model.

The relative values of the exponents indicate that tuning $V_{gs}$ is the most effective way to reduce current variations. Results also show that under fixed bias point conditions the current variation is much more sensitive to changes in transistor length than width. In our simulation tool, we will use this model to calculate the RMS of circuit node voltage variance and branch current variance.

III. SIMULATION TOOL

The method we will describe to calculate circuit node variances due to variability noise is general and can be written for any modern circuit simulator. We chose to write it for the Berkeley SPICE simulator due to its public availability. The variability tool has been implemented specifically for the BSIM4 [10] model. In order for SPICE to perform the analysis a variability analysis card must be added. The variability card takes advantage of the circuit simulator’s small-signal analyzer which is typically used for calculating circuit electrical noise, gain, or bandwidth, and uses the same functions to calculate voltage variances due to random process variability. The exponents of Eq. (1) are hard-coded into this card. The analysis begins by first calculating the nominal DC bias of the circuit, with only the nominal transistor current. Then each transistor is modeled as shown in Fig. 2a by a deterministic transistor in parallel with a sinusoidal current noise source of RMS value,

$$\sqrt{\sigma^2} = I_{avg} \cdot \sigma \Delta I_{avg}. \quad (2)$$

The contribution of each transistor to the output node variance is determined by linearizing the circuit around its nominal bias point and then finding the transfer function between the terminals of the offending noise source and the output. The transfer function is expressed as a complex number but since
the input noise source is a RMS value, all phase information contained in the transfer function is unnecessary. The absolute value of the transfer function squared is multiplied to the square of the RMS value of the input variability noise source to find the contribution at the output. Since the input variability noise sources are independent, statistical addition allows us to add the variance contribution of each transistor to the output node \( V_{out} \) to get the total output variance,

\[
\sigma_{V_{out}}^2 = \sum_{k=1}^{N} I_{vk}^2 \cdot \left| \frac{V_{out}}{I_{in_k}} \right|^2. \tag{3}
\]

The dimensionality \( (N) \) is determined by the number of variability noise sources in the circuit. The variable \( in_k \) is the input terminal of the \( k \)-th variability noise source. This computation is done using the adjoint matrix method [11] which allows us to add uncorrelated noise sources to be considered without making circuit simplifications.

In order for the user to call the variability analysis a .var statement must be added to the netlist, shown in Fig. 2b. The argument to the .var statement is a list of nodes for which the variance is to be computed. The output of the variability analysis is a table containing the variances of the desired nodes and the RMS values of the contribution of each transistor in the circuit to the output. This list indicates to the designer which transistors contribute most to the output variance. This tool can also calculate the effects of the variability noise across different process corners by adding an additional parameter to the .var option which specifies the desired corner.

IV. DESIGN EXAMPLES

To use the simulation tool the five constants \((\alpha, \beta, \eta, \zeta, C_{on})\) that describe the variability noise are required. They can be found most accurately through silicon measurements. When silicon is not available the constants can be determined by using a circuit simulator. The simulator runs a Monte Carlo simulation of I-V curves of varying transistor sizes and fits the results to the variability noise model. The RMS error of the variability noise model will be larger for data obtained by the simulated Monte Carlo approach. This is due to the simplistic mismatch models embedded into the technology model file. In this section we will present two design examples and compare results from measured silicon and simulated by Monte Carlo to the results of the variability analysis tool added to SPICE.

A. Current Source

The current source is an important element in almost all analog designs. Using the variability noise model we will investigate size versus current variance tradeoffs for specific current source topologies. Figure 3 shows two different topologies for the same nominal current source. In the following analysis, the assumption is that \( V_{gs} \) and \( V_{ds} \) of both circuits are equal and that a transistor of width \( 2W \) has twice the drive strength of a transistor of width \( W \). The variance of \( I_1 \)

\[
\sigma_{I_1}^2 = \left( \frac{A}{(nW)^\alpha L^3 V_{gs}^q V_s} \right)^2. \tag{4}
\]

Since the current variability noise is independently identically distributed, the variance of \( I_2 \) is

\[
\sigma_{I_2}^2 = \sum_{i=1}^{n} \left( \frac{I_{on}}{n} \right)^2 \left( \frac{A}{W^\alpha L^3 V_{gs}^q V_{ds}^q} \right)^2. \tag{5}
\]

The ratio of the current variances is

\[
\frac{\sigma_{I_1}^2}{\sigma_{I_2}^2} = n^{(1-2\alpha)}. \tag{6}
\]

Figure 4 shows a plot of the ratio of the variances vs. \( \alpha \), the exponent of \( W \). Using traditional approximations where \( \alpha = 0.5 \), the ratio of the current variances is 1 which indicates that either sizing scheme would result in the same variance at the output. For values of \( \alpha < 0.5 \), lower output variance is obtained by sizing the current source as a set of parallel minimum-width devices. For technologies associated with an \( \alpha \) value greater than 0.5, lower output variance is obtained

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**Fig. 2.** Variability model.

**Fig. 3.** Current source topologies.

**Fig. 4.** Current source current-variance ratio.
by doing the opposite and sizing the current source as one large device. From measured silicon we calculated $\alpha$ for a 65-nm technology to be 0.3. This indicates that a topology containing smaller devices in parallel is best for reducing output current variance for a current source with a fixed average value. Intuitively, increasing the width of a transistor has two effects. The larger physical size decreases the variance but simultaneously it increases the nominal average current which increases the variance by a square factor. Therefore, increasing the width is only appropriate if these two factors result in a net decrease. This is only true when $\alpha < 0.5$. A similar analysis can be done for the length, where one transistor of width $W$ and length $L$ is compared to $n$-parallel transistors of width $W$ and length $nL$. The resulting current variance ratio is

$$\frac{\sigma^2_{I_{\text{single}}}}{\sigma^2_{I_{\text{parallel}}}} = n^{(1+2\beta)}.$$ \hspace{1cm} (7)

As long as $\beta$ is positive it is always better to have parallel devices of larger lengths than one single device of a smaller length. In all technologies $\beta$ has a positive value. For the 65-nm technology in this example $\beta$ was calculated to be 0.8.

Our simulator is validated by measured data. Data from a 65-nm bulk CMOS test chip was collected for transistors of the same cumulative width, 0.5 $\mu$m, but implemented with either one or two fingers. The two transistors were spatially located next to one another on the die. The SPICE variability simulator calculated the relative current variance to be 1.32 and is indicated as the intersection between the solid vertical line and the $n = 2$ curve in Fig. 4. Also plotted are the measured relative variances for each of the 60 operating point biases. Since the current variance equation is not dependent on the transistor operating point, all 60 operating points measured should coincide. The measured results and the results calculated by the SPICE tool have a RMS error of 5.0% which is within the modeling accuracy of 5.4%.

These findings are counterintuitive to traditional sizing approaches for optimal variance. The finger analysis shows that any correlation of random process variability through the shared diffusion is not significant and variability noise analysis can still be applied with reasonable accuracy. The results also support the analog layout rule-of-thumb that suggests using many fingers for large transistors to reduce mismatch. For technologies with $\alpha \leq 0.5$ using minimum-width fingers to compose the larger transistor will achieve the lowest variance.

### B. Differential Amplifier

To further demonstrate the capabilities of our variability noise simulator, we will calculate the voltage variance of an NMOS-input differential amplifier with a PMOS current-mirror load. The schematic is shown in Fig. 5. To show how this tool can be useful in present design environments we used the simulated Monte Carlo approach to calculate the exponents of a different 65-nm bulk CMOS process. As shown in Fig. 6 the RMS error is 12.65% for NMOS in the TT corner. The model for the PMOS devices has a RMS error of 14.32% in the same process corner. It is interesting to note that $\alpha > 0.5$ for this technology. This is due to the $1/\sqrt{W L}$ dependence in the equation for current mismatch embedded into the circuit simulator. This highlights the importance of an appropriate model. The $1/\sqrt{W L}$ relationship sits at a sensitive point in optimization problems where slight perturbations can cause different conclusions to be drawn. The errors from the Monte Carlo approach are much larger than the calculated RMS error from the measured data shown in Fig. 1. This is expected and is due to the simplistic nature of the simulator mismatch model used to generate the points.

The differential amplifier uses small devices and has a DC gain of 10.3. The first method used to calculate the voltage variances of all the nodes in the circuit is a 5000-sample Monte Carlo analysis in SPECTRE. The data from the Monte Carlo simulation was then used to calculate the voltage variance of the nodes. The second approach was the use of the SPICE variability tool. Table I shows the standard deviation calculated through both approaches. At the high-gain node there is an error of 5.6% which is within the accuracy of the variability noise model. The output of the simulator also indicates the contribution of each transistor to the total voltage variance of the desired node and is shown in Table II. These results indicate that the input differential pair has about 36× more
TABLE I
STANDARD DEVIATION DUE TO RANDOM PROCESS VARIABILITY.

<table>
<thead>
<tr>
<th>Node</th>
<th>Monte Carlo (mV)</th>
<th>SPICE tool (mV)</th>
<th>Difference (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>4.7</td>
<td>4.2</td>
<td>11.0</td>
</tr>
<tr>
<td>B</td>
<td>9.4</td>
<td>9.4</td>
<td>0</td>
</tr>
<tr>
<td>C</td>
<td>10.0</td>
<td>9.4</td>
<td>6.0</td>
</tr>
<tr>
<td>$V_{out}$</td>
<td>167.7</td>
<td>177.2</td>
<td>5.6</td>
</tr>
</tbody>
</table>

TABLE II
CONTRIBUTION TO OUTPUT VOLTAGE STANDARD DEVIATION.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Size ($\mu$m)</th>
<th>Contr. to output $\sigma$ (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_0$</td>
<td>0.99/0.12</td>
<td>123.7</td>
</tr>
<tr>
<td>$M_1$</td>
<td>0.99/0.12</td>
<td>121.2</td>
</tr>
<tr>
<td>$M_2$</td>
<td>1.2/0.3</td>
<td>26.2</td>
</tr>
<tr>
<td>$M_3$</td>
<td>1.2/0.3</td>
<td>22.7</td>
</tr>
<tr>
<td>$M_4$</td>
<td>2.4/0.3</td>
<td>5.3</td>
</tr>
<tr>
<td>$M_5$</td>
<td>2.4/0.3</td>
<td>4.5</td>
</tr>
</tbody>
</table>

The contribution to the output voltage ($V_{out}$) variance compared to the next most dominant pair of transistors, the PMOS loads. This information provides insight as to which transistors to upsize to minimize the total variation.

The tool also allows for efficient investigation of the various tradeoffs between size, variance, and DC gain of the differential amplifier. Table III shows different sizing and operating points for the differential amplifier and its associated output voltage standard deviation and power consumption. For a fixed current, as the size of the input differential pair decreases, $V_{cm}$, the common-mode voltage at the differential input, must increase to provide enough overdrive. In response, the DC gain of the amplifier will decrease. The output voltage variance is a function of both the transistor sizes and the amplifier gain. Design decisions should be chosen based on the context with which this amplifier is used. For example, if this amplifier were to drive a high-gain common-source output stage we would desire a low voltage variance at the output to minimize the gain variation of the second stage which would drive our design choices towards larger transistor sizes and a low $V_{cm}$.

This method of analyzing random process variability allows a designer to quickly obtain relevant statistical information. For a fixed circuit topology a Monte Carlo method has a time-cost which is linearly dependent on the number of samples run, whereas the variability noise tool requires close to constant time to gather the same statistical information. For analog designers this information is very useful for making better variability-aware design decisions. By knowing the variance of important nodes the designer can potentially meet the same performance requirements without having to overdesign.

V. CONCLUSIONS

We have presented an alternate method to Monte Carlo for computing spatial circuit variances due to random process variability. This approach is feasible because random process variability can be accurately modeled as a single independent current noise source. We have added the linear variability analysis to the Berkeley SPICE simulator with the advantage of decreased computation time compared to Monte Carlo, while still obtaining the same accuracy. This work shows a 5.0\% RMS error between the values computed by the tool and measured silicon data. This tool can be used to study area and yield tradeoffs for different circuit topologies as we showed through our analysis of the differential amplifier.

Design decisions are very circuit-dependent and a tool that quickly shows the contributions to, and total variance of, desired output voltages and currents will allow a designer to make quicker design decisions. An extension of this work is to include a dynamic method of linearizing the small-signal gain so that this approach is still applicable for noise sources with larger RMS values. This can be easily integrated into more advanced circuit simulators.

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