**Challenges at 45nm and Beyond**
November 11, 2008    1:30-3:30pm

Design at 45nm technologies and below is a risky proposition because of the many design challenges involved: variability, leakage, verification complexity, poor analog device performance, etc. In this panel, experienced designers coming from different backgrounds talk about how they have overcome some of the design and CAD challenges in 45nm, what CAD challenges still exist and how the CAD community can help.

**Speakers:**
- Dan Bailey - *Advanced Micro Devices, Inc., Austin, TX*
- Eric Soenen - *Taiwan Semiconductor Mfg. Co., Austin, TX*
- Puneet Gupta - *Univ. of California, Los Angeles, CA*
- Paul Villarrubia - *IBM Corp., Austin, TX*
- Sang Dhong - *IBM Corp., Sunnyvale, CA*

**Mixed-signal Simulation Challenges and Solutions**
November 11, 2008    4:00-5:30pm

The design of complex mixed-signal system-on-a-chip (SOC) designer poses challenging requirements on the simulation design environment. The simulation platform has to include simulations at the behavioral, gate and transistor-level which have traditionally been done in separate environments. As the scaling trend continues, the designer needs additional accuracy and capacity, new capabilities such as efficient statistical simulation that takes into account layout dependent effects. In this panel we have representatives from the CAD and design community discussing the challenges and current solutions available to the mixed-signal simulation challenge.

**Speakers:**
- Henry Chang - *Designer's Guide Consulting, Los Altos, CA*
- William Walker - *Fujitsu Labs, Ltd., Sunnyvale, CA*
- John G. Maneatis - *True Circuits, Inc., Los Altos, CA*
- John Croix - *Nascentric, Inc., Austin, TX*

**More Moore: Foolish, Feasible, or Fundamentally Different?**
November 10, 2008    6:15-7:15pm

**Moderator:** Andreas Kuehlmann - *Cadence Design System, Berkeley, CA*

Moore's law has been a foundation of modern electronics, sustained primarily by scaling. But can this continue despite the serious problems of litho, variability, device physics, and cost? This panel looks at several possibilities. Perhaps Moore's law will muddle through, as it has so far, with a combination of tools, process, and design. But even if technically possible, Moore's law is in practice driven by economics, and economics might turn against further scaling. Also, we've all seen how performance of single cores has topped out, despite scaling. Might this be a fundamental problem with planar technologies, prompting the need to go 3-D to get further performance increases? Or might CMOS itself give way to other technologies, allowing Moore's law yet another respite?

Compare and contrast for yourself these four very different visions of the future of your job, your industry, and your personal gadgets.

**Speakers:**
- Rob Aitken - *ARM, Sunnyvale, CA*
- Jerry Bautista - *Intel Corp., Santa Clara, CA*
- Wojciech Maly - *Carnegie Mellon Univ., Pittsburgh, PA*
- Jan Rabaey - *Univ. of California, Berkeley, CA*