CMOS-MEMS Integration: Why, How and What?

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ABSTRACT
CMOS-MEMS integration can improve the performance of the MEMS (micro-electromechanical systems), allows for smaller packages and leads to a lower packaging and instrumentation cost. As argued in this article, processing MEMS above CMOS is the most promising approach for CMOS-MEMS integration, but it limits the thermal budget for MEMS processing. Poly-SiGe provides the desired material properties for MEMS applications at significantly lower temperatures compared to Poly-Si. A case study of a CMOS-integrated SiGe gyroscope will be presented.

Categories and Subject Descriptors
B.8.0 [**Hardware**]: Performance and Reliability – *general.*

General Terms
Measurement, Performance, Reliability, Experimentation.

Keywords
CMOS-MEMS integration, poly-SiGe, technology.

1. INTRODUCTION
This paper discusses first the reasons for choosing CMOS-MEMS integration, in particular integration by SiGe processing above CMOS. In the next chapter, the processes available for poly-SiGe post-processing are explained. The final chapter then shows a case study of a CMOS-integrated SiGe gyroscope.

2. WHY?
Integration of the MEMS device with the integrated circuit becomes increasingly important for compactness and performance reasons [1-4]. The majority of current MEMS products on the market, however, still uses a hybrid approach (Fig. 1). Such an approach is modular and, as a consequence, has a much shorter development time as compared to the monolithic approach. Also it allows for an independent optimization of the integrated circuit (IC) and the MEMS technology. On the other hand, the assembly and packaging cost is higher in comparison to the monolithic approach. Consequently, once volumes become high enough, the longer development time needed for the monolithic approach is most likely to be paid back by the reduced assembly and packaging cost. Monolithic integration can also be chosen in cases where a lot of interconnections between the MEMS and the CMOS need to be made (e.g. imagers), if miniaturization is important or if an increase in system performance is required. When separate chips for the MEMS and the IC are used, performance-limiting parasitics are present due to the interconnections between the MEMS and logic chip [4]. These parasitics result mainly from the size of the bond pads and from the long bonding wires and would be reduced substantially by on-chip integration.

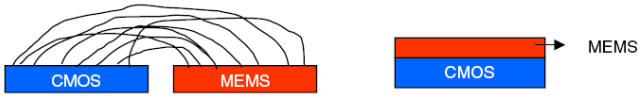

Figure 1. Hybrid approach (left) versus monolithic integration of MEMS and CMOS (right) [2].

Integrating MEMS devices in state of the art CMOS processes, yielding a miniature monolithic system solution, can be done in various ways. We can distinguish three major principles:

(1) processing microsystems first and integrated circuits last and typically next to the sensors [5];
(2) mixing the fabrication of both [6];
(3) and processing the integrated circuit first and the microsystem last [7,8] and typically on top of the circuitry.

This third method is, in our view, the most promising way to do smart microsystem processing, as it allows the use of standard CMOS processes and fairly independent optimization of the CMOS and MEMS. In addition, a new generation of circuitry can easily replace the older one without affecting the MEMS on top of it. Moreover, post-processing provides the most compact form of putting MEMS and CMOS together as the CMOS circuitry can potentially be situated underneath the MEMS structures. However, post-processing limits the thermal budget for MEMS processing. Poly-SiGe provides the necessary mechanical properties and reliability required for MEMS applications at a significantly lower temperature compared to conventional poly-Si (i.e. depositing temperatures of ≤450°C instead of ≥800°C) [7-9]. This makes the poly-SiGe technology very well suited for post-CMOS integration of MEMS.

3. HOW?
Already a multitude of processes have been developed for poly-SiGe MEMS [7-13] and the main tendency has been to reduce the processing temperature [10-12] or to increase the deposition rate at equal temperature [9,13]. By using a multilayer process (Fig.

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2) that combines PECVD and CVD at 2 Torr, high-quality films can be obtained at low temperature (≤450ºC) with very high deposition rates (~100nm/min) [9]. This is the ideal process for the deposition of thick SiGe layers (e.g. for capacitive sensing applications) on top of standard CMOS. A low resistivity of 1.45 mΩcm, a tensile stress of 35 MPa and a very low strain gradient of 3.6×10^{-6} μm^{-1} have been achieved using a top Si-rich stress compensation layer [14]. The contact between Al and SiGe was found to be ohmic as required for CMOS integration [15].

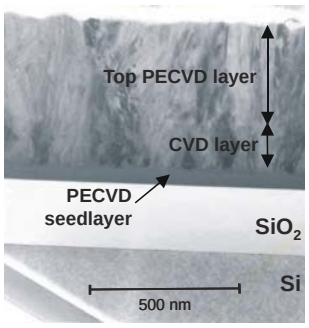

Figure 2. Cross-section of the PECVD/CVD poly-SiGe multilayer [9].

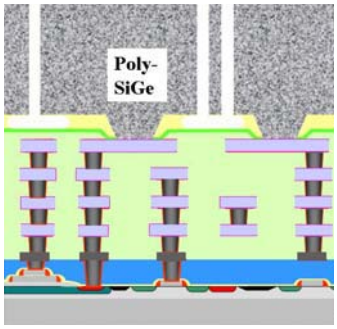

Figure 3. Schematic cross-section of the integrated gyroscope.

4. WHAT?

As a case study an integrated poly-SiGe gyroscopes is presented [15]. The gyroscopes are made in a 10µm thick poly-SiGe structural layer processed above 8" standard 0.35µm CMOS wafers with 5 metal layers (top 4 layers are Al interconnects) and standard passivation (Fig. 3). The sacrificial layer is a thick undoped Si-oxide layer, which is planarized by the use of CMP. The SiGe structural layer is deposited by the combined CVD and PECVD process described above. The release is done using wet processing with HF and CO_2 super-critical drying. The gyroscopes obtained as such (Fig. 4) are free moving and the basic on-chip electronics, needed for the characterization of the mechanical structures (single-ended CDS switched-capacitor amplifiers and buffers, see Fig. 5), are fully functional. The evaluation of the response of the structures, mounted in a 44-pin metal case has been carried out in a vacuum chamber. The results for both the drive and Coriolis detection modes show a good agreement with design values. Measured Q factors for the drive and detection mode at a pressure of 0.8mTorr are in the range of 8-10000 and 4-6000, respectively. The achievable ratio of carrier amplitude to noise floor for the drive and detection mode for this prototype mounted on a test board with the auxiliary circuitry (crystal oscillator, differential amplifiers) required for gyroscope characterization is 110dB and 90dB, respectively, allowing for a yaw rate resolution of 0.020/s for 50Hz measurement bandwidth.

5. CONCLUSION

In conclusion, poly-SiGe post-processing has the potential to become a generic technology in which different MEMS devices can be processed (together) on top of standard CMOS. Moreover, similar processing can be used to fabricate thin-film caps above MEMS devices forming an area-saving MEMS-device-scale 0-level package [13]. Therefore this process might ultimately enable the creation of highly integrated miniature systems with improved performance over the state-of-the-art.

6. ACKNOWLEDGMENTS

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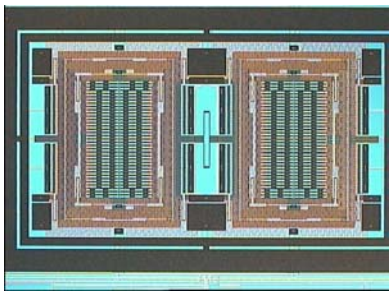

Figure 4. Photograph of the poly-SiGe gyroscope processed on top of a standard 0.35 µm CMOS process with 5 metal levels [15].

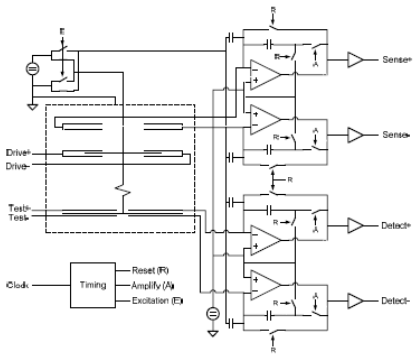

Figure 5. Schematic of the on-chip electronics of the integrated gyroscope of Fig. 4 [15].