EDAA/DATE PhD Forum

The EDAA/DATE PhD Forum offers the opportunity for PhD students to present their thesis work to a broad audience in the design automation and test community from both academia and industry. During the presentation at the DATE Conference it helps students to establish contacts when entering the job market. On the other side, representatives from industry and academia get a glance of state-of-the-art research in design automation and test.
This year we received a total of 60 submissions out of which 46 have been accepted for presentation at a dinner reception. The review process was conducted by a team of 10 internationally renowned reviewers. Our thanks go to all presenters, the PhD Forum Committee and all who were involved in conducting the review process and arranging and organizing the Forum event at DATE. We also thank the EDAA and DATE organizers and representatives for making this Forum possible.

Paul Pop
Chair 2008 EDAA/DATE PhD Forum

PhD Forum Committee

P. Pop (Chair), Technical University of Denmark
R. Buchty, Univ. Karlsruhe, Germany
R. Dick, Northwestern University, USA
R. Dorsch, IBM Böblingen, Germany
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E. Larsson, Linköping University, Sweden
M. Loghi, Politecnico di Torino, Italy
S. F. Nielsen, Technical University of Denmark
A. Shrivastava, Arizona State University, USA
Y. Xie, Penn. State University, USA

Presentations

Ahmed, W., Curtin University of Technology, "Hardware-Software Partitioning to Address System Evolution and Product Lines in Embedded Systems and SoCs"
Alessandro, C., University of Naples Federico II, "Finite Field Arithmetic for Cryptographic Applications: Theoretical Results, Algorithms and Architectures"
Andriamisaina, C., UBS University, "High-Level Synthesis of Multi-mode Architectures for DSP Applications"
Baloukas, C., Democritus University of Thrace, "Data Structures Optimization Methodology of Dynamic Applications in Embedded Systems"
Bartzas, A., Democritus University of Thrace, "Extraction and Utilization of Software Metadata for Dynamic Embedded Applications"
Beck, A.C.S., Federal University of Rio Grande do Sul, "Transparent Reconfigurable Accelerator for Heterogeneous Behavior Systems"
Brisolara de Brisolara, L., Federal University of Rio Grande do Sul, "Strategies for Embedded Software Development Based on High-level Models"
Brunelli, D., University of Bologna, "Real-time scheduling for Energy Harvesting Sensor Networks"
Cyrille, C., STMicroelectronics, "A Design Space Exploration for Space-Time AdapteRs"
Gharehbaghi, A.M., Sharif University of Technology, "System-Level Design Verification"
Gioulekas, F., University of Patras, "Architectures and Implementation of Error Correcting Codes"
Grosse, D., University of Bremen, "Using Formal Methods for Verification of Complex Systems"
Guerra e Silva, L., INESC-ID, "Models and Algorithms for Timing Analysis of Integrated Circuits under Process Variations"
Hashizume, Y., The University of Kitakyushu, "Post-Silicon Clock-timing Tuning with the Discrete PDE Delay Value"
Helms, D. OFFIS, "Leakage Models for High Level Power Estimation"

Hentschke, R., Universidade Federal do Rio Grande do Sul, “New Place and Route Algorithms for Wire Length Improvement With Concern to Critical Paths”
Izosimov, V., University of Linköping, “Scheduling and Optimization of Fault-Tolerant Embedded Systems”
Jenihhin, M., Tallinn University of Technology, “Assertion-based verification and testing with Decision Diagrams”
Kamkin, A., Institute for System Programming of Russian Academy of Sciences, “Functional Validation of Microprocessor Units Based on Contract Specifications”
Kim, M., University of California, Irvine, “xTune: Model-Based Online Verifiable Cross-Layer Adaptation for Distributed Real-Time Embedded Systems”
Krishnan, R., The Pennsylvania State University, “Soft Errors - Tools, Testing & Interactions”
Lettnin, D., University of Tübingen, “SofTPaDS: Semiformal Verification of Temporal Properties in Hardware Dependent Software”
Li, M., IMEC, “Algorithm-Architecture Co-Design for Energy-Efficient Software Defined Radio”
Loi, I., University of Bologna, “Developing Mesochronous Synchronizers to Enable 3D NoCs”
Lorenzi, L., Università degli Studi di Brescia, “Design of a low-power high resolution integrated radar”
Marongiu, A., University of Bologna, “Lightweight Barrier Based Parallelization Support for NCC MPSoC Platforms”
Mathew, J., University of Bristol, “Area Efficient On-chip Fault Tolerant Architectures”
Matsunaga, T., Waseda University, “Arithmetic Synthesis under Bitwise Constraints”
Neophytou, S., University of Cyprus, “High Quality Test Generation for Various Applications in Digital Systems Test”
Nicopoulos, C.A., Ecole Polytechnique Federale de Lausanne, “ViChaR: A Dynamic Virtual Channel Regulator for Network-on-Chip Routers”
Paci, G., University of Bologna, “Exploration of Low Power Adders for a SIMD Data Path”
Pandey, S., Darmstadt University of Technology, “Energy Conscious Robust OnChip Bus Architecture Synthesis for MPSoCs”
Parandeh-Afshar, H. University of Tehran, “Accelerating Arithmetic Dominated Circuits on FPGAs by new synthesis and architectural methods”
Paulsson, K., Universität Karlsruhe, “Exploitation of Dynamic and Partial Hardware Reconfiguration for On-Line Power/Performance Optimization in Self-Adaptive Systems”
Plessas, F., University of Patras, “Electronic Circuit Subsystems for Broadband Wireless Applications”
Raghavan, P., IMEC, “Low Power Instruction Memory and Register File Plug-ins”
Regazzoni, F., University of Lugano, “DPA resistant design flow for design of secure coprocessors”
Reineke, J., Universität des Saarlandes, “Predictability of Cache Replacement Policies”
Ruggiero, M., University of Bologna, “Communication-Aware Stochastic Allocation and Scheduling Framework for Conditional Task Graphs in Multi-Processor Systems-on-Chip”
Rullmann, M., Dresden University of Technology, “Optimization of Reconfiguration Costs in Reconfigurable Computing”
Sawicki, S., Federal University of Rio Grande do Sul, “A 3D I/O Pads Assignment based on the Circuit Structure”
Schallenberg, A., Carl von Ossietzky Universität Oldenburg, “OSSR+R: Modelling and Simulation Self-Reconfigurable Systems”
Stuijk, S., Eindhoven University of Technology, “Predictable Mapping of Streaming Applications on Multiprocessors”
Tawk, M., University of Valenciennes, “MPSoC Simulation Acceleration by a Variable-Sized Sampling”
Tumeo, A., Politecnico di Milano, “CerberO: a framework for reconfigurable multiprocessor real-time embedded systems on FPGA”
Wendt, M., Graz University of Technology, “System Level Energy Estimation and Analysis for Smart Cards and Mobile Devices”