Mixed-Signal Design Space Exploration of Time-Interleaved A/D Converters for Ultra-Wide Band Applications

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Abstract

This paper addresses system-level design of time-interleaved analog-to-digital converters (TI-ADCs) for ultra-wide band communications. Design space exploration of a TI successive approximation architecture is performed via Monte Carlo simulations, by exploiting behavioral models built bottom-up after characterizing the main ADC blocks in a 90-nm 1-V CMOS technology. Different speed/resolution scenarios are efficiently investigated and the impact of parallelism on system performance, yield and power consumption is assessed starting from the early design phases, finally enabling the selection of two candidate implementations (a 6-bit 4.6-mW and a 7-bit 8.1-mW ADC targeting 1 GS/s) that effectively trade accuracy for energy efficiency and area.

1. Introduction

Emerging wide-band wireless communications, such as ultra-wideband (UWB) [1], require analog-to-digital converters (ADC) operating at high speed (~GS/s) and medium resolutions (4-6 bits) with extremely low power consumption and implementation costs. While the exponential dependence of area and power on the number of bits makes flash ADCs maximally efficient for lower resolutions ($\leq$ 5 bits) [2], for the higher resolutions ($\geq$ 6 bits) required by battery-powered multimedia consumer applications, successive approximation (SAR) converters are being increasingly used in parallel arrays, to realize high effective sampling rates with decreased power and area [3][4]. However, like all parallel topologies, time-interleaved (TI) SAR ADCs end with facing the same challenges that flash converters have always faced, such as the realization of the sampling function at high speed, and minimization or compensation of mismatch between the numerous elements. In the literature, TI ADC specifications are mostly determined a priori, by relying on designer's experience and heuristics [4]. Accurate evaluation of mismatch induced performance degradations and energy efficiency, which turn out to play a crucial role for successful design, are rarely carried out at system-level. In this work, we perform mixed-signal design space exploration of a TI-ADC for UWB receivers through a rigorous platform-based methodology [5]. A statistical behavioral model of the system is hierarchically obtained by composing the models of its analog and digital building blocks. In the bottom-up phase of the design, model parameters including the principal circuit non-idealities are extracted from electrical simulations on real implementations of the ADC building blocks in a 90nm CMOS technology. In the top-down phase, ADC performances are computed through Monte Carlo simulations, providing insight in performance degradations at system-level, and allowing selection of those system configurations that optimize well specified quality factors, such as resolution, power, and area. Leveraging quickly executable models anchored to feasible performances, our approach allows efficient and accurate performance estimations, thus avoiding time-consuming iterations in the design flow.

2. Channel Mismatch Errors in TI-ADCs

An M channel TI-ADC is made up of M ADC blocks that operate at only a fraction f_s/M of the required sample rate f_s. Every sampling time, a de-multiplexer feeds the input of one of them with the actual analog signal. Then it switches to the next converter. Once the conversion cycle from every channel is completed, a multiplexer retrieves the corresponding data. The final result is therefore an ADC that operates at the required sample rate f_s. The ADC performance is heavily affected by undesired spectral components due to four types of mismatches in the parallel channel parameters: offset, gain, timing (i.e. clock skew) and bandwidth. To investigate the combined effect of these mismatches we refer to the general block diagram in Figure 1, showing an ADC channel. The timing mismatch, i.e. the deviation from the ideal sampling period T_s is modeled as a time shift of the input signal $x(t)$. The transfer function $G_l(j\omega)$, ideally equal to 1, captures the finite bandwidth filtering effect of the sample-and-hold circuit (S/H) in each channel, in case a distributed time-interleaved S/H is assumed. Finally, each channel has an ideal sampler and quantizer with a gain g_l and an offset o_l. The combined effect of offset, gain and timing mismatches for a given sinusoidal input signal is

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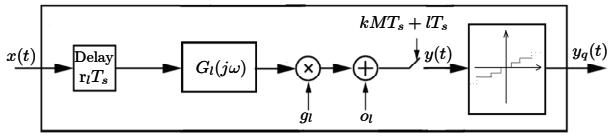

Figure 1: Behavioral model of a TI-ADC channel

extensively analyzed in [6]. Offset mismatch generates spurious tones at frequencies multiples of f_s/M. Signal-to-noise and distortion ratio (SNDR) degradations due to this error are independent of the signal amplitude and frequency. Conversely, gain mismatch errors occur with a period of M/f_s but their magnitude is modulated by the input frequency f_0. Gain error power is, however, independent of f_0. Timing deviations due to systematic clock skew also create spurs at the same frequencies as gain mismatch (and therefore undistinguishable), but SNDR degradations in this case are larger as f_0 increases.

When mismatch between the (finite) bandwidths of the S/Hs is also considered, by extending the result reported in [7] to an arbitrary number of channels, the sampled output from each channel can be approximated as the result of the input signal passing trough a linear filter with transfer function given by:

$$G_l(\omega) = \frac{1 - \mathrm{e}^{-\left(T_s/\tau_l + j\omega T_s\right)}}{\left(1 + j\omega\tau_l\right)\left(1 - \mathrm{e}^{-\left(T_s/\tau_l + j\omega M T_s\right)}\right)} \qquad (1)$$

where τ_l is the time constant of the sampling circuit in the track-mode, and the tracking time is equal to T_s. For a sinusoidal signal, bandwidth mismatch includes a combination of gain and phase mismatches, both dependent on the input frequency as well as the S/H bandwidth. Moreover, phase errors induced by bandwidth mismatch are a nonlinear function of f_0 as opposed to the linear behavior of clock skew effects.

3. TI-ADC Behavioral Model

Each channel SAR ADC is modeled in Matlab using the same block parameters as in Figure 1 to capture the effects of mismatch. The ideal sampler and quantizer blocks are also changed with a more accurate SAR ADC model that includes the effect of thermal noise and static non-linearities. The real SAR model parameters are extracted bottom-up based on feasible performances of the main building blocks in a 6-bit 90-nm 1V CMOS implementation. The reference 6-bit SAR (Figure 2) is based on a fully dynamic architecture, as the one in [8], and consists of a passive S/H circuit, a dynamic comparator topology [2], and a SAR digital controller that drives a DAC placed in a feedback loop with the comparator. The input signal is sampled only at the beginning of the conversion cycle and then held for a number of cycles equal to the resolution n of the ADC.

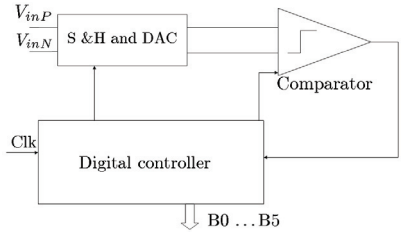

Figure 2: Diagram of the reference channel SAR ADC

An additional sample clock period T_s is allowed for proper settling of the S/H. Therefore, the minimum number of channels for a given resolution n will be $M_{min}=n+1$. Comparator and S/H thermal noise are modeled as random zero mean gaussian generators with a given variance. ADC thresholds are finally perturbed to represent the static non-linearities (INL and DNL) of a real quantizer.

Monte Carlo simulations are carried out based on the following assumptions on mismatch statistics:

- Channel *offset* o_l has a zero mean uniform probability density function (PDF) in the interval [-LSB/4; LSB/4] since we assume that a calibration circuit, as in [2], is capable of providing offset correction in the above range;
- Channel *gain* g_l has a gaussian distribution with mean $G=1$;
- Relative clock *skew* r_l in each channel has a zero mean gaussian PDF;
- The channel S/H bandwidth b_l is a gaussian variable with mean B. The mean bandwidth of the first order low-pass filter approximation is computed by imposing that a maximum LSB/4 sampling error is allowed within the sampling time T_{SH}. T_{SH} is equal to the time available for each SAR conversion step and can be expressed as $T_{SH}=T_s \cdot M/(n+1)$. The average bandwidth will therefore be:

$$B = (1+\varepsilon)\frac{(n+2)\ln 2}{2\pi T_{SH}}, \qquad (2)$$

  ε being an additional design margin over the theoretical minimum value.

Comparator noise is a function of its power consumption. Noise variance has been estimated from the 6-bit SAR reference design, sized for a noise standard deviation σ_n=1.4mV~LSB/9 to be conservative. For other resolutions, a "hard" scaling rule would suggest that the σ_n/LSB ratio should be kept constant. Since this would theoretically lead to a 4 time increase in power consumption for each additional bit, we finally opt for a "soft" scaling rule, allowing only a doubling in the power consumption per bit. Therefore, the comparator energy per comparison E_{comp} is scaled with resolution based on the following law:

$$E_{comp}(n) = 2^{n-6} E_{comp}(6), \qquad (4)$$

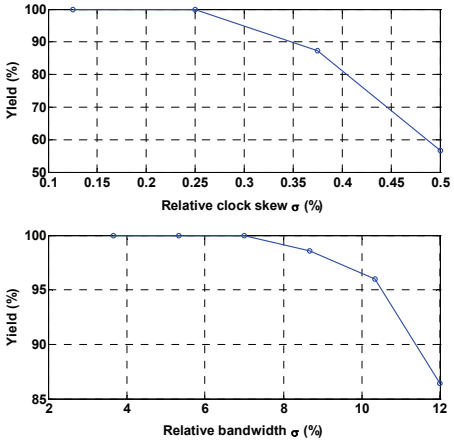

Figure 3: 5.5-ENOB yield in a 6b TI-ADC vs. clock skew (σ_τ/T_S) at Nyquist and bandwidth (σ_b/B) standard deviations

which leads to the following noise scaling relation

$$\sigma_n(n) = \frac{\sigma_n(6)}{\left(\sqrt{2}\right)^{n-6}}. \quad (5)$$

Based on (5), noise is allowed to decrease by only a 1.4-factor for each bit, so as to limit power consumption while still keeping thermal noise sufficiently below the quantization error.

4. Design Space Exploration Results

To investigate the sensitivity of a TI system to the different mismatch sources, we first performed Monte Carlo simulations on a 6-bit TI-ADC operating at 1.1 GS/s with ideal channel samplers and quantizers. A number of 1,000 samples per run is sufficient thanks to the assumptions on PDFs made in Section 3. Since one SAR comparison cycle T_{SH} is reserved for input sampling, the array is made up of 7 elements. We define the *design yield* as the percentage of samples providing an effective number of bits (ENOB) larger than 5.5. For instance, in Figure 3, design yields are represented as a function of the standard deviation of timing and bandwidth mismatches. Yield is quickly degraded by timing mismatches showing that clock skew is the most critical error for 6 bit. However, a 98% yield can still be guaranteed by a relative skew standard deviation σ_τ=0.27%, corresponding to a 2.4-ps absolute value. On the other hand, bandwidth mismatch is expected not to be an issue in our design. In fact, constraints imposed by linearity already called for such a high bandwidth *B* that the effects of mismatch became practically irrelevant to the final SNDR.

More importantly, the combined effect of all mismatches has been also simulated as a function of the number of array elements. A first set of simulations was performed to find out the resolution offering the best trade-off between performance and cost in complexity and power consumption. As practical values for the mismatch source variances, we chose those values that guaranteed a 98% yield (at the 5.5-ENOB level) for the 6-bit TI-ADC in our previous explorations. All sigma are assumed independent of the resolution of the converter, except for the offset variance, which scales with the LSB because of the offset compensation network that needs to be sized according to the ADC resolution. Experiments were performed in two cases: (A) the channel ADCs have no noise and distortion; (B) each channel has a noise source as determined in Section 3 and maximum static non-linearities as in Table 1. Figure 4 shows the average ENOB and spurious free dynamic range (SFDR) as a function of resolution from 4 to 9 bits. Even in case (A), because of channel mismatches, the ENOB curve saturates to 6.25 when the number of parallel component increases. As a matter of fact, using more than 8 parallel elements (to implement a 7 bit ADC) turn into a waste of power and area for the tested values of mismatches. Results are even worse in case (B), where additional 0.2-bit ENOB degradations are observed with respect to case (A), almost independent of *n*.

Bit	4	5	6	7	8
INL (LSB)	0.05	0.11	0.22	0.44	0.9
DNL (LSB)	0.04	0.05	0.08	0.08	0.08

Table 1: Maximum INL and DNL of a channel ADC as a function of its resolution (based on a 90-nm CMOS implementation)

A second set of simulations aimed to characterize TI architectures when the number of elements is increased while targeting the same nominal resolution. Increasing the number of channels above M_{min} relaxes the speed requirements of each SAR ADC and increases the sampling time available to the S/H thus reducing the effects of bandwidth mismatch. Simulation parameters have been set as in case (B). Implementing a 6 bit converter by interleaving 7, 8 or 9 elements has a negligible impact on performance. The variation in ENOB (less than 0.05 LSB) is of the same order as the Monte Carlo run accuracy. Due the high bandwidth of the S/H, the additional time available for settling does not bring substantial advantages.

5. Energy Efficiency Considerations

In addition to ENOB and SNDR, energy efficiency has a key role in determining the final architecture for our applications. To account for this aspect, we report first order energy scaling considerations, assuming the SAR ADCs as the dominant source of power consumption.

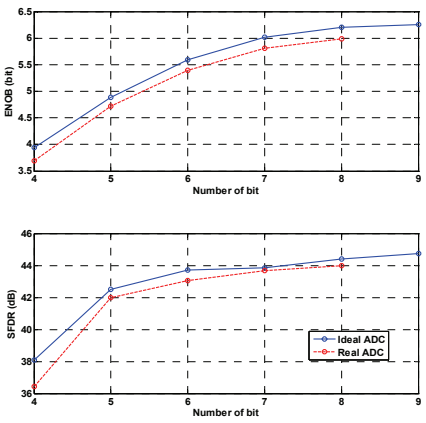

Figure 4: ENOB and SFDR as a function of resolution (σ_o=0.08 LSB, $\sigma_{g/G}$=0.8%, σ_r=0.27%, $\sigma_{b/B}$=7%)

Based on our dynamic 6-bit 90-nm CMOS SAR reference implementation, the analog energy per conversion is estimated as in Section 3 for both comparator and S/H, and is assumed to double each time one bit is added ("soft" law). Conversely, the energy per operation in the digital portion, also estimated based on the 90-nm prototype, is almost independent of the ADC resolution. The total power consumption and the figure of merit $FoM=P_{tot}/(2^{ENOB} \cdot f_S)$, traditionally employed to compare different ADC implementations in terms of energy per conversion-step [2] are represented in Figure 5 as a function of the ADC resolution.

On the other hand, increasing parallelism for a fixed resolution does not increase the power consumption when a dynamic architecture is used. In fact, power can be expressed as a function of the SAR energy per conversion E_{conv} as follows:

$$P_{tot} = MP_{ch} = M\frac{n}{n+1}E_{conv}f_{SH} = nE_{conv}f_s \qquad (6)$$

where f_{SH} is the frequency of the SAR algorithm. Equation (6) shows that power consumption is only a function of the resolution and the sampling rate of the TI-ADC.

Based on results in Figure 4 and Figure 5, an 8-element 7-bit ADC can be selected as a good compromise for our target UWB application. It offers 96% design yield, a 5.8 average ENOB, 43.6-dB average SFDR. Based on the reference SAR architecture implementation in 1-V 90-nm plain CMOS, we obtain 8.1-mW power consumption, 131 fJ/Conversion-step and 0.41-mm^2 area occupation. However, a 6-element design is also competitive in our performance range. In spite of a 0.4-bit ENOB degradation (17% design yield, 5.4 mean ENOB, 43-dB SFDR) it would cost 40% less power (4.6 mW) and 58% less area (0.17 mm^2) while achieving a 25% improvement in the FoM (99 fJ/Conversion-step). Its

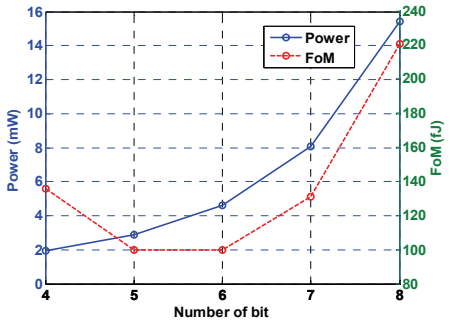

Figure 5: Power consumption and FoM as a function of TI-ADC nominal resolution

efficiency would be even higher if a "hard" scaling law was used in estimations (see Section 3).

6. Conclusions

We performed mixed-signal design space exploration of a TI SAR-ADC for UWB battery-powered consumer applications through a rigorous platform-based methodology. Although parallel SAR architectures remain promising for high data rates and medium resolutions (5-7 bits), it was shown that their well-known efficiency advantage over other approaches can be relevantly overcome by mismatch errors for higher resolutions. Based on exploration results, two configurations, a 7-bit and a 6-bit array, effectively trading performance for power consumption and area, were proposed as the best candidates to match the requirements of the target application. The presented work has been partially supported by the Italian research program PRIN protocol 2005093524_002.

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