Impact of Leakage Current on Data Retention of RF-powered Devices During Amplitude-Modulation-based Communication

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Abstract

Devices powered by an electromagnetic field are inherently power-constrained and thus must carefully manage static and dynamic power. High ambient temperatures and field strengths can increase the temperature of RF-powered devices up to more than 100 degrees Celsius, thereby allowing the leakage current to rise to a dominating portion of the static power consumption.

Leakage reduction techniques for application in RF-powered devices are examined in this paper with the goal to avoid malfunction of the device during amplitude modulation-based communication. Results show that without leakage reduction a correct operation cannot be guaranteed for the investigated 130 nm process technology for energy gaps that are defined by the widely applied ISO/IEC 14443-2 standard (100% field modulation). The evaluation of leakage reduction techniques shows that applying body biasing prolongs the data retention time by nearly 200%, while source biasing in general aggravated the circuit’s robustness against power gaps (reduction in data retention time by up to 76% loss), as did also voltage scaling (up to 98% reduction).

1. Introduction

Contactless ICs powered by a radio frequency field are used in an increasing number of applications, including electronic passports issued by a large number of countries around the world, as well as contactless credit cards. In everyday life the circuit must also operate reliably in an environment with high ambient temperature and field strength. A high field strength results in self-heating of the silicon as the energy that is not required to operate the chip must be dissipated on-chip [2]. This results in a total chip temperature of more than 100 degrees Celsius.

At this temperature leakage current will consume a significant portion of the total static current of chips fabricated with deep submicron technology [3]. While this does not limit the data retention capability of sufficiently supplied chips, amplitude modulation-based communication schemes influence the device’s stability in the case of high leakage current. Widely used communication standards [1, 2] define a 100% modulation index which causes energy gaps - i.e., periods of time during which no energy is available from the field. During energy gaps the device’s dissipated power must be provided by on-chip capacitors, resulting in a voltage drop (Figure 1). Data retention cannot be guaranteed should the voltage fall below the minimum voltage ($V_{dd\text{min}}$). This work focuses on analysis of leakage reduction techniques that can be applied during 100% ASK modulation to prevent device malfunction. The results will show that not all techniques developed for circuits with a stable power supply are applicable to RF-powered chips.

Figure 1. During energy gaps induced by 100% ASK modulation leakage currents are drawn from on-chip capacitors. The resulting voltage drop must not violate the minimum operating voltage condition.

The main contributions of our work are as follows: (i) the development of an analytical system-level model that enables analysis of the efficiency of leakage reduction techniques for RF-powered devices; (ii) to the best of our knowledge, this is the first work showing that 100% ASK modulation - although widely used - is not the best choice
for RF-powered devices fabricated using deep submicron technology.

This paper is organized as follows: Section 2 describes the model to calculate the time a circuit can guarantee data retention in the case that the power supply delivers no energy. Section 3 elaborates the advantages and drawbacks of the investigated leakage reduction techniques when used during energy gaps. Section 4 shows simulation results for a sample circuit and the impact of the leakage reduction techniques on the data retention time. Section 5 concludes this paper.

2. Modeling Data Retention Time During Energy Gaps

Estimating the data retention time \( T_{dr} \) at system level is crucial for defining the appropriate power management. Analytical models, as proposed in this work, allow statements about the circuit’s maximum data retention time at a very early stage of the design process without detailed knowledge of the final design.

2.1 Modeling Approach

To define an accurate, yet simple model of the RF-powered circuit, a model is proposed that is built upon the following properties: supply voltage, on-chip capacitance between \( V_{dd} \) and \( V_{ss} \), leakage current models, and finally the bias currents of the IC (see Figure 2). Based on our experience, the on-chip capacitance as well as the number of devices (proportional to the leakage current) can be derived from the estimated chip area in a reliable way.

![Figure 2. Equivalent circuit of an unpowered integrated circuit. The charge stored in the on-chip capacitor \( C \) must buffer all static currents.](image)

The voltage applied to the circuit while it is powered is denoted as \( V_0 \). The static current consists of two parts, namely the leakage current \( i_{\text{leak}} \) and the constant static current \( I_{\text{const}} \). The latter includes all constant currents dissipated by the circuit, such as bias currents and other analog currents required to keep the circuit operating. It is assumed that there is no dynamic current during the gaps, which is a realistic assumption for RF-powered devices.

Based on the model, the charge that can be used for compensating dissipated energy is given by

\[
Q_{dr} = C \cdot (V_0 - V_{dr})
\]

where \( V_{dr} \) denotes the voltage at which data retention is guaranteed. During the energy gap \( T_{dr} \) a charge is dissipated by the static currents \( Q_{\text{static}} \) as given by

\[
Q_{\text{static}} = \int_0^{T_{dr}} i_{\text{leak}}(t) \, dt + I_{\text{const}} \cdot T_{dr}
\]

While \( I_{\text{const}} \) is considered to be constant over the voltage \( V_{dd} \), the leakage current varies with the operating voltage \( V_{dd} \). Thus, the leakage current changes over the energy gap because the on-chip capacitance is discharged and \( V_{dd} \) is reduced \( (U = \frac{Q}{C}) \).

In order to guarantee data retention throughout the entire duration of the energy gap \( T_{dr} \), the following condition must be satisfied:

\[
Q_{dr} \geq Q_{\text{static}}
\]

3 Impact of Leakage Reduction Techniques on Data Retention Time

Leakage current dominates the static current consumption of RF-powered devices fabricated in deep submicron when operated at high temperature. Thus, leakage reduction is essential to avoid malfunctions caused by voltage drops below the minimum permissible operating voltage. Figure 3 depicts the leakage current savings when applying voltage scaling \( (V_{dd}) \), body biasing \( (V_{bs}) \), and source biasing \( (V_{ss}) \). The combination of the reduction techniques is also given. While the savings generally look well, not all reduction techniques prolong the data retention time, but even reduce it. In the following treatment, the leakage reduction techniques are analyzed regarding their application during energy gaps caused by amplitude modulation of the field.

Supply voltage scaling. Forcing the supply voltage to a lower level reduces the leakage current immediately. The drawback is the dramatic reduction in the buffered charge (between \( V_{dd} \) and \( V_{ss} \)) used to compensate the leakage current during the energy gap. This reduces the data retention by the time \( T_{\text{lost}} \) which can be calculated using Equation 4.

\[
Q_{\text{lost}} = (V_{dd0} - V_{dd\text{scale}})C = \int_0^{T_{\text{lost}}} i_{\text{leak}}(t) \, dt + I_{\text{const}} \cdot T_{\text{lost}}
\]

where \( Q_{\text{lost}} \) denotes the charge lost due to voltage scaling, \( V_{dd0} \) is the nominal voltage scaling, and \( V_{dd\text{scale}} \) is the reduced voltage used for voltage scaling.
4. Experimental Results

A test circuit was developed using standard cells in 130 nm technology [4] with high-$V_T$ devices for verification of the modeling approach. The CMOS circuit operates at a voltage of 1.5 V with data retention guaranteed for voltages down to 0.8 V. The minimum data retention time is taken from the ISO/IEC 14443-2 standard. There, the maximum duration of an energy gap is defined by the parameters $t_1$ and $t_4$, resulting in a minimum $T_{dr}$ of $\max(t_1) + \max(t_4) = 3.4\mu s$ for a baudrate of 106 kbit/s.

In this work, voltage scaling, body biasing and source biasing are investigated regarding their application for RF-powered devices. Figure 4 depicts the chip voltage over the energy gap when different body-biasing voltages are applied. As expected from the theory and the SPICE simulations (Figure 3), the data retention time does not increase monotonically with bias voltage, but reaches a maximum of 195% prolongation when biased with 0.4 V as shown in Figure 4 and Table 1. The figure also shows that voltage scaling ($V_{bs} = 0$) can reduce the data retention time dramatically - e.g., scaling the voltage down from 1.5 V to 1.1 V reduces $T_{dr}$ to about 50%, while reducing the voltage near to the data retention voltage yields a reduction of up to 98%.

The data retention time is determined for all combinations of the investigated leakage reduction techniques. Voltage-over-time simulation is automatically performed at different source and body-biasing voltage points. Voltage scaling was investigated any further as the drawbacks are obvious. The results of the analysis show that body biasing in general increases the data retention time, while source biasing has no effect (+2%) and even reduces the circuit’s ability to compensate energy gaps by up to 76% (see Table 1 and Figure 5 and Table tResults). The decrease in $T_{dr}$ in the case of source biasing is due to the fact that the charge available from the on-chip capacitor is reduced dramatically if data retention voltage is increased. Source biasing also reduces the data retention time when used together with body biasing - e.g., from 195% prolongation ($V_{bs} = 0.4V$).
and \( V_{\text{SS}} = 0 \text{V} \) down to a reduction by 76\% \( (V_{\text{bs}} = 0.4 \text{V} \) and \( V_{\text{SS}} = 0.6 \text{V} \). Thus, a technique that reduces leakage current is not always well-suited to RF-powered devices. However, one can think about applying source biasing to specific parts of the circuit that do not have to retain data - e.g., large combinational data paths.

Figure 5. Data retention capability of the investigated CMOS circuit when applying body biasing \( (V_{b}) \) and source biasing \( (V_{\text{vss}}) \) during an energy gap.

In contrast, body biasing is shown to be effective for electromagnetic field-powered devices as it prolongs data retention by up to 195\%. These savings come with an increased complexity in the process and area of the devices.

5. Conclusion

In this paper we elaborated the impact of field modulation-based communication protocol on the data retention of RF-powered devices. The investigations were carried out for communication protocols using 100\% amplitude modulation communication causing periods during which no power is available from the RF field. A model for the data retention time is proposed which can be applied very early in the design process.

Results in an industrial 130 nm process with high-\( V_T \) devices showed that an RF-powered device heated up to more than 100 degrees Celsius by high ambient temperature and self-heating effects cannot retain data over the standardized period of 3.4 \( \mu\text{sec} \) [1] during an energy gap. Voltage scaling, body biasing, and source biasing - leakage reduction techniques traditionally applied to devices with a constant power - were investigated for application in RF-powered devices. The evaluation of leakage reduction techniques shows that applying body biasing prolongs the data retention time by nearly 200\%, while source biasing in general aggravated the circuit’s robustness against power gaps (reduction in data retention time by up to 76\% loss), as did also voltage scaling (up to 98\% reduction).

Table 1. Data retention time for different body- and source-biasing voltages. The results from the proposed analytical approach \( (\text{mod} \ [\mu\text{sec}]) \), SPICE simulations \( (\text{sim} \ [\mu\text{sec}]) \), prolonging of the data retention time \( (\text{impr}) \), and errors between SPICE simulation and the analytical model are shown \( (\text{err}) \).

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References


