Spatial Correlation Extraction via Random Field Simulation and Production Chip Performance Regression

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Abstract

Statistical timing analysis needs a priori knowledge of process variations. Lack of such a priori knowledge of process variations prevents accurate statistical timing analysis, for which foundry confidentiality policy has largely been blamed. A significant part of process variations are design specific, and can only be extracted from production chip performance statistics. In this paper, I adopt the homogeneous isotropic random field model for intra-die random variations, apply fast Fourier transform (FFT) to simulate a homogeneous isotropic random field, obtain corners for Monte Carlo SPICE simulation of timing critical paths in a VLSI circuit, and apply regression to match production chip performance statistics. Experimental results based on a timing critical path in an industry design with 65nm Predictive Technology Models reveal constant mean, increased standard deviation, and decreased skewness of a signal propagation path delay as spatial correlation increases. The proposed spatial correlation extraction technique can be applied in a chip tapeout process, where process variations extracted from an early tapeout help to improve statistical timing analysis accuracy and guide engineering change order of subsequent tapeouts.

1 Introduction

VLSI technology scaling has introduced increased variations in VLSI designs, including (1) variations in the VLSI manufacturing process, e.g., of layout geometry, dopant concentration, and stress, and (2) variations at system runtime, e.g., of temperature and power/ground supply voltage. Such process and system runtime variations lead to increasingly significant system performance variation, which increases probability of timing violation and hinders VLSI design performance improvement. Statistical timing analysis is necessary to capture such system performance variation and form the basis of nanoscale VLSI performance optimization.

Traditional VLSI timing analysis finds minimum and maximum signal arrival times at each node, and captures only inter-die variation. Statistical timing analysis computes the signal arrival time distribution at each node in a probability density function, and finds the “timing yield,” which is the probability that a chip meets its timing specifications under process and system runtime variations. Significant accuracy improvement has been achieved in statistical timing analysis, e.g., by including into consideration correlations between process and system runtime variations [2, 3], multiple-gate-input switching [1], crosstalk coupling [7, 8], etc. However, a fundamental problem remains in achieving accurate VLSI statistical timing analysis, which is addressed in this paper.

Statistical timing analysis needs a priori knowledge of process variabilities, e.g., in terms of standard deviations and correlations of various process parameters. Lack of such a priori knowledge of process variabilities has formed a fundamental gap to achieve accurate parametric yield estimation. For this foundry confidentiality policy has been largely blamed. However, a significant part of process parameter variabilities differ for each design, and can only be achieved after a VLSI design is manufactured and measured [22]. Extracting process variabilities can be achieved based on production chip performance statistics, even without access to foundry confidentiality data. Of particular interest is spatial correlation extraction, which is critical to achieve accurate statistical timing analysis [16], and can only be extracted from production chip performance statistics as is shown as follows.

Test chips and test structures help foundry process development and provide design guidelines in SPICE models, technology file parameters, and design rules. However, they provide only limited capability for production monitoring and yield analysis [22]. This is because process para-
ters in a test chip may not have the same variabilities as in the production chip. Most interconnects in a test chip look like nothing in a production chip. Lateral layout feature dimensions, e.g., wire width and transistor channel length, are given by lithography process and affected by nearby features [5]. Vertical layout feature dimensions, e.g., wire thickness and gate oxide thickness, are given by chemical mechanical polishing (CMP) process and depend on local layout density [17]. As a result, accurate production monitoring and yield analysis can only be achieved via production chip based process variation extraction.

Process parameter spatial correlation has received increased attention recently. A conventional technique partitions the layout plane by a grid, assuming perfect correlation for all random variables (e.g., transistor threshold voltage or channel length) in the same grid cell, and computes a correlation matrix for the grid cells [2]. The number of correlated random variables can be further reduced by (1) clustering the grid cells into perfect correlation circles [15], (2) applying principle component analysis (PCA) [2, 20], or (3) applying Kahuna-Loëve expansion [4]. These techniques are based on a discrete random field (represented by the grid cells). A continuous (homogeneous isotropic) random field is the simplest model for intra-die variation (consisting of a single parameter), which greatly facilitates spatial correlation extraction, with reasonable accuracy (a homogeneous isotropic random field has a constant mean and a spatial correlation which depends only on distance) [25]. However, in [25], spatial correlations are extracted based on direct measurement at sampling sites across a chip, which is unlikely to be available in a production chip for process variations, while IR drop and on-chip temperature variation spatial correlations can be extracted in generalized least square fitting [14]. To the best of my knowledge, no practical process variation spatial correlation extraction method is available, except a recent publication [13] which proposes to refine spatial correlation bounds by rejection sampling based on statistical static timing analysis (SSTA) results.

In this paper, I model process parameter variations across a chip in homogeneous isotropic random fields, and propose a spatial correlation extraction technique based on production chip performance statistics. I simulate a homogeneous isotropic random field by fast Fourier transform (FFT), generate corners for Monte Carlo SPICE simulation, and apply regression to match production chip performance variability. The proposed technique can be applied to a chip tape-out process, where process variation extraction based on an early tapeout improves statistical timing analysis accuracy and guides engineering change order of subsequent tapeouts.

The rest of the paper is organized as follows. After giving the problem formulation in Section 2, I propose a spatial correlation extraction technique in Section 3, and present the experimental results in Section 4, before conclude in Section 5.

2 Problem Formulation

In this paper, we study process variation extraction based on production chip performance statistics, which is the only reliable measurement data for process variation extraction and subsequent engineering change order for timing yield improvement in a tapeout process. The problem is formulated as follows.

**Problem 1 (Process Variation Extraction)** Given

1. a circuit under test,
2. performance models, and
3. production chip performance statistics,

find parameter variations in the performance models which best match the production chip performance statistics.

VLSI process variations are categorized as (1) inter-die variation, which can be filtered out by averaging over dies, (2) systematic intra-die variation, which is predictable (up to certain accuracy level) via CMP and lithography simulations and subsequent parasitics extraction, and (3) residual intra-die random variation. In this paper, I model the residual random variations by homogeneous isotropic random fields, and apply regression to extract spatial correlations of the random fields which best fit the production chip performance statistics. For the most accurate statistical performance analysis, I simulate homogeneous isotropic random fields to generate corners, and apply Monte Carlo SPICE simulation for the timing critical paths in the design. For efficiency, I construct functions of performance variations in terms of process parameter spatial correlations, and apply regression based on the constructed functions. Algorithm 1 summarizes the proposed process variation extraction method.

**Algorithm 1:** Process Variation Extraction via Production Chip Performance Statistics

**Input:** Circuit under test, performance models, production chip performance statistics

**Output:** process parameter spatial correlations

1. Predict systematic variations
2. For each set of process parameter spatial correlations
3. Simulate homogeneous isotropic random fields
4. Perform Monte Carlo SPICE simulation
5. Find functions of performance var. in spatial corr.
6. Perform regression
7. Find best fit process parameter spatial correlations
3 Modeling and Extraction of Spatial Correlations

3.1 Homogeneous Isotropic Random Field

Let us model intra-die random variations by homogeneous isotropic random fields [25], i.e., they have identical means at every location on the chip, and their spatial correlations depend only on the distance between the two locations. The accuracy of such homogeneous isotropic random field models is ensured as follows.

1. Systematic variation prediction includes minimum deviation regression, which leaves the remaining intra-die random variations of identical (zero) means in the layout plane.

2. Most manufacturing steps have no orientation preference, e.g., CMP and ion implantation, with some exceptions, e.g., lens aberration occurs only in the step-and-repeat layout plane. Scaling the layout plane in the orientation preference direction removes such orientation preference.

A homogeneous isotropic random field model for intra-die random variations achieves not only accuracy but also efficiency in spatial correlation extraction. The formal definition of a homogeneous isotropic random field is as follows.

Definition 1 A random function \( ξ(x) \) \((x \in \mathbb{R}^n)\) is a homogeneous isotropic random field if \( \mathbb{E}[ξ(x)] = \text{const} \) \((\text{e.g., } 0)\), \( \mathbb{E}[ξ^2(x)] < \infty \), and its autocovariance function \( \mathbb{E}[ξ(x)ξ(y)] = R_{ξξ}(r) \) depends only on the distance \( r = |x − y| \) between the two locations \( x \) and \( y \) [21].

A homogeneous isotropic random field has specific autocovariance functions, e.g., as follows [25]:

\[
R_{ξξ}(r) = e^{-αr}
\]

where \( α \) is a parameter that regulates the decay rate of the correlation function with respect to distance \( r \).

The simplicity of this model (with a single parameter \( α \)) greatly facilitates spatial correlation extraction. I adopt this spatial correlation function for homogeneous isotropic random field extraction in this paper, while this method is independent of the spatial correlation function that we adopt, any other possible spatial correlation functions can also be applied or found by regression techniques [25].

3.2 Fast Fourier Transform Based Simulation

I simulate the random fields of process parameters to generate corners for Monte Carlo SPICE simulation.

A homogeneous isotropic random field \( ξ(x) \) is completely described by its autocovariance function \( R_{ξξ}(r) \) or its autospectral density function \( G_{ξξ}(ω) \), which form a Fourier transform pair [24]:

\[
R_{ξξ}(r) = \int_{R} e^{iωr}G_{ξξ}(ω)dω
\]

\[
G_{ξξ}(ω) = \int_{R} e^{-iωr}R_{ξξ}(r)dr
\]

where \( ω = 2πλ^{-1} \) is frequency, \( λ^{-1} \) is wavenumber, \( λ \) is wavelength. For a real-valued random field, \( G_{ξξ}(ω) = G_{ξξ}(-ω) \), we denote the one-sided spectral density function as \( S_{ξξ}(ω) \).

Let \( ω_c \) be the upper cutoff frequency, above which the values of the frequency spectrum are insignificant for practical purposes. We divide the interval \([0, ω_c]\) into \( N \) equal parts, each having length \( Δω = ω_c/N \). To apply the FFT in the simulations, we choose \( ω_k \) such that for any \( k ≥ 1 \), \( ω_{k+1} - ω_k = Δω \). Let \((r, ϕ)\) be the polar coordinates in a 2-D random field. The simulation result \( ξ'(r, ϕ) \) is given in the form of Riemann integral sum as follows [10].

\[
ξ'(r, ϕ) = \sqrt{2πΔω}\sum_{l=-L}^{L}\sum_{k=1}^{N}\sqrt{ω_kS_{ξξ}(ω_k)}J_l(ω_kr)(cos(lϕ)η_{lk1} + sin(lϕ)η_{lk2})
\]

where \( J_l(\cdot) \) is Bessel function of \( l \)-th order, \( η_{km}, m = 1, 2 \) are independent Gaussian random variables with zero mean and unit variance.

The algorithm for simulating a homogeneous isotropic random field using FFT consists of two steps as follow.

1. Define two arrays for \( 1 ≤ k ≤ N \) and \(-L ≤ l ≤ L\):

\[
a_{lk} = \sqrt{2πΔωω_kS_{ξξ}(ω_k)η_{k1}}
\]

\[
b_{lk} = \sqrt{2πΔωω_kS_{ξξ}(ω_k)η_{k2}}
\]

2. Calculate approximated random field value at any location \((r, ϕ)\):

\[
ξ'(r, ϕ) = \sum_{l=-L}^{L}\sum_{k=1}^{N} J_l(ω_kr)(cos(lϕ)a_{lk} + sin(lϕ)b_{lk})
\]

We have \( S_{ξξ}(ω) \) as follows by substituting (1) into (2).

\[
S_{ξξ}(ω) = \int_{0}^{∞} e^{-(α+iω)r}dr = \frac{1}{α + iω}
\]
The simulated random field is isotropic and asymptotically homogeneous (as \( L \to \infty \)) Gaussian with zero mean and unit standard deviation. A similar homogeneous isotropic random field simulation method is available in [10].

3.3 Regression

Having the corners generated by simulating the random fields of process parameters, I apply Monte Carlo SPICE simulation and find the mean square mismatch of critical path delays given by (1) the proposed model prediction and (2) production chip measurement. The tentative random fields are then perturbed to minimize the mean square mismatch.

Regression for spatial correlation decay rate extraction is formulated as follows.

**Problem 2 (Spatial Correlation Decay Rate Extraction)**

Given

1. timing paths \( \{ p_i \} \),
2. production chip performance statistics (e.g., moments \( \{ m_i \} \) (standard deviations, skewness, etc.) and correlations \( \{ \text{corr}_{ij} \} \) of delays \( \{ d_i \} \) of timing paths \( \{ p_i \} \)),
3. process parameter variations \( \{ v_i \} \) (e.g., in homogeneous isotropic random fields of autocovariance functions in the form of \( R_{\xi \xi}(r) = e^{-\alpha r} \)),
4. functions of production chip performance statistics (path delay moments \( \{ m_i \} \) and correlations \( \{ \text{corr}_{ij} \} \) in spatial correlation decay rates \( \{ \alpha_i \} \), given by homogeneous isotropic random field simulation and SPICE simulation,

find the spatial correlation decay rates \( \{ \alpha_i \} \) which best fit production chip performance statistics (path delay moments \( \{ m_i \} \) and correlations \( \{ \text{corr}_{ij} \} \)).

For efficiency, I construct functions of path delay statistical moments and correlations in terms of process parameter spatial correlation decay rates, such that applying Monte Carlo SPICE simulation is not needed in regression. For a straightforward implementation, I adopt a greedy steepest descent algorithm for nonlinear optimization. More powerful methods, e.g., Levenbert-Marquis algorithm for least mean square regression, can be applied for improved efficiency and solution quality.

4 Experiment

The proposed spatial correlation extraction method is validated in the following experiments.

Given inter-die variations and systematic intra-die variations by lithography and CMP simulations and subsequent parasitics extraction, I simulate the effect of spatial correlation on timing critical path delay as follows.

1. I perform timing analysis by Synopsys PrimeTime and find a timing critical path.
2. I find the locations of the cell instances in the timing critical path, simulate a homogeneous isotropic random field according to an assumed spatial correlation delaying rate \( \alpha \), and find the variations for each cell instance in the critical path.
3. I modify the netlist and the device models for the cell instances in the timing critical path, and perform SPICE simulation for the critical path delay statistical distribution.

Let us study signal propagation delay variation of a timing critical path of 30 combinational logic gates in an industry design of 109,000 components. The logic gates in the path include inverters, buffers, NAND, OR, XOR, and AOI gates, which are placed in a 165.2\( \mu m \times 554.4\mu m \) layout region. We simulate homogeneous isotropic random fields for gate channel length \( L_{gate} \), transistor threshold voltage \( V_{th} \), and interconnect width \( w_{int} \) variations, and perform SPICE simulation for the critical path delay statistical distribution.

We assume near zero spatial correlation for the transistor threshold voltage \( V_{th} \) variation (which results from ion implantation) by setting a large spatial correlation decay rate \( \alpha = 1 \). The spatial correlation decay rate \( \alpha \) ranges from 1, 0.1, to 0.01 for gate length \( L_{gate} \) and interconnect width \( w_{int} \), such that cell instances several hundreds or thousands \( \mu m \) apart would have virtually no correlation. We have a \( 1\mu m \) cutoff wavelength \( \lambda_u = 1\mu m \), and partition the correlation frequency spectrum \([0, \omega_0]\) into 100 equal parts \( N = 100 \). Bessel functions are of order ranging from −50 to 50, i.e., \( L = 50 \). The simulated homogeneous isotropic random fields have an approximately unit standard deviation \( \sigma = 1 \). We scale the simulated random field according to different standard deviations of the parameters, e.g., gate length \( L_{gate} \) and interconnect width \( w_{int} \) have \( 3\sigma = 15\% \), transistor threshold voltage has \( 3\sigma = 30\% \).

Fig. 1 gives probability density functions (pdf’s) for the critical path delay with different spatial correlation decay rate \( \alpha \). Each pdf is achieved by SPICE simulation based on 1000 samples of random field variation corners. Table 1 gives the means and the standard deviations of the critical path delay variations for different spatial correlations. We have the following observations.

\( ^2 \) A more detailed analysis of process parameter variations would separate PMOS and NMOS transistor channel lengths and threshold voltages, and interconnect widths on different routing layers.
The mean critical path delay is constant for different spatial correlation decay rate $\alpha$, while the standard deviation of the critical path delay increases as the spatial correlation decay rate decreases. A decreased spatial correlation decay rate gives increased spatial correlation. The two extreme cases $\alpha = \infty$ and $\alpha = 0$ corresponds to zero and 100% spatial correlation, respectively. In the presence of zero spatial correlation, delay variations for the components in a timing path would cancel each other and result in smaller path delay deviation. A larger spatial correlation results in a larger path delay variation.

The critical path delays have a positive skewness $\gamma_1$, i.e., their distributions have a longer right tail than a left tail. The skewness $\gamma_1$ of the critical path delay decreases as the spatial correlation decay rate decreases, i.e., an increased spatial correlation results in an increasingly symmetric path delay distribution.

We observe constant mean, increased standard deviation and decreased skewness of a signal propagation path delay for a decreased spatial correlation decay rate. Delay variations for other signal propagation paths are similar, i.e., the absolute locations and the orientations of the gates in the paths do not affect random variations in a homogeneous isotropic field, while the scale of the distances between the gates in a timing path can be translated to the scale of the spatial correlation decay rate $\alpha$, i.e., placing the gates in a path closer to each other is equivalent to scaling down $\alpha$, which implies a larger path delay variation.

For efficiency, we can construct approximated functions of path delay deviations in terms of spatial correlation decay rates, e.g., by least mean square regression based on SPICE simulation results for sampled spatial correlation decay rates. For example, I approximate the standard deviation for the path delay of 30 combinational logic gates in the experiment as follows (Fig. 2).

$$\sigma = 61.86\alpha^2 - 102.5\alpha + 90.85$$

(7)

where $\alpha$ is the spatial correlation decay rate for gate channel length $L_{\text{gate}}$ and interconnect width $w_{\text{int}}$ ($\alpha = 0$ for transistor threshold voltage $V_{\text{th}}$).

Based on the functions of path delay deviations in spatial correlation decay rates, we can apply regression techniques and find process parameter spatial correlation decay rates which best fit the path delay distributions obtained from production chip performance measurement. The achieved spatial correlations can then be taken into account in statistical physical design optimization techniques, e.g., placement and gate sizing, in a successive chip tapeout process.

The proposed spatial correlation extraction technique is quite efficient. It takes 0.61s to simulate a homogeneous isotropic random field and generate a set of corners for 30 locations, and 2.05s for SPICE simulation to conduct transient analysis across a 5000ps time frame with 1ps time step, on an i686 Linus system with a 2.8GH z processor.
and 512MB memory. Finding an approximated quadratic function for path delay standard deviation $\sigma$ of spatial correlation decay rate $\alpha$ takes linear time of the number of samples. The runtime of regression for best fit spatial correlation decay rates $\alpha$ is given by the number of path delays and the number of process parameter variations, which can be bounded for accuracy-efficiency tradeoff.

5 Conclusion

Spatial correlation is critical to VLSI timing critical path delay variation. In this paper, I propose spatial correlation extraction based on production chip performance statistics. I adopt the homogeneous isotropic random field model for the on-chip variations, and propose a fast Fourier transform (FFT) based random field simulation technique to generate variation corners for Monte Carlo SPICE simulation of a timing critical path delay. In this paper, I propose spatial correlation optimization, e.g., in a successive chip tapeout process.

References