Abstract

This paper presents a time-domain jitter expansion technique for high-speed digital bit sequence jitter testing. While jitter expansion has been applied to phase noise measurements of sinusoidal signals before, its applicability to random clock jitter testing and data-dependent jitter testing have not been explored. The latter problems have wide application and necessitate new analysis procedures given in this paper. Since low phase noise sinusoids can be generated relatively easily as compared to low jitter digital clocks, the proposed technique utilizes a low-frequency sine wave as a reference signal which can be fed to the device under test with less concern for reference signal noise. A special circuit called a jitter-sensor is used for jitter extraction and produces a low-speed output signal with higher jitter values that track the jitter of the high-speed digital test signal. Thus, conventional narrow-bandwidth testers are able to analyze the sensor output. This allows high resolution jitter testing for high-speed digital signals possible at low cost.

1. Introduction

Jitter testing is essential for ensuring signal integrity of high-speed digital devices. As data rates increase, timing accuracy becomes critical and jitter budget gets tighter. However, performing precise jitter testing for a high-speed bit stream from communication devices such as a Serializer/Deserializer is challenging. Instead of testing jitter, bit error rate (BER) testing is considered as a system-level test method to verify high-speed digital communication systems. However, BER testing is expensive in terms of test time [1]. Modern digital communication systems are designed for very low BER (less than $10^{-12}$) and a repeatable test needs to detect 100 bit errors at least. To put this in perspective, a BER test will take 2.5 hours to detect a single bit error from a 10 Gbps signal with a BER of $10^{-15}$ [2]. In addition, most BER tests are performed on carefully tailored high-performance test equipment. Due to the expense associated with conventional BER test procedures, jitter testing is emerging as a feasible way to predict BER.

To measure jitter, combinations of spectrum analyzers, digital oscilloscopes, etc, are typically used [3]. Since jitter is a timing spec, frequency domain measurements must be mapped to the time domain or else stable high-speed triggering and sampling circuits must be used for direct time domain measurements. However, ensuring stability of time-based test setups even on test benches is not an easy problem to solve due to the complexity of a typical jitter testing setup. As an example, a mixer-based jitter test system utilizes mixers, variable oscillators, filters, power detectors, etc. which are very similar to the components used in a phase noise meter. A time-based test system needs complex timing circuits including sampler, trigger, etc. Integrating these functions fully on the load board of a jitter tester is a challenging problem. If these functions are implemented on the back-end of an automatic test environment (ATE), noise from transmission channels between load-boards and ATEs is a concern. Thus, implementing a complex jitter test setup in a production test environment is difficult. Many jitter (or phase noise) test systems utilize a highspeed reference signal. For example, oscilloscope-based techniques need a high-speed digital clock or a sine wave as a reference sampling clock. A mixer-based jitter tester also uses an at-speed sine wave to mix down the input jittery signal. However, jitter or phase noise of the reference signal itself is one of the major factors limiting jitter testing accuracy. In addition, a high-speed reference signal with low jitter is relatively hard to source from a tester (at reasonably low cost). In comparison, a clean low-frequency reference signal can be generated and distributed easily on the tester load board itself. In summary, current jitter testing is limited by (1) the resolution with which jitter can be measured, (2) the cost
of conventional jitter measurement test setups and (3) the effects of the test environment on the accuracy of the jitter testing procedures.

To overcome these issues, we propose a new jitter test technique for digital signals (clocks and digital data streams). The proposed technique does not sample or trigger a high-speed input signal directly. It rather couples the digital input signal to a reference signal, in this case a sine wave, and then analyzes the envelope of the coupled signal. The technique results in jitter expansion which has been shown earlier to measure phase noise of sinusoidal signals. One of the possible setups for processing the resulting test signal from the envelope detector is to sample/digitize the detector output, and then analyze the data in a digital signal processor (DSP). The sensor output is at low-frequency, so a low-speed analog-to-digital converter (ADC) is enough to sample the sensor output signal. Thus, the proposed technique makes the overall test setup significantly simpler by avoiding the demanding needs of high-speed data acquisition. In addition, the sensor has promise for on-chip or on-board implementation because of its simplicity. Jitter expansion through the sensor enables high-resolution jitter testing. Jitter expansion consists of generating a low-speed signal at the output of the sensor with larger values of jitter than the high-speed test signal whose jitter is being measured in such a way that the jitter of the resulting low-frequency signal shows perfect correlation with the jitter of the original high-speed signal. (In essence, the resulting low-speed signal contains an amplified value of the original high-speed signal jitter.) The sensor output is already at low-speed and contains expanded jitter. When sampling this sensor output signal using a low-speed ADC, any sampling error or limited sampling rate does not directly degrade overall jitter test resolution because of the jitter expansion effect. Thus, the proposed sensor enables high-resolution jitter testing. In the proposed test setup, a low-frequency sine wave is applied as a reference. In terms of signal integrity, feeding a low-speed signal into the sensor can be performed with less effort. In addition, a sine wave is considered as a reliable reference compared to others such as clock or ramp signal. The low-frequency sine wave reference reduces a concern for measurement noise due to noisy reference signal. Another key contribution of our technique is that it enables data-dependent jitter (DDJ) testing for a digital bit sequence. When a preset bit pattern is applied to the sensor, random and data-dependent jitter values are obtained from the sensor output signal at the same time.

2 Jitter expansion analysis

2.1 Previous work

Jitter expansion technique described in [4] enables a high-resolution jitter test by expanding (amplifying) sub-picosecond clock jitter through a sensor more than 1000 times. The proposed sensor converts jitter from the high-speed input signal to amplified (expanded) jitter in the low-speed output signal. To enable frequency conversion and jitter scaling between the input and the output of the sensor, the reference signal which is applied to the other input port of the sensor should have a small frequency offset compared to the jittery high-speed input signal: signal under test (SUT). Using this test method, one can observe much larger amount of jitter at the low-frequency output of sensor compared to that of the original high-speed input signal. It is called jitter expansion in [4]. A scaling factor of jitter expansion is determined by the frequency of two inputs. Thus, jitter values obtained from the sensor output signal is directly related to those of the original high-speed input.

Table 1. Definition of variables

<table>
<thead>
<tr>
<th>Variable</th>
<th>Definition</th>
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<tbody>
<tr>
<td>$A_c$</td>
<td>Clock amplitude</td>
</tr>
<tr>
<td>$A_r$</td>
<td>Reference signal amplitude</td>
</tr>
<tr>
<td>$T_c$</td>
<td>Clock period</td>
</tr>
<tr>
<td>$T_r$</td>
<td>Reference signal period</td>
</tr>
<tr>
<td>$\tau_c$</td>
<td>Clock time constant</td>
</tr>
<tr>
<td>$f_c(\omega_c)$</td>
<td>Clock (angular) frequency</td>
</tr>
<tr>
<td>$f_r(\omega_r)$</td>
<td>Reference signal (angular) frequency</td>
</tr>
<tr>
<td>$f_{os}(\omega_{os})$</td>
<td>Offset (angular) frequency</td>
</tr>
<tr>
<td>$k$</td>
<td>The time-based window number</td>
</tr>
<tr>
<td>$t$</td>
<td>Time</td>
</tr>
<tr>
<td>$t_k$</td>
<td>Time in $k^{th}$ time-based window</td>
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<tr>
<td>$t_k^*$</td>
<td>The time where $S(t_k)$ peaks in voltage</td>
</tr>
<tr>
<td>$\Delta t_k$</td>
<td>The timing error of $D(t_k)$ in $k^{th}$ time-based window</td>
</tr>
<tr>
<td>$C_r(\cdot)$</td>
<td>Clock rising edge</td>
</tr>
<tr>
<td>$C_{rj}(\cdot)$</td>
<td>Jittery clock rising edge</td>
</tr>
<tr>
<td>$C_f(\cdot)$</td>
<td>Clock falling edge</td>
</tr>
<tr>
<td>$R(\cdot)$</td>
<td>Reference signal</td>
</tr>
<tr>
<td>$S(\cdot)$</td>
<td>Coupled signal of $D_r(\cdot)$ and $R(\cdot)$</td>
</tr>
<tr>
<td>$S_j(\cdot)$</td>
<td>Coupled signal of $D_{rj}(\cdot)$ and $R(\cdot)$</td>
</tr>
<tr>
<td>$u(\cdot)$</td>
<td>Step function</td>
</tr>
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</table>
signal with a known scaling factor.

2.2 Clock jitter expansion with at-speed reference

In this section, we revise the jitter expansion analysis. The previous publication [4] addressed the jitter expansion with a single-tone assumption where a jittery clock was described as a sine wave with phase noise. The single-tone assumption simplifies the analysis, but does not fully represent actual clock signal transients. In this paper, we analyze the jitter expansion effect using rising/falling formula derived from a lumped RC interconnect model to remove the single-tone assumption. The lumped RC model introduces clock rising/falling transitions as below,

\[ C_r(t) = A_c(1 - e^{-\frac{t}{\tau_c}})u(t), \]
\[ C_f(t) = A_c(1 - e^{-\frac{t}{\tau_c}})u(t) - A_c(1 - e^{-\frac{t-\frac{T_c}{2}}{\tau_c}})u(t-\frac{T_c}{2}). \]  

Figure 2 illustrates a time-based window through which signals are observed cycle by cycle. The window width is adjusted to fit the period of the clock denoted as (a). When the clock does not contain jitter, every cycle of the clock presents at the same position of the window. On the other hand, a jittery clock appears at various positions due to timing deviation.

A reference sine wave is denoted as (b), and its frequency is close to that of the clock. However, the two signals (a) and (b) are chosen to have a small frequency offset. Due to the offset, the reference signal period does not fit within the window width. When observing the reference window-by-window, it drifts relative to the clock at fixed rate determined by the offset frequency. Equation 3 represents the reference signal shown in a single window. The period difference between the reference and the clock \( T_r - T_c \) is the amount of drift over a single window. Thus, total drift at time \( t \) is calculated as the observed number of windows \( k \) multiplied by a single window drift \( T_r - T_c \). The reference signal is denoted as,

\[ \frac{dS(t_k^*)}{dt_k} = \frac{A_c}{\tau_c} e^{-\frac{t_k^*}{\tau_c}} - A_r \omega_r \sin(\omega_r(t_k^* - k(T_r - T_c))). \]  

From Equation 4 and 5, the corresponding peak value of the coupled signal is solved as shown in Equation 6.

\[ S(t_k^*) = A_c(1-e^{-\frac{t_k^*}{\tau_c}})u(t_k^*) + A_r \cos(\omega_r(t_k^* - k(T_r - T_c))). \]  

\[ S(t_k^*) \] is a discrete function of \( k \) as shown in Figure 3. We call it the envelope function.

So far, we have performed the analysis for a non-jittery clock. Next, we consider the case where jitter exists in the clock. The jittery clock does not present itself at the same position of the window over time. Due to \( \Delta t_k \), timing variation of the clock in the \( k^{th} \) window, the clock position varies in the horizontal direction. The jittery clock (rising edge only) is modeled as below,

\[ C_{rj}(t_{k'}) = A_c(1 - e^{-\frac{t_{k'} - \Delta t_{k'}}{\tau_c}})u(t_{k'} - \Delta t_{k'}). \]  

Assuming the reference signal does not have phase noise, Equation 8 represents the ‘jittery’ coupled signal.

\[ S_{j}(t_{k'}) = A_c(1-e^{-\frac{t_{k'} - \Delta t_{k'}}{\tau_c}})u(t_{k'} - \Delta t_{k'}) + A_r \cos(\omega_r(t_{k'} - k'(T_r - T_c))). \]  

For analysis, the reference signal is coupled to the clock through a RF transformer. The sum of two signals in Equation 4 describes the coupling effect. The coupled signal has a unique shape that depends on two input signals: the clock and the reference. The shape of the coupled signal is not the same across all observation windows. Due to effect of the reference drift and the clock jitter, the couple signal has timing deviation within the window.

\[ R(t) = A_c \cos(\omega_r(t - k(T_r - T_c))). \]  

\( R(t) \) is a function of \( t \) and \( k \).
The peak voltage of the signal is then solved as below.

\[ \frac{dS_j(t_k^{**})}{dt_{k'}} = A_c \cdot e^{-\frac{t_k^{**} - \Delta t_{r'}}{T_c}} - A_r \cdot \omega_r \cdot \sin(\omega_r \cdot (t_k^{**} - k'(T_r - T_c))) \]  

(9)

The peak voltage of the signal is then solved as below.

\[ S_j(t_k^{**}) = A_c + A_r \cdot \cos(\omega_r \cdot t_k^{**} - k' \cdot \omega_r(T_r - T_c)) \]

\[ -T_c \cdot \omega_r \cdot A_r \cdot \sin(\omega_r \cdot t_k^{**} - k' \cdot \omega_r(T_r - T_c)) \]  

(10)

Note that two envelope functions \( S(t_k^*) \) and \( S_j(t_k^{**}) \), one without jitter and the other with jitter respectively, have different slopes with respect to each other as seen in Figure 4.

Finally, we measure jitter from the ‘jittery’ envelope function \( S_j(t_k^{**}) \) which has timing deviation due to the input clock jitter. In comparison, \( S(t_k^*) \) does not hold jitter because it is generated from the non-jittery clock. By applying a reference DC voltage as shown in Figure 4, two level crossing points are found. \( S(t_k^*) \)'s level crossing time is ideal without any timing error. However, \( S_j(t_k^{**}) \)'s crossing point has the effect of timing jitter.

To compute the timing error of \( S_j(t_k^{**}) \), we set the condition of \( S_j(t_k^{**}) = S(t_k^*) \). From Equation 6 and 10, we derive the below.

\[ \omega_r \cdot (t_k^* + k'T_c) = \omega_r \cdot (t_k^{**} + k'T_c) + 2N\pi \]  

(11)

where \( N \) is an integer. From Equation 5 and 9, we get

\[ t_k^{**} = t_k^* + \Delta t_{k'} \]  

(12)

where \( k' = k + \Delta k \). Applying Equation 12 to Equation 11 and letting \( N = -\Delta k \), we get

\[ \frac{\Delta kT_c}{\Delta t_{k+\Delta k}} = T_c \cdot \frac{T_c}{T_r - T_c} \]  

(13)

where \( \Delta kT_c \) is the timing error of \( S_j(t_k^{**}) \) in seconds. Equation 13 represents the ratio of the sensor output envelope jitter \( \Delta kT_c \) and the sensor input clock jitter \( \Delta t_{k+\Delta k} \). Therefore, the jitter expansion is performed through the sensor with a known scaling factor \( T_c \cdot \frac{T_c}{T_r - T_c} \).

2.3 Clock jitter expansion with low-frequency reference

We extend the previously described jitter expansion technique to low-frequency reference cases. As illustrated in Figure 5, the reference signal of frequency \( f_r = f_{os} \) can be coupled to the digital clock with frequency \( f_c \), where \( f_{os} \) is the small frequency offset. To analyze the case of \( f_r = \frac{f_c}{n} - f_{os} \), the time-based window should be doubled in width compared to the previous case. In the same manner, for a reference of \( f_r = \frac{f_c}{n} - f_{os} \) the time window is four times longer. The rest of the analysis is the same as the previous described at-speed reference case. The extended analysis results in the jitter expansion ratio for the case of \( f_r = \frac{f_c}{n} - f_{os} \) as \( \frac{nT_c}{T_r - nT_c} \) where \( n = 1, 2 \) or 4.

3 Applications: digital bit streams

Data-dependent jitter (DDJ) is a type of deterministic jitter which only appears in digital bit streams. Limited bandwidth or impedance mismatches in the digital system causes DDJ to the bit sequence [5]. As shown in Figure 6, the bit sequence has amplitude variation due to limited bandwidth. When digital bits toggle at low-frequency, the voltage goes fully high or low. However, high-frequency bit switching does not allow the voltage to go fully high or low. This amplitude variation eventually causes DDJ. It should be noted that DDJ is assumed to be independent to random jitter (RJ) [5].

In this section, we apply the previously described jitter expansion technique to a bit sequence (preset pattern). In terms of analysis, the main difference compared to the clock jitter case is that the size of the time window. To analyze jitter of the bit pattern of length \( n \), a window length of \( \frac{n}{2} \) is required. A low-frequency signal such as \( f_r = \frac{f_{os}}{n} \) is preferred to at-speed reference \( f_c - f_{os} \) for ease of generation. For a certain types of bit patterns, the at-speed reference signal makes the dynamic range of the envelope function too small. For experiment, we utilize an 8-bit pattern. Longer bit patterns re-
duce the dynamic range of the envelope. An arbitrary combination of the 8 bits can be chosen and the pattern is applied to the input of the RF coupler. The other input of the coupler is fed by a low-speed reference signal whose frequency is $f_{os}$. The observation window is four times wider than that of the at-speed reference case. Once we apply the coupled signal to the envelope detector, this sensor generates the low-speed envelope function which contains jitter originated from the bit sequence. Some part of the envelope represents jitter of a particular bit edge while other part of the envelope holds the other edge’s jitter. To distinguish jitters which come from different bit transitions, we conduct the following computer simulation.

4 Simulation

In this simulation setup, we evaluated the jitter expansion of the bit sequence. 1 GHz jittery bit sequence 11101100 was coupled to a 249 MHz reference sine wave. Note that, here the reference signal frequency is further reduced to $f_{os}$. Figure 6 illustrates the accumulated view (625,000 cycles) of the bit sequence 11101100. Dispersion of the waveform in time is due to its jitter. First, we obtained level (reference DC voltage) crossing time data from two rising edges of the sequence denoted by (a) and (b). Timing error from each signal edge is random. However, the mean of timing error from (a) is not the same as that from (b) due to DDJ. Jitter histogram in Figure 7 represents random jitter obtained from (a) and (b) separately. Sample set (a) and (b) contain 10.01 psec RMS and 10.00 psec RMS random jitter respectively, and the distance between their mean values is 15.78 psec which corresponds to DDJ. Figure 8 shows the corresponding envelope waveform. This accumulated plot contains 2,500 cycles of the envelope. Time dispersion of the plot is due to the envelope jitter which is originated from the input bit sequence jitter. By applying a reference level to the envelope, two data sets of level crossing timing error (a) and (b) are obtained as shown in Figure 9. Sample set (a) and (b) hold 2,490.23 psec RMS and 2,490.08 psec RMS respectively with the mean distance 3,930.31 psec. Thus, jitter from the envelope signal is 249 ($= \frac{47}{4T_c - 4T_r}$) times larger than that of the original bit sequence.

5 Hardware measurement

We implemented the hardware test setup shown in Figure 1. The sensor including a RF coupler and an envelope de-
tector was designed on a printed circuit board. To generate a bit sequence with jitter injection, a pattern generator (Mircowave Logic GigaBert 1400Tx) was used with an external clock delivered from another signal generator (Agilent E4432B). Depending on the amount of phase noise of the Agilent E4432B RF output, the GigaBert 1400Tx generates output data with the corresponding jitter. In addition, the reference signal was derived from Agilent 83623B, and the sensor output was digitized using Alazartech AT460 Digitizer (14-Bit, 125 MS/s). In this hardware measurement section, we verify jitter testing resolution of the proposed technique. To do so, we inject a small amount of additional jitter to the bit sequence, and then observe the change of the digitized sensor output signal in terms of jitter value. For a non-jittery input bit stream, the bit sequence of 11101100 was generated from the pattern generator without any modulation. In comparison, a jittery bit sequence 11101100 was generated by modulating phase noise of 0.005 rad RMS, equivalent to 0.568 psec RMS, for the Agilent E4432B RF output. For the reference signal, a 349 MHz ($= f_c - f_{os}$) sine wave is utilized, while the bit sequence is at speed of 2.8 Gbps.

To illustrate jitter effect in details, a small part of the digitized envelope signal (without jitter injection) is shown in Figure 10 with jitter histogram. Jitter of this envelope signal measures 1.350 nsec RMS. In comparison, Figure 11 shows the digitized envelope signal for jitter injection case. Jitter of this envelope signal measures 1.370 nsec RMS. Injected jitter of 0.568 psec RMS is amplified to 0.198 nsec RMS jitter at the output of the sensor. Assuming that injected jitter is independent of jitter from other sources or measurement noise, computed value of the injected jitter is 0.660 psec RMS. Note that this computed value of 0.660 psec RMS is close to the injected jitter of 0.568 psec RMS in sub-picosecond range. Thus, hardware results demonstrate the effectiveness of the proposed approach in measuring the jitter of digital data pattern through jitter expansion.

6 Conclusion

We analyzed jitter expansion effect of the proposed test technique for digital signals including clocks and digital data bit streams. To mitigate the requirement of a high frequency reference signal, a low-frequency reference signal is utilized. In computer simulations, the expanded jitter of the low frequency signal showed perfect correlation with jitter of the high-speed signal. Hardware measurements demonstrate the sub-picosecond jitter testing resolution of the proposed technique. Thus, the proposed approach is simple, low-cost and effective for measuring the jitter of clock signals and digital data bit streams.

References