Design Guidelines for Metallic-Carbon-Nanotube-Tolerant Digital Logic Circuits

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Abstract
Metallic Carbon Nanotubes (CNTs) create source-drain shorts in Carbon Nanotube Field Effect Transistors (CNFETs), causing excessive leakage, degraded noise margin and delay variation. There is no known CNT growth technique that guarantees 0% metallic CNTs. Therefore, metallic CNT removal techniques are necessary. Unfortunately, such removal techniques alone are imperfect and insufficient. This paper demonstrates the necessity for co-optimization of processing techniques for metallic CNT removal together with CNFET-based circuit design. We present a probabilistic CNFET circuit model which forms the basis for such co-optimization, and use the model to derive design and processing guidelines that enable design of CNFET-based digital circuits with practical constraints on leakage, noise margin and delay variations. These guidelines are essential for designing robust metallic-carbon-nanotube-tolerant digital circuits.

1. Introduction
Carbon Nanotube Field Effect Transistors (CNFETs) are promising extensions to silicon CMOS due to their small size and high performance [Guo 04, Javey 04]. Figure 1.1 shows the side view of a CNFET. Parallel Carbon Nanotubes (CNTs) are grown on or transferred to a substrate. The regions of the CNTs under the gate are undoped. The conductivity of these undoped regions is controlled by the gate. The source and drain regions of the CNTs are heavily doped. The gate, source and drain contacts, and interconnects are defined by conventional lithography.

![Figure 1.1. Carbon-Nanotube Field-Effect-Transistor.](image)

Figure 1.2 shows the schematic of a 32 nm CNFET inverter. Note that the inter-CNT distance in the horizontal direction is controlled by the CNT growth process. Hence it is not limited by the minimum lithographic spacing.

![Figure 1.2. Schematic of a CNFET inverter.](image)

An ideal CNFET technology can offer 13X EDP (Energy Delay Product) advantage over 32 nm Silicon CMOS [Deng 07a, Guo 04]. However, a major gap exists between such ideal results and practical CNFET circuits because of fabrication-related imperfections. Major imperfections in CNFET technology include the presence of misaligned CNTs and metallic CNTs. [Patil 07] describes a technique to design digital logic circuits that function correctly in the presence of misaligned CNTs. Metallic CNTs remain a major barrier to CNFET technology.

A CNT can be either metallic (m-CNT) or semiconducting (s-CNT). We denote \( p_m \) and \( p_s \) (where \( p_s = 1 - p_m \)) as the average fraction of m-CNTs and s-CNTs, respectively, within an ensemble of CNTs. A typical growth process produces CNTs with \( p_m = 1/3 \) and \( p_s = 2/3 \) [Saito 98]. The conductivity of an m-CNT cannot be controlled by the gate voltage. Hence, an m-CNT causes a short between the source and drain of a CNFET, resulting in excessive leakage and/or digital logic gate malfunction (with severely degraded noise margin). Hence, m-CNTs are undesirable for CNFETs. Since no known CNT growth technique guarantees to produce exclusively s-CNTs, m-CNTs must be removed after CNT growth.

Two major techniques for selectively removing m-CNTs from an ensemble of m-CNTs and s-CNTs are:
1. Current-induced electrical burning [Collins 01]: This approach is not scalable for large-scale VLSI systems since it involves individually contacting and breaking down m-CNTs in each CNFET.
2. Selective chemical etching [Zhang 06]: This approach is scalable and can be integrated with VLSI semiconductor processing. Experimental results also show a very high removal rate [Zhang 06]. Therefore, we focus on this technique in this paper.

The basic principle of selective chemical etching is to remove m-CNTs whose diameters are smaller than a certain cut-off diameter \( c_m \); however, the etching also has a similar effect on s-CNTs but with a different cut-off diameter \( c_s \) (Fig. 1.3). The net effect is summarized below:

1. All CNTs with diameters less than \( c_s \) are etched away;
2. Only s-CNTs with diameters between the two cutoffs \( c_s \) and \( c_m \) survive the etching process;
3. All CNTs with diameters greater than \( c_m \) survive.

For an ideal selective chemical etching process, \( c_s = 0 \) and \( c_m \rightarrow \infty \), meaning that all s-CNTs are preserved while all m-CNTs are removed. Unfortunately, actual etching processes are not ideal. For example, [Zhang 06] reports \( c_m = 2 \) nm and \( c_s = 1.4 \) nm for a range of CNT diameters between 1 nm and 2.8 nm. Hence, the following two questions must be answered for designing metallic-CNT-tolerant digital logic circuits:

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1 m-CNTs are actually “cut into pieces” instead of being “removed” during selective chemical etching [Zhang 06].
1. **Processing question:** What $p_m$, $c_m$ and $c_s$ values must be satisfied for designing CNFET circuits with practical constraints on leakage, noise margin and delay variation?

2. **Design question:** Determine $N_{\text{min}}$, the minimum number of CNTs per CNFET prior to etching (for specified values of processing parameters ($p_m$, $c_m$ and $c_s$)), such that the aforementioned constraints are satisfied.

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**Figure 1.3. Simple Model for Selective Chemical Etching.**

Major contributions of this paper are:

1. A probabilistic model is introduced for analyzing the effects of m-CNTs on circuit performance metrics such as leakage, noise margin and delay variation.

2. Quantitative bounds and sensitivities of processing ($p_m$, $c_m$ and $c_s$) and design ($N_{\text{min}}$) parameters are derived to answer the above questions. Table 1 presents a qualitative summary of these sensitivities.

**Table 1. Sensitivities of circuit performance metrics to processing and design parameters.**

<table>
<thead>
<tr>
<th></th>
<th>Leakage</th>
<th>Noise Margin</th>
<th>Delay Variation</th>
</tr>
</thead>
<tbody>
<tr>
<td>$c_m$</td>
<td>Very strong</td>
<td>Very strong</td>
<td>Weak</td>
</tr>
<tr>
<td>$c_s$</td>
<td>Weak</td>
<td>Strong</td>
<td>Strong</td>
</tr>
<tr>
<td>$p_m$</td>
<td>Weak</td>
<td>Strong</td>
<td>Strong</td>
</tr>
<tr>
<td>$N^*$</td>
<td>Weak</td>
<td>Strong</td>
<td>Strong</td>
</tr>
</tbody>
</table>

* $N$ is the number of CNTs per CNFET prior to etching.

Section 2 details the detrimental effects of m-CNTs on CNFET circuit performance metrics – leakage, noise margin and delay. A probabilistic model is presented in Sec. 3 for analyzing the effects of non-ideal m-CNT removal on CNFET circuit performance. Based on this model, Sec. 4 identifies the most important parameters for each circuit performance metric, analyzes their effects quantitatively and provides simple design and processing guidelines. Section 5 concludes this paper.

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**2. Detrimental Effects of Metallic CNTs on CNFET Circuits**

We use a CNFET SPICE model implemented including device non-idealities [Deng 06] with a 32 nm CNFET technology. This SPICE model has been calibrated to experimental data with greater than 90% accuracy [Amlani 06]. The supply voltage is fixed at 0.9V for this technology node [ITRS 06]. The average fraction of m-CNTs ($p_m$) is 1/3 unless otherwise specified [Saito 98]. The inverter layout style in Fig. 1.2 is used where the same set of CNTs are used in pull-up (p-type) and pull-down (n-type) devices. Thus, the number of CNTs and their types (m- or s-) are the same for pull-up and pull-down CNFETs.

### 2.1 Leakage

The off-current of a CNFET dramatically increases due to the presence of m-CNTs resulting in excessive leakage. While s-CNTs alone can achieve very high $I_{\text{on}}/I_{\text{off}}$ of $10^4$ to $10^6$ [Chen 05, Zhang 06], a mixture of m- and s-CNTs severely degrades it. The $I_{\text{on}}/I_{\text{off}}$ ratio of a mixture of both types of CNTs is:

$$\frac{I_{\text{on}}}{I_{\text{off}}} = \frac{N_i I_{s,\text{on}} + N_m I_{m,\text{on}}}{N_i I_{s,\text{off}} + N_m I_{m,\text{off}}} \quad (2.1)$$

where $N_i$ and $N_m$ are the numbers of s- and m-CNTs, respectively. According to the assumption that $p_m = 1/3$, we have $N_i/N_m = 2$ on average. $I_{s,\text{on}}$ is the s-CNT current when $V_{gs} = V_{ds} = V_{\text{supply}}$, $I_{s,\text{off}}$ is the s-CNT current when $V_{gs} = 0$ and $V_{ds} = V_{\text{supply}}$ and $I_m$ is the m-CNT current when $V_{gs} = V_{\text{supply}}$. Typically, $I_m > I_{s,\text{on}} > I_{s,\text{off}}$ and the difference between $I_m$ and $I_{s,\text{on}}$ is a strong function of CNT diameter and the CNT-source/drain contact interface [Javey 04]. Even under the optimistic assumption that $I_{s,\text{on}} = I_m$ in (2.1), $I_{\text{on}}/I_{\text{off}}$ is only 3 for CNFET if no m-CNT removal techniques are applied. This number is orders of magnitude smaller than desired values of $I_{\text{on}}/I_{\text{off}}$, e.g., 6,000 for high performance and $5\times10^7$ for low standby power applications based on current silicon CMOS technology [ITRS 06].

### 2.2 Gate Robustness and Noise Margin

We use static noise margin (SNM) as a metric for the robustness of a logic gate. SNM is defined as the maximum square between the normal and mirrored voltage transfer curves (VTCs) [Hill 68]. Figure 2.1 shows simulated VTCs for two CNFET inverters ($N = 100$). Figure 2.1a is the VTC of a CNFET inverter with 0% m-CNTs. An SNM of > 3/8 * $V_{\text{supply}}$ is measured from the curve. Figure 2.1b shows the VTC of a CNFET inverter with 33% m-CNTs without performing any etching. This inverter does not give a full rail-to-rail output, which reduces the gain as well as the noise margin. The VTC in Fig. 2.1b has a SNM of zero.

![Fig 2.1. Simulated Voltage Transfer Curve of CNFET inverters.](image)

**Fig 2.1. Simulated Voltage Transfer Curve of CNFET inverters.**

### 2.3 Delay

The delay of a CNFET gate can be estimated by:

$$\text{delay} = \frac{C_{\text{load}} V_{\text{supply}}}{I_{\text{drive}}} \quad (2.2)$$

Consider a $1 \rightarrow 0$ output transition from a $0 \rightarrow 1$ step input at the input of an inverter and a fixed load. The drive current is given by:

$$I_{\text{drive}} = I_{\text{pulldown}} + I_{\text{pullup}} = I_{s,\text{pulldown}} + I_{m,\text{pulldown}} - I_{m,\text{pullup}} \quad (2.3)$$

Since pull-up s-CNTs are turned off, their currents are neglected. An m-CNT essentially acts as a resistor, so its current depends on the voltage across it. If we consider the $V_{\text{supply}}/2 \rightarrow V_{\text{supply}}$ transition time as the propagation delay, pull-down m-CNTs have larger voltage drop across them compared to the pull-up m-CNTs. Thus, the net m-CNT current is in favor of...
the s-CNT current drive. Figure 2.2 shows that with $p_m=33\%$ and no m-CNT removal, a mean delay reduction of nearly 30\% can be observed by simulation. However, this mean delay benefit cannot be utilized in a practical design because m-CNTs severely aggravate leakage and noise margins, as discussed in Sec. 2.1 and 2.2.

Compared with mean delay, delay variations can be a bigger challenge in the presence of m-CNTs. Because whether a CNT is metallic or semiconducting is totally stochastic, the ratio of the number of m-CNTs to the number of s-CNTs differs from gate to gate (the parameter $p_m$ only specifies the average ratio). Error bars in Fig. 2.2 show that standard deviation is 10\%~15\% of mean delay for the above-mentioned inverter with $p_m=33\%$ and no m-CNT removal. Additional variation is introduced when selective etching is applied (see Sec. 3).

3. Probabilistic Model of Imperfect CNFET Logic Gates with Metallic CNTs

3.1. Single-CNT CNFETs

Both s- and m-CNTs have diameter distributions. We use probability density functions, $f_{md}(x)$ and $f_{sd}(x)$, to model diameter distributions of m-CNT and s-CNT respectively.\(^2\) For s-CNT, the drive current increases with its diameter [Deng 07b]. Denote $I_s(x)$ to be the current of an s-CNT of diameter $x$. The mean and variance of the s-CNT current is then given by:

$$\mu(I_s) = \int_0^{c_s} I_s(x)f_{sd}(x)dx \quad \text{(3.1)}$$

$$\sigma^2(I_s) = \int_0^{c_s} [I_s(x) - \mu(I_s)]^2 f_{sd}(x)dx \quad \text{(3.2)}$$

Current through an m-CNT ($I_m$) remains nearly constant for all practical diameters assuming ohmic contacts [Deng 07b]. Therefore, the mean and variance of $I_m$ are:

$$\mu(I_m) = \int_0^{c_m} I_m f_{md}(x)dx = I_m \quad \text{(3.3)}$$

$$\sigma^2(I_m) = \int_0^{c_m} [I_m - \mu(I_m)]^2 f_{md}(x)dx = 0 \quad \text{(3.4)}$$

The selective chemical etching technique, described in Sec.1, can be modeled using a function $e(x)$ of a CNT of diameter $x$. The etching function $e(x)$ is the probability that a CNT of diameter $x$ is removed during etching. In order for an etching process to selectively etch m-CNTs, this etching function must be different for m- and s-CNTs, denoted as $e_m(x)$ and $e_s(x)$, respectively. Therefore, the mean current of both types of CNTs after etching are:

$$\mu(I_e) = \int_0^{c_s} I_s(x)[1-e_s(x)]f_{sd}(x)dx \quad \text{(3.5)}$$

$$\mu(I_m) = \int_0^{c_m} I_m f_{md}(x)dx \quad \text{(3.6)}$$

For brevity, we assume a first-order simplification and represent etching functions as step functions below:

$$e_s(x) = \begin{cases} 1 & (x < c_s) \\ 0 & (x \geq c_s) \end{cases} \quad e_m(x) = \begin{cases} 1 & (x < c_m) \\ 0 & (x \geq c_m) \end{cases} \quad \text{(3.7)}$$

Parameters $c_s$ and $c_m$ are referred to as cutoff diameters. This first-order model is equivalent to the one described in Fig. 1.3. Using this model, the expressions for mean currents of both types of CNTs become:

$$\mu(I_s) = \int_0^{c_s} I_s(x)f_{sd}(x)dx \quad \text{(3.8)}$$

$$\mu(I_m) = \int_0^{c_m} I_m f_{md}(x)dx \quad \text{(3.9)}$$

The variances of these currents are:

$$\sigma^2(I_s) = \int_0^{c_s} I_s^2(x)f_{sd}(x)dx - \left[\int_0^{c_s} I_s(x)f_{sd}(x)dx\right]^2 \quad \text{(3.10)}$$

$$\sigma^2(I_m) = \int_0^{c_m} I_m^2 f_{md}(x)dx - \left[\int_0^{c_m} I_m f_{md}(x)dx\right]^2 \quad \text{(3.11)}$$

The above results for s-CNTs and m-CNTs can be combined to give the mean and variance of single CNT current:

$$\mu(I_{CNT}) = p_s \mu(I_s) + p_m \mu(I_m) \quad \text{(3.12)}$$

$$\sigma^2(I_{CNT}) = \mu^2(I_{CNT}) - \mu^2(I_s) - \mu^2(I_m) \quad \text{(3.13)}$$

The values of $\mu(I_s), \mu(I_m), \sigma(I_s), \sigma(I_m)$ in (3.12) and (3.13) can be calculated from equations (3.8) – (3.11).

3.2. CNFETs with Multiple CNTs

The current drive of a CNFET with $N$ CNTs is modeled as the sum of $N$ individual random currents, whose statistical properties are studied in (3.12) and (3.13). We assume that the types (m- or s-) and diameters of CNTs are independent, and identically distributed (i.i.d). Simple rules can be used to determine the mean and variance of the current of a CNFET with $N$ CNTs:

$$\mu(I_N) = N\mu(I_{CNT}) \quad \text{(3.14)}$$

$$\sigma^2(I_N) = N\sigma^2(I_{CNT}) \quad \text{(3.15)}$$

where $\mu(I_{CNT})$ and $\sigma(I_{CNT})$ are calculated in (3.12) and (3.13). Note that the $\sigma/\mu$ ratio of $I_N$ decreases by $1/\sqrt{N}$ as a result of the i.i.d assumption.


CNT diameter distributions vary significantly depending on CNT growth techniques. However, Gaussian distribution is commonly used to fit experimental data [Liu 02]. For the purpose of this section, we assume the diameters of both s-CNTs and m-CNTs are normally (Gaussian) distributed with mean ($\mu_d$) = 1.5 nm, and standard deviation ($\sigma_d$) = 0.1 nm. In addition, we discuss the implications of non-Gaussian distributions. We use the models in [Deng 07b] to calculate the current through an s-CNT of diameter $x$, denoted by $I_s(x)$. For practical designs, large $c_m$ and

\(^2\) CNT diameters are discrete. However, the discrete CNT diameters are spaced very closely and can be considered as continuous. Also note that the discussions and results in this paper can also be applied to discrete CNT diameter distributions.
small $c_s$ are desired. Hence, it is reasonable to assume $c_m > \mu_d > c_s$. This assumption is consistent with experimental data [Zhang 06].

### 4.1. Leakage

We estimate the ratio of leakage power to dynamic power in a CNFET circuit by using the $I_{on}/I_{off}$ ratio [Noise 00]. Since power is averaged across the entire chip, it is sufficient to consider only the mean values of $I_{on}$ and $I_{off}$ over all gates. These mean values can be derived from (3.8), (3.9) and (3.12) as:

$$
\mu(I_{on}) = \frac{\int I_{on} f(x) dx}{\int f(x) dx}
\mu(I_{off}) = \frac{\int I_{off} f(x) dx}{\int f(x) dx}
$$

(4.1)

Excessive leakage is caused when the second (m-CNT) term of the denominator is much greater than the first (s-CNT) term of the numerator. In this case, (4.1) can be simplified as:

$$
\frac{\mu(I_{on})}{\mu(I_{off})} = p_m \frac{\int I_{on} f(x) dx}{\int I_{off} f(x) dx} + p_m \frac{\int f(x) dx}{\int f(x) dx}
$$

(4.2)

where $F_{md}(x)$ stands for the cumulative diameter distribution function of m-CNTs. Figure 4.1 shows four $\mu(I_{on})/\mu(I_{off})$ curves versus $c_m$ with different $c_s$ and $p_m$ values. As shown in Fig.4.1, the changes in $c_s$ and $p_m$ do not have a big impact on this ratio compared to the changes in $c_m$. This observation is further confirmed by a sensitivity analysis with respect to $c_m$, $c_s$ and $p_m$ evaluated at point ($c_m=\mu_d+2\sigma_d$, $c_s=\mu_d+2\sigma_d$, $p_m=1/3$). The point is chosen such that its sensitivity values are typical throughout the region of interest. The definition of sensitivity is:

$$
Sensitivity = \frac{\partial}{\partial \text{param}} \left( \frac{\mu(I_{on})}{\mu(I_{off})} \right)
$$

(4.3)

Figure 4.1. $\mu(I_{on})/\mu(I_{off})$ vs. $c_m$ (with s-CNT $I_{on}/I_{off} = 10^5$).

This predominant effect of $c_m$ can also be seen from (4.2), in which the key factor is the tail probability $[1-F_{md}(c_m)]$ in the denominator. This probability is fully determined by $c_m$ given the diameter distribution. For example, when Gaussian distribution is assumed, it can be derived that the tail probability drops faster than $\exp[-(c_m-\mu_d)^2 / 2\sigma_d^2]$ when $c_m$ is large.

The following conclusions can be drawn from this analysis:

1) $I_{on}/I_{off}$ is highly sensitive to $c_m$. For $I_{on}/I_{off}$ values, e.g., $\sim 10^4$ [ITRS 06], the guideline for $c_m$ (assuming Gaussian diameter distribution and $p_m = 1/3$) is:

| Guideline | $c_m > \mu_d + 4\sigma_d$ (Gaussian) |

2) $p_m$ can also help to improve $I_{on}/I_{off}$. However, since the sensitivity of changing $p_m$ is much less than $c_m$, the target ratio can only be achieved when $p_m$ is extremely small.

3) The leakage problem cannot be resolved by changing $c_s$ alone because it does not help to eliminate m-CNTs.

For non-Gaussian CNT diameter distributions, (4.2) can be used to find a similar guideline for $c_m$. Specifically, the value (or range) of $c_m$ must be chosen such that the tail probability of $[1-F_{md}(c_m)]$ is on the order of $1/10^4 = 10^{-4}$, assuming $10^4$ is the targeted $I_{on}/I_{off}$ ratio.

### 4.2. Noise Margin

Suppose that $SNM_{g}$ is the required static noise margin that a logic gate must satisfy. Given a set of processing parameters ($p_m$, $c_m$, $c_s$) and the number of CNTs per CNFET ($N$), we calculate the probability that a gate will fail to satisfy the SNM requirement. We refer to this as $PNMV$ or probability of noise margin violation (PNMV). For simplification, we restrict our discussion to only inverters in this paper. The general analysis technique holds for complex gates as well.

The way to calculate PNMV for inverters is described in the Appendix. Figure 4.2 plots these calculated PNMV with different parameter values. The relative impact of various parameters on PNMV can be explained as follows:

1) $c_m$ has a very strong effect on PNMV (Fig. 4.2(a)). However, beyond a certain range of $c_m$, PNMV stops decreasing and reaches a limit. In this scenario, all the m-CNTs are etched out and very little benefit is gained by further increasing $c_m$. This limit is decided by $p_m$ and $c_s$, as discussed next.

2) $p_m$ and $c_s$ together determine the aforementioned limit of PNMV given a particular $N$. Comparing curves 1 and 2 in (a), it is shown that this limit is not even related to the required noise margin ($SNM_{g}$). This is because in this limit case (when no m-CNT survives etching), the meaning of PNMV is equivalent to “the probability that there is no s-CNT after etching”. If we further assume $c_s = 0$ (ideal etching), then this limit can be easily derived:

$$
PNMV(ideal etching) = P\{#s\text{-CNT} = 0\} = p_m^N
$$

(4.5)

Figure 4.2. (a) PNMV vs. $c_m$. (b) PNMV vs. $N$ ($SNM_r = V_{dd}/4$).

When all process parameters are fixed, design parameter $N$, the number of grown CNTs per CNFET, can be used to achieve required levels of $SNM_{g}$, as shown in Fig.4.2b. This is because
larger $N$ protects the CNFET from undesirable random fluctuations, in a similar way as in (3.15). For a target PNMV, processing parameters ultimately set a lower bound on $N$. We denote this lower bound $N_{\text{min}}$. For CNFET circuits to be practical on a billion-gate scale, a PNMV value on the order of $10^{-10}$ is desired. Table 2 shows $N_{\text{min}}$ values for different processing condition under this constraint.

### Table 2. Guidelines for $N_{\text{min}}$.

<table>
<thead>
<tr>
<th>Ideal Etching</th>
<th>$c_m = \mu_d + 4\sigma_d$</th>
<th>$c_0 = \mu_d - \sigma_d$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$p_m=33%$</td>
<td>$c_m=21$</td>
<td>$c_0=9$</td>
</tr>
<tr>
<td>$p_m=8%$</td>
<td>$c_m=9$</td>
<td>$c_0=35$</td>
</tr>
</tbody>
</table>

* These guidelines are for a Gaussian CNT diameter distribution. For non-Gaussian diameter distributions, we can use corresponding values of $c_m$ and $c_0$ that gives the same cumulative probability.

This table delivers mixed news: the good news is that the noise margin problem can effectively be handled during design by increasing $N_{\text{min}}$; the bad news is that increased $N_{\text{min}}$ implies increased cost. That is why processing advancements such as reduction in $p_m$ can deliver significant benefits.

### 4.3. Delay Variations

As discussed in Sec. 2.3, m-CNTs result in delay variations in CNFETs by causing fluctuations in the drive current. We use Taylor expansion at the point $I_{\text{drive}} = \mu(I_{\text{drive}})$ to Eqn. (2.2). The standard deviation of delay can then be approximated by the 1$st$ order term of Taylor expansion as (we will show that this is a good fit with SPICE simulation results):

$$\sigma(\text{delay}) = \frac{C_{\text{load}} V_{dd}^2}{\mu(I_{\text{drive}})^2} \sigma(I_{\text{drive}}) = \frac{\mu(\text{delay})}{\mu(I_{\text{drive}})} \sigma(I_{\text{drive}})$$

(4.6)

For practical leakage power and noise margin requirements discussed in Sec. 4.1 and 4.2, most m-CNTs will be removed by etching. So it is reasonable to neglect the $(I_{\text{m,pullup}} - I_{\text{m,pulldown}})$ term in (2.3). We further approximate the drive current $(I_{\text{s,pullup}})$ in (2.3) by the saturation current $I_{\text{s,son}}$. Thus, $I_{\text{drive}} = I_{\text{s,pullup}} = I_{\text{s,son}}$ (4.7)

Then for an inverter with CNFET with $N$ CNTs, (4.6) can be simplified to

$$\frac{\sigma(\text{delay})}{\mu(\text{delay})} = \frac{\sigma_s(I_{\text{s,son}})}{\mu_s(I_{\text{s,son}})}$$

(4.8)

where $\mu_s(I_{\text{s,son}})$ and $\sigma_s(I_{\text{s,son}})$ can be calculated from (3.14) and (3.15) by assuming m-CNT currents to be zero, which gives

$$\frac{\sigma(\text{delay})}{\mu(\text{delay})} = \frac{\sigma_s(I_{\text{s,son}})}{\mu_s(I_{\text{s,son}})} = \frac{(\sigma^2 + p_m \mu^2)}{\mu^2}$$

(4.9)

where $\mu_s = \mu(I_{\text{s,son}})$ and $\sigma_s = \sigma(I_{\text{s,son}})$ are current mean and standard deviation for single s-CNT and can be derived from (3.8) and (3.10).

Figure 4.3a compares (4.9) with Monte Carlo simulation results with $N = 30$. Because (4.9) neglects the m-CNT current terms as discussed above, its result becomes independent of $c_m$. This is certainly not true as compared by the two simulation results with $c_m = \mu_d + \sigma_d$ and $\mu_d + 4\sigma_d$ in the figure; however, the difference among the two simulation curves and the curve estimated by (4.9) are within 17%, which shows that $c_m$ has a minimal impact on delay variations. Figure 4.3a also shows that delay variations rises stably with increasing $p_m$.

Figure 4.3b plots the results in (4.9) with $c_s$ as the x-axis. It is shown that delay variation changes slowly with $c_s$ when it is less than $\mu_d - \sigma_d$; after this point, the percentage change of $\sigma(\text{delay})/\mu(\text{delay})$ becomes very significant, corresponding to a much higher removal-percentage increase for s-CNTs (not shown in the figure).

**Guideline:** $c_s < \mu_d - \sigma_d$ (Gaussian)

Four different $N$ values are also shown in Figure 4.3b. Because a $1/\sqrt{N}$ relation is predicted by (4.9), delay variation is more significant when $N$ is small. Therefore, delay variation requirements can also impose constraints on $N_{\text{min}}$, although this constraint is usually not the limiting factor compared to the one discussed in Sec.4.2. For example, even if ideal etching is assumed, the requirement on $N_{\text{min}}$ by PNMV ($10^{-10}$) is 21 according to Table 2, while the impact of $N$ on delay variation is already very small when $N > 20$ as shown in Fig. 4.3b. However, if $p_m$ is significantly improved (e.g. 8% as shown in Table 2), delay variations can become significant.

### Conclusion

There is no known technique available today to grow 100% s-CNTs. Therefore, m-CNT removal techniques such as selective chemical etching are necessary. Unfortunately, such removal techniques are imperfect. Hence, co-optimization of CNT removal and circuit design is necessary for enabling robust digital logic using CNFETs. This paper answers two most important questions regarding this co-optimization:

**Question 1 (Processing Question):** What $p_m$, $c_m$ and $c_s$ values must be satisfied for CNFET circuits with practical constraints on leakage, noise margin and delay variation?

**Answer:** Under the assumptions explained in this paper, our guideline is to achieve $c_m = \mu_d + 4\sigma_d$ and $c_s < \mu_d - \sigma_d$. 
Question 2 (Design question): Determine $N_{\text{min}}$, the minimum number of CNTs per CNFET prior to etching, such that the aforementioned constraints are satisfied.

Answer: With the above guidelines on $c_m$ and $c_s$, our recommendation is to use $N_{\text{min}} = 62$ for $p_m = 1/3$. Significant reduction of $p_m$ can improve overall circuit performance (area, speed, power) by reducing $N_{\text{min}}$.

Future work includes fabrication of CNFET circuits with selective chemical etching, with help from chemists, for experimental validation of the assumptions made (including CNT diameter distribution and spatial distribution of m-CNTs and s-CNTs) and guidelines presented in this paper.

Acknowledgment

This research was supported in part by the FCRP Gigascale Systems Research Center (GSRSC) and the National Science Foundation. J. Zhang and N. Patil are supported by Stanford Graduate Fellowships.

References


Appendix

We solve the PNMV for an inverter from processing and design parameters in this section. For simplification, we neglect the effect of s-CNT diameter on its current, so that $I_s(x) = I_p = \text{constant}$. Simulations show that this simplification has negligible impact on PNMV.

When both m-CNT and s-CNT currents are independent of CNT diameters, the noise margin is only determined by the numbers of both types of CNTs. If $SNM_s$ is the required noise margin, then the following test function can be calculated using a proper device model:

$$T(N_s, N_m, SNM_R) = \begin{cases} 0, & \text{if } SNM(N_s, N_m) \geq SNM_R \\ 1, & \text{if } SNM(N_s, N_m) \leq SNM_R \end{cases} \quad (A.1)$$

where $N_m$ is the number of m-CNTs, $N_s$ is the number of s-CNTs, and $SNM(N_s, N_m)$ is the static noise margin of an inverter with $N_s$ s-CNTs and $N_m$ m-CNTs.

Because only the number of CNTs matters, the etching processes can be further simplified as Bernoulli trials - there is probability $p_{es}$ ($p_{em}$) that an s-CNT (m-CNT) is removed, and probability $1-p_{es}$ ($1-p_{em}$) that it remains intact. The following equations determine $p_{es}$ and $p_{em}$:

$$p_{es} = \int_0^{q_{es}} f_{es}(x)dx, \quad p_{em} = \int_0^{q_{em}} f_{em}(x)dx \quad (A.2)$$

For a CNFET with $N$ CNTs, the number of s-CNTs (m-CNTs) prior to etching, $N_s$ ($N_m$), follows a binomial distribution:

$$N_s \sim B(N, p_s), \quad N_m \sim B(N, p_m) \quad (A.3)$$

With the definition of $p_{es}$ ($p_{em}$) in (A.2), we can also model the number of s-CNTs (m-CNTs) after etching, $N_s$ ($N_m$), with binomial distribution:

$$N_s \sim B(N, q_{es}), \quad N_m \sim B(N, q_{em}) \quad (A.4)$$

Therefore, the probability of a CNFET with $N$ CNTs to have $N_s$ s-CNTs and $N_m$ m-CNTs after etching is given by

$$P_N(N_s, N_m) = \sum_{N_{es} = 0}^{N_s} \sum_{N_{es} = 0}^{N_m} \binom{N}{N_s} \binom{N-N_s}{N_{es}} \binom{N_m-1}{N_{es}} p_{es}^{N_{es}} q_{es}^{N_{es}} p_{em}^{N_m-1-N_{es}} q_{em}^{N_m-N_{es}} \quad (A.5)$$

PNMV can be derived by combining (A.1) and (A.5):

$$PNMV = \sum_{N_s=0}^{N_s} \sum_{N_m=0}^{N_m} T(N_s, N_m, SNM_R) \cdot P_N(N_s, N_m) \quad (A.6)$$