Calibration of Integrated CMOS Hall Sensors Using Coil-on-Chip in ATE Environment

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Abstract
Due to high demand for hall sensors mostly in the automotive and industrial applications, development and manufacturing of hall sensors in System-on-Chip (SoC) became more important. On the other hand, options for test and characterization of hall sensors in manufacturing environment are very limited. In most cases external field generators are used in order to characterize the hall sensors on a small set of production samples. In this paper, we present our Coil-on-Chip (CoC) calibration methodology where there is no need for a dedicated setup/assembly. Our methodology is also immune to self-heating. Our methodology enables reduced costs in test equipment, 100% screening of hall sensors in manufacturing tests, and reliable trimming of sensitivity spread over temperature from -40°C to 150°C. Measurement results before trimming show less than 20% six-sigma spread for normalized sensitivity across 120 samples of different hall sensor structures processed in a 0.35 µm high-voltage CMOS process.

1. Introduction
Magnetic field sensors offer numerous applications such as measuring currents without any contact, proximity sensing, compass applications, and measuring displacement.

A hall sensor is a transducer that varies its output voltage in response to changes in magnetic field. Today hall sensor and readout electronics could be integrated on the same chip using a CMOS process [1]. This makes them very cost-effective. On the other hand, CMOS process still has severe limitations for a performant hall sensor. These are, but not limited to, sensitivity variation with time and temperature, low sensitivity, and high offset voltage, which could be an order of magnitude larger than the output voltage [2].

Options for testing and characterization of hall sensors in volume production are very limited. Most frequent used technique is the utilization of external field generators to characterize the hall sensors on a small set of production samples [3]. One possible solution is the integration of a coil on the contractor of the handler. The coil in the contractor requires a current in the range of 30 A to 60 A to generate a magnetic field of 100 mT. The current must be switched on and off during each program run and may generate huge power peaks, therefore resulting in long settling times. This would not make it a viable solution for reduced test times in the manufacturing environment. In [4], the authors present a solution that uses an excitation coil manufactured by direct bonding onto the chip surface. This process might have difficulties in mechanical alignment of the magnetic field perpendicular to the surface of the sensor. Due to these limitations, sensitivity calibration is mostly done at the application level by providing several knobs in the silicon [5]. However, an early screening without a need for the application setup and wide-range trimming will reduce the setup costs.

Utilizing the coil directly on the chip is a low-cost alternative to the above mentioned techniques. It does not require a special test setup and assembly. No mechanical alignment difficulties could be seen as the coil and the hall sensor have comparable form factors and the same plane. Therefore, Coil-on-Chip (CoC) becomes a potential low-cost solution while not losing the accuracy. In [6], (de)modulation techniques are presented to differentiate the low-amplitude reference magnetic field generated by CoC from the external magnetic field where gain is dynamically calibrated.

Besides all advantages, CoC has a major drawback of self-heating when high-amplitude coil currents are applied in order to achieve high signal-to-noise ratio requirements. High amplitude in the coil current heats the coil and consequently the hall sensor as a result of heat transfer through the substrate. This affects the accuracy of tests. In this paper, we address this issue and propose a solution where we are able to calibrate the sensitivities with high precision in ATE under the presence of self-heating and of high residual offsets. We demonstrate our results by measurements of hall sensors in manufacturing environment.

The paper is organized as follows. In section 2 we describe the mechanisms of self-heating. In section 3 we describe our calibration methodology. In section 4 we present the reliability aspects of CoC integration. In
section 5 we present the experimental setup and results performed on more than 100 samples using an ATE program in production environment. In section 6 we draw conclusions.

2. Self-heating in hall sensor with CoC

In order to generate magnetic fields in the range of 2-5 mT, it is necessary to apply a coil current with amplitudes in the range of a few tens of mA. Such high-amplitudes in the coil current heat the coil and then the hall sensor due to heat transfer through the substrate. This generates local temperature differences across the hall sensor. In fact, a 1% mismatch in the sheet resistances of the left and right sides of the plane where the hall-bias current \( I_{\text{hall}} \) flows generates around 30 mV offset at the output in a 3 V process. On the other hand, the output due to the hall effect itself is just in the range of a few 100 µV’s. Since this offset is not stationary, it will be difficult to cancel using any spinning technique [7]. Therefore, it is important to cancel the impact of self-heating.

Following mechanisms are observed in the transients of the output voltage as a result of self-heating caused by the bias current of coil (see Figure 1):

- **Electrical ringing:** This is caused by the bottom-plate capacitance of the hall sensor and the inductance of the coil. This transient happens within micro-seconds range. However, with larger loads on the hall sensor output, this might increase to mili-seconds range.

- **Hot spot:** This is caused by the heating caused by the amplitude of the coil current. There occurs a large shift in the offset voltage within micro-seconds range.

- **Drift with temperature:** This is caused by the thermal energy transfer from the coil and by the non-uniform settling of temperature gradients across the hall sensor. This effect is orders of magnitude slower than the impact observed in hot spot.

- **Cooling:** This is caused by the release of coil bias. A similar sequence of events is observed as in heating, first a sudden jump of the offset voltage to the initial state before the coil current is applied. This is followed by a slow change of the offset by temperature drift.

Using measurements we demonstrate the impact of self-heating on the output. The device under test is a hall sensor implemented in a 0.35 µm CMOS process technology. It has the geometry of cross structure with an edge of 45 µm and has the n-type EPI material where hall effect occurs. The plate is surrounded with a coil that has a diameter of 73 µm and has 5 turns of 2 parallel metal tracks with a width of 2 µm. Figure 2 shows the measured transients of the coil current and the corresponding Hall-plate output voltages obtained from two samples implemented in TQFP48 package. The results clearly show that the offset levels differ from sample to sample. Also the amount of offset shift (mid-point between the maximum and the minimum of the output) due to self-heating differs as well. This large shift in offset is caused by the hot-spot mechanism.

![Figure 1: Impact of coil self-heating on the output of the Hall-sensor.](image)

On the other hand, the peak-to-peak value of the hall sensor voltage still stays comparable where this shows that the magnetic-field sensitivities from sample to sample stay comparable. In fact, the peak value \( (V_{\text{hallmax}}-V_{\text{hallmin}})/2 \) gives the Hall voltage that is induced by electromagnetic field generated by the coil.

![Figure 2: Measurements that illustrate the impact of hot-spot mechanism on the offset voltage shift of the same hall sensor on two samples.](image)

The output voltage also drifts with temperature formed by self-heating. Figure 3 demonstrates this. This affect is only limited to a change of less than a few µV’s over
60 ms. Therefore, we do not need to estimate temperature drift in the cycle once the duration between two measurements is kept short.

![Figure 3: Measurements that illustrate the impact of output drift with temperature.](image)

### 3. Definition of transients and calibration procedure

Using ATE we generate the transients of the coil current and perform switching of hall terminals to stimulate current spinning technique to eliminate the offset at the output [1]. The hall sensor is biased with a current source after measuring the current under maximum voltage bias. At each temperature the bias value needs to be defined since the temperature coefficient of the resistance of the hall sensor is rather high. Using a bipolar current waveform, residual offset as well as the large offset drift due to self-heating is calibrated out from the measurement. In this way, we precisely measure the sensitivity of the hall sensor.

The transient waveform of the coil current is shown in Figure 4. There might still be a small offset drift due to self-heating from H3 to H4 and from V3 to V4. In order to control this drift, we need to keep the amplitude of the coil current below 50 mA. We also have a drift from H1 to V1 where we need to allow some time between H4 and V2 (>2 ms).

![Figure 4: Transient of the coil current bias.](image)

This limitation in time is due to slow ATE equipment where in hardware switching times will be in the order of microseconds where self-heating affects could be significantly reduced with on-chip spinning circuits.

Calibration procedure is described by the following set of equations where horizontal and vertical mode switchings are based on techniques described in [1]:

\[
H3 : \text{V}_{\text{hallHF}} = S_xB_e + S_xB_c + V_{\text{offh}} (T = T_{H3})
\]

\[
H4 : \text{V}_{\text{hallHF}} = S_xB_c - S_xB_c + V_{\text{offh}} (T = T_{H4})
\]

\[
V3 : \text{V}_{\text{hallVF}} = S_xB_e + S_xB_c - V_{\text{offv}} (T = T_{V3})
\]

\[
V4 : \text{V}_{\text{hallVF}} = S_xB_c - S_xB_c - V_{\text{offv}} (T = T_{V4})
\]

\[
V_{\text{hallex}} = (V_{\text{hallHF}} + V_{\text{hallVF}} + V_{\text{hallex}} - V_{\text{hallVF}})/4 + V_{\text{hallex}}
\]

where

\[
S : \text{Sensitivity of the hall sensor}
\]

\[
B_c : \text{External magnetic field (it should be kept stable during the full period)}
\]

\[
V_{\text{off}}(T) : \text{Offset voltage at temperature T where T is set by self-heating}
\]

\[
V_{\text{hallex}} : \text{Calibrated hall sensor voltage}
\]

\[
V_{\text{hallex}} : \text{Error term, which is given by:}
\]

\[
V_{\text{hallex}} = [V_{\text{offh}} (T = T_{H3}) - V_{\text{offh}} (T = T_{H4})] +
\]

\[
V_{\text{offv}} (T = T_{V3}) - V_{\text{offv}} (T = T_{V4})]/4)
\]

In fact, equation (2) indicates that we rely on having \(T_{H3}=T_{H4}\) and \(T_{V1}=T_{V2}\) in order to get rid of impact of residual offset on the output.

The residual offset is given by the difference in offsets in horizontal and vertical spinning:

\[
V_{\text{off}} = (V_{\text{hallHF}} + V_{\text{hallVF}} - V_{\text{hallex}})/2
\]

\[
V_{\text{off}} = [V_{\text{offh}} (T = T_{H3}) + V_{\text{offh}} (T = T_{H4})]/2 -
\]

\[
[V_{\text{offv}} (T = T_{V3}) + V_{\text{offv}} (T = T_{V4})]/2
\]

In order to minimize the impact of self-heating on the output and the residual offset, we need to have \(T_{H3}=T_{H4}\) and \(T_{V1}=T_{V2}\). This could be achieved by reducing the peak value of the coil current and/or by reducing the pulselength of the positive/negative parts of the coil current, basically by minimizing the total energy delivered to the coil. The minimum pulselength that could be achieved in the current ATE setup could be 4 ms in the current setup defined by the settling time of output due to the loading of the tester.

In order to exclude the impact of self-heating we also applied the above calculations for the ATE data when the coil current bias is zero. This figure is the primary residual offset of the hall sensor since in field operation the magnetic field would be generated external where there will be no self-heating impact.

Following are limitations of the ATE setup:
Multiplexing the source and sense points to emulate the behavior of current spinning is rather slow. This elevates the self-heating problem where we need to keep the amplitude of the coil current rather small.

Horizontal and vertical switching should ideally follow each other in the positive and the negative parts of the coil current. This could not be done due to limited speed of spinning in ATE.

We characterize the hall sensor using a small range of magnetic fields. For this reason, the external magnetic field variation should be kept well below the resolution of input range during one coil cycle. For instance, if the application requires a resolution of 1%, the external magnetic field variation in the ATE setup should be limited to 1% of the magnetic field generated by CoC. Typically, we can generate magnetic fields in the order of 5 mT using CoC. Therefore, for instance for 1% resolution we require $<50 \mu T$ variation in the external magnetic field.

### 4. Reliability aspects of CoC

For reliability analysis, we use the parameters of a 4-metal 3.3V 0.35 μm CMOS process. We consider two scenarios for this analysis:

- **Scenario-1**: CoC with 50 mA peak current in 5% duty cycle during device operation where we target 1% failure in 20 years
- **Scenario-2**: CoC with 50 mA peak current in ATE where maximum allowed current should be below the peak current (50 mA/μm²) that melts the track.

Results shown in Table 1 indicate that CoC design is more constrained by the impedance of the coil to stay within the supply range rather than minimum track-width to meet the reliability requirements.

Impact of self-heating will also be reduced by reducing the coil resistance in order to have less heat dissipation in the coil resistance. There is still margin to lower the resistance of coil by making the coil tracks wider. Further increasing track width of those coils will reduce the coil resistance; however this increase in track width is limited by the number of turns that could be fit in a certain silicon area defined by the size constraints of hall sensor.

### Table 1: CoC design parameters for run-time calibration (Scenario-1) and for ATE-based calibration (Scenario-2).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Scenario-1</th>
<th>Scenario-2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature of metal [°C]</td>
<td>150</td>
<td>150</td>
</tr>
<tr>
<td>Max allowed current [mA/μm²]</td>
<td>2</td>
<td>50</td>
</tr>
<tr>
<td>Sheet resistance (M2, M3, M4) [Ω/μm]</td>
<td>72, 55, 34</td>
<td>72, 55, 34</td>
</tr>
<tr>
<td>Minimum track width</td>
<td>0.7, 0.7, 0.8</td>
<td>0.7, 0.7, 0.8</td>
</tr>
<tr>
<td>Via resistance [Ω]</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td><strong>Target hall sensor</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Coil side [μm]</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>Number of turns per metal layer [N] – $N_{turn} = 3xN$</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Magnetic field [mT]</td>
<td>8.49</td>
<td>8.49</td>
</tr>
<tr>
<td><strong>Reliability constraints</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum number of vias between each pair of metals</td>
<td>10</td>
<td>1</td>
</tr>
<tr>
<td>Minimum track width (M2, M3, M4) [μm]</td>
<td>3.4, 3.4, 2.2</td>
<td>0.7, 0.7, 0.8</td>
</tr>
<tr>
<td>$R_{coil}$ [Ω]</td>
<td>300</td>
<td>1191</td>
</tr>
<tr>
<td><strong>Supply range constraints</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum number of vias between each pair of metals</td>
<td>18</td>
<td>18</td>
</tr>
<tr>
<td>Minimum track width (M2, M3, M4) [μm]</td>
<td>14, 14, 16</td>
<td>14, 14, 16</td>
</tr>
<tr>
<td>$R_{coil}$ [Ω]</td>
<td>59</td>
<td>59</td>
</tr>
</tbody>
</table>

* 1% failure in 20 years

### 5. Experimental results

We processed several test structures with CoC in state-of-the-art 0.35μm CMOS process optimized for high-voltage automotive and industrial applications. Fully automated measurements were performed using an automatic test equipment (ATE) program in production environment.

Each hall sensor is surrounded with CoC (see Figure 5) where each terminal of hall sensor is fully accessible by the ATE equipment. Table 2 lists the features of some of those test structures. Acronym SH stands for the standard-shaped hall sensor while CR stands for the cross-shaped hall sensor. NEP stands for N-type epitaxial (NEPI) layer while NEP stands for NEPI pinched with PPLUS implant. NEP plate is expected to have improved current sensitivity (with respect to NE plate). This might be at the expense of reduced offset stability over temperature. The layout of the test chip is shown in Figure 6. SH_NE50 is placed at another test chip. Both test chips were packaged in LQFP64 package.

Descriptions of parameters are given in Table 3. Table 4 lists the values of those parameters obtained from ATE data for the test structures: SH_NE50, CR_NEP45, SH_NE25. The results show that the normalized sensitivity of CR_NEP45 is the highest.
Figure 5: Hall sensor with CoC.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{coil_{max}}$</td>
<td>Maximum amplitude of the coil current</td>
</tr>
<tr>
<td>$R_{coil_{max}}$</td>
<td>Resistance of the coil when $I_{coil}=I_{coil_{max}}$</td>
</tr>
<tr>
<td>$i_{hall}$</td>
<td>Current bias of the hall sensor</td>
</tr>
<tr>
<td>$R_{hall}$</td>
<td>Resistance of the hall sensor when $i_{hall}=i_{hall_{max}}$</td>
</tr>
<tr>
<td>$V_{hall_{calc}}$</td>
<td>Calibrated hall sensor output when $i_{hall}=i_{hall_{max}}$</td>
</tr>
<tr>
<td>$V_{hall_{off}}$</td>
<td>Static offset when $I_{coil}=0$</td>
</tr>
<tr>
<td>$DNL$ [LSB]</td>
<td>DNL when the coil current is swept from 0 to $I_{coil_{max}}$ in 32 steps</td>
</tr>
<tr>
<td>$INL$ [LSB]</td>
<td>INL when the coil current is swept from 0 to $I_{coil_{max}}$ in 32 steps</td>
</tr>
<tr>
<td>$SC_{norm}$</td>
<td>Normalized current-related sensitivity of the hall sensor ($V_{hall_{calc}}/I_{coil_{max}}/i_{hall}$)</td>
</tr>
<tr>
<td>$TC-SC_{norm}$</td>
<td>First-order temperature coefficient of $SC_{norm}$</td>
</tr>
<tr>
<td>$B_{eff}$</td>
<td>Magnetic field efficiency of the coil, taken from bench measurements and/or hand-calculations</td>
</tr>
</tbody>
</table>

Table 2: Description of measured parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>SH_NE50</th>
<th>CR_NEP45</th>
<th>SH_NE25</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of turns</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Side dimension [um]</td>
<td>113</td>
<td>73</td>
<td>65</td>
</tr>
<tr>
<td>Magnetic field efficiency of the coil [mT/A]</td>
<td>50.1</td>
<td>77.5</td>
<td>87.0</td>
</tr>
</tbody>
</table>

Table 2: CoC parameters of 0.35 µm CMOS test structures used in ATE.

Statistics of parameters given in Table 4 are listed in Table 5. Each cell indicates two values (ML, SL) for percentage spread of a parameter at room temperature (25°C) over 120 samples. The percentage ML indicates an average value for the one-sided spread:

$$ML = 100 \times (Max - Min)/(2 \cdot Mean)$$  \hspace{1cm} (4)

where the range is given by (1±ML/100)*Mean.

The percentage SL indicates a one-sided spread for a six-sigma process that allows a mean deviation of 1.5σ:

$$SL = 4.5 \cdot \sigma / Mean$$  \hspace{1cm} (5)

where the range is given by (1±SL/100)*Mean. In fact, a six-sigma process that is normally distributed will have 3.4 defect parts per million beyond a point that is 4.5 standard deviations above or below the mean.

The results show that six-sigma (±4.5*σ) spread of normalized sensitivity ($SC_{norm}$) is minimum in SH_NE25 while it is maximum in CR_NEP45. Spread on sensitivity from sample-to-sample is limited to 20% although spread on static offset is quite high. The latter could be removed by current spinning [1]. This variation in sensitivities could easily be tuned by trimming the amplitude of the hall bias current.

Our calibration procedure enables 100% screening and
trimming of hall sensors without a need for end-of-line/application calibration. After this trimming, it is still possible to perform dynamic calibration schemes as proposed in [6] using CoC for instance in order to overcome aging impact on sensitivity.

### 6. Conclusions

In this paper we presented Coil-on-Chip (CoC) results that were obtained from ATE in production environment. Results indicate that we can calibrate the sensitivities with high precision over temperature range from -40°C to 150°C under the presence of self-heating as well as high residual offsets. Measurement results before trimming show less than 20% six-sigma Gaussian spread for normalized sensitivity across 120 samples of different hall sensor types.

Our methodology is a low-cost solution since trimming of sensitivity does not require a special test equipment and assembly.

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### 7. References


