A Novel Technique for Improving Temperature Independency of Ring-ADC

Shun Li, Hua Chen, Feng Zhou
ASCI & System State-Key Lab, Fudan University, Shanghai 201203, China
fengzhou@fudan.edu.cn

Abstract

A new temperature compensation technique for ring-oscillator-based ADC is proposed in this paper. It employs a novel fixed-number-based algorithm and a CTAT current biasing technology to compensate the temperature-dependent variations of the output, thus eliminates the need of digital calibrations. Simulation results prove that, with the proposed technique, the resolution under the temperature range of 0℃ to 100℃ can reach a 2-mV quantization bin size with an input voltage span of 120mV, at the sampling frequency f_s=100KHz.

1. Introduction

Windowed analog-to-digital converters (ADCs) are widely used in digital DC-DC converters due to the fact that the output voltage is regulated in the vicinity of the reference voltage. In recent years, synthesizable windowed ADCs based on delay-line [1, 2, 3] or ring-oscillator [4, 5] structures have been reported. These structures have the advantages of low-power, low-area and high-resolution so that they are very suitable for digital DC-DC applications. However, one severe problem for them is that the digital output data is temperature-dependent since the delay of the delay-cells can't be precisely controlled against the temperature variations. Digital calibrations can be accomplished in a number of ways. A simple strategy is to subtract a reference value from the converted output [1] or to obtain a correction ratio to a reference value [6]. Since the variations of the digital output due to temperature variation are not pure dc offset or gain error, these types of calibrations may be imprecise. A look-up table can improve the precision. However, it will take a large chip area. Besides, an additional ADC is necessary to convert the measured analog temperature value into a digital one, which will further increase the circuit's complexity and the power consumption.

In this paper, we propose a novel temperature compensation technique for ring-oscillator-based ADCs. We put forward a fixed-number-based algorithm and a Complementary-to-Absolute-Temperature (CTAT) current biasing scheme. With our technique, a ring-ADC can achieve dramatic temperature independency without the complex digital calibrations.

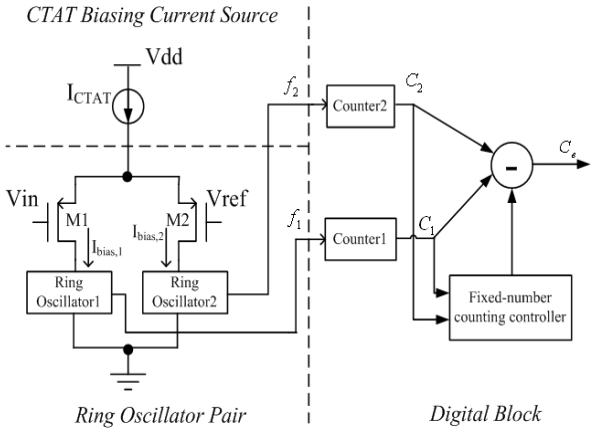

Figure 1. Ring-ADC using the proposed temperature compensation technique.

The proposed ring-ADC has been simulated with a typical 0.35μm CMOS mixed signal process (Charted). For comparison, a traditional ring-ADC that employs a normal fixed-time-based algorithm [5] and conventional biasing current source is also simulated. Results reveal that, with the temperature range of 0℃ to 100℃, the input voltage span of 120mV and the sampling frequency of 100KHz, the proposed ring-ADC can reach a 2-mV quantization bin size while the traditional ring-ADC only 16-mV.

2. System Architecture

The principle of the proposed temperature compensation technique is explained with a ring-ADC system shown in Figure1. It consists of a CTAT biasing current source, a ring oscillator pair and a synthesizable digital block.

The CTAT biasing current source is used to generate a temperature compensated current for the two ring-oscillators. The error voltage between V_{in} and V_{ref}, V_e, brings on error current between two branches, $I_{bias,1}$-$I_{bias,2}$, thus different frequencies at the two ring-oscillators are generated. The two frequencies are captured by two counters, then our fixed-number-based algorithm is applied to derive the temperature- independent output.

978-3-9810801-3-1/DATE08 © 2008 EDAA

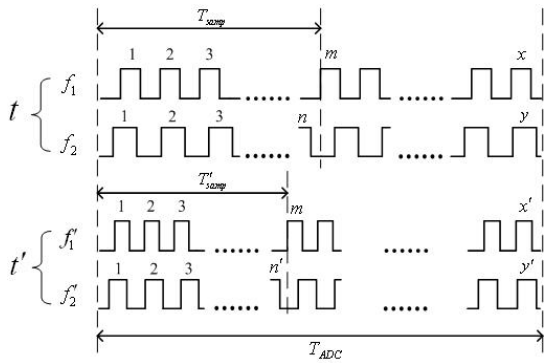

Figure 2. C_e under different temperature.

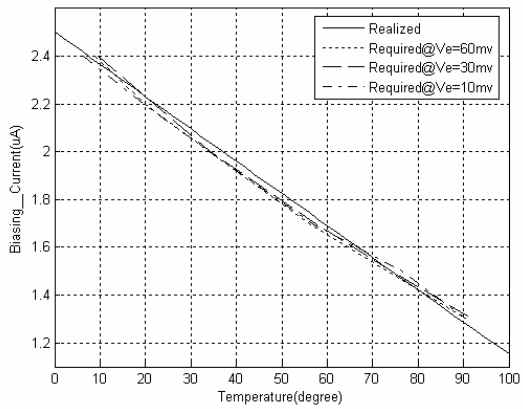

Figure 3. The required and realized I_{CTAT}.

3. Fixed-Number-Based Algorithm

The right part of Figure1 can also be used to explain the fixed-time algorithm [5] if we replace the module fixed-number counting controller with a fixed-time one. The counters are reset at the beginning of each sampling cycle and stopped after a fixed period of time. Then one counter's output is subtracted from the other. The result, C_e, is given by [5]:

$$C_e = T_{ADC} K_f \left(I_{bias,1} - I_{bias,2} \right) \tag{1}$$

where T_{ADC} is the ADC sampling period, K_f is the constant characterizing the ring oscillator frequency sensitivity to its biasing current. $I_{bias,1}$ and $I_{bias,2}$ are the biasing currents of the two branches. The digitized error voltage can be calculated by scaling C_e. Actually, the error frequency,

$$f_e = f_1 - f_2 = K_f \left(I_{bias,1} - I_{bias,2} \right) \propto V_e \tag{2}$$

where V_e is the error input voltage. Then,

$$C_e = T_{ADC} \left(f_1 - f_2 \right) = T_{ADC} f_e \tag{3}$$

When temperature migrates from t to t', assume $I_{bias,1}$, $I_{bias,2}$, f_1, f_2 change to $I_{bias,1}'$, $I_{bias,2}'$, f_1', f_2', respectively. The following discussion will show that in our solution, the CTAT current biasing will make $I_{bias,1}/I_{bias,2}$ independent of the temperature. That is to say, when temperature migrates from t to t', $I_{bias,1}'/I_{bias,2}'=I_{bias,1}/I_{bias,2}$, and consequently $f_1'/f_2'= f_1/f_2$.

Then, according to Figure2, we have:

$$C_e \Big|_{t,fixed-time} = x - y = T_{ADC} \left(f_1 - f_2 \right) = T_{ADC} f_e \tag{4}$$

$$C_e \Big|_{t',fixed-time} = x' - y' = T_{ADC} \left(f_1' - f_2' \right) = T_{ADC} \frac{f_1'}{f_1} \left(f_1 - f_2 \right) \tag{5}$$

Obviously, C_e changes with the temperature. It means that, with the fixed-time-based algorithm, C_e varies with the temperature and can't reflect V_e correctly.

In the proposed fixed-number-based algorithm, the counters are also reset at the beginning of each sampling cycle but stopped when the first counter's output reaches a fixed-number, say, m, in Figure2. Then, (4) and (5) can be rewritten as:

$$C_e \Big|_{t,fixed-number} = m - n = T_{samp} \left(f_1 - f_2 \right) = T_{samp} f_e \tag{6}$$

where

$$T_{samp} = \frac{m}{f_1} \tag{7}$$

$$C_e \Big|_{t',fixed-nuber} = m - n' = T'_{samp} \left(f_1' - f_2' \right) = T'_{samp} \frac{f_1'}{f_1} \left(f_1 - f_2 \right) \tag{8}$$

where

$$T'_{samp} = \frac{m}{f_1'} = \frac{T_{samp} f_1}{f_1'} \tag{9}$$

Substituting (9) into (8), we get:

$$C_e \Big|_{t',fixed-nuber} = T_{samp} \left(f_1 - f_2 \right) = T_{samp} f_e = C_e \Big|_{t,fixed-number} \tag{10}$$

Thus, a temperature-independent C_e can be obtained.

Conclusion 1 *With the Fixed-Number-Based algorithm, the output of the frequency-ADC will be temperature-independent if the ratio of the currents of the two branches keeps a constant all over the considered temperature range.*

Lemma 1 *With the Fixed-Number-Based algorithm, for different input voltages, the currents ratios may be different. It doesn't matter as long as the ratio is temperature-independent for a given input voltage. Further more, we don't need to know the value of the ratio.*

4. Requirements for I_{CTAT}

The above conduction is based on the assumption that when the temperature migrates from t to t', $I_{bias,1}/I_{bias,2}$ keeps unchanged, as is not the case without our CTAT current biasing technique. Given a circuit of a ring oscillator, for example, the left part of Figure1, and an input (V_{in}-V_{ref}), we can always derive a relationship between the current of the two branches:

$$I_{bias,2} = A I_{bias,1} \tag{11}$$

Generally A is the function of both the input (V_{in}-V_{ref}) and the temperature. We found that we can properly design the biasing current, say, to be a CTAT, to guarantee that A is independent of the temperature, but may still be the function of the input. Starting from the assumption that A is only the function of the input, we inversely conduct the

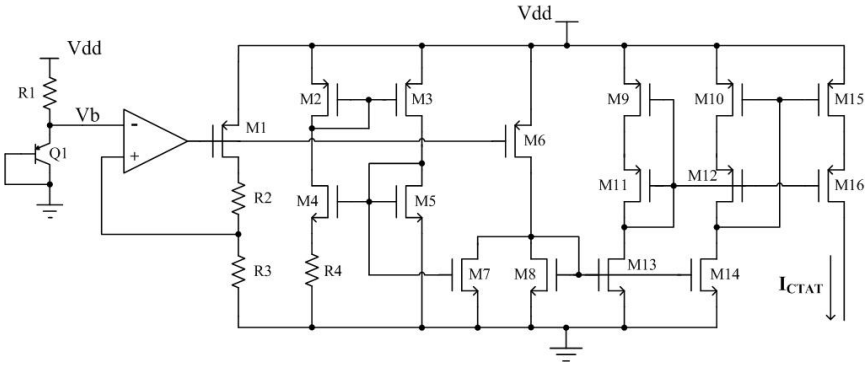

Figure 4. Schematic of the CTAT biasing current source.

requirements for the biasing current, I_{CTAT}. From Figure1, we obtain [7]:

$$\left(V_{in}-V_{ref}\right)^2=\frac{2}{\mu_p C_{ox}\left(W/L\right)_{M1,2}}\left(I_{CTAT}-2\sqrt{I_{bias,1}I_{bias,2}}\right) \quad (12)$$

By substituting (11) into (12) and using $I_{bias,1}+I_{bias,2}=I_{CTAT}$, I_{CTAT} should be:

$$I_{CTAT}=\frac{1}{2}\frac{\left(1+A\right)\left(V_{in}-V_{ref}\right)^2}{\left(1-\sqrt{A}\right)^2}\mu_p C_{ox}\left(W/L\right)_{M1,2} \quad (13)$$

where μ_p and C_{OX} are temperature-dependent parameters. Their temperature dependencies are given by [8]:

$$\mu_p=\mu_{p0}\left(\frac{T}{T_0}\right)^{-l},C_{ox}=C_{ox0}\left[1+\alpha_{C_{ox}}\left(T-T_0\right)\right] \quad (14)$$

where l is a positive constant ($l\approx2$), α_{Cox} is negative. Thus expression (13) can be simplified as:

$$I_{CTAT}\approx I_{CTAT0}\left[1-B\left(T-T_0\right)\right] \quad (15)$$

where

$$I_{CTAT0}=\frac{1}{2}\frac{\left(1+A\right)\left(V_{in}-V_{ref}\right)^2}{\left(1-\sqrt{A}\right)^2}\mu_{p_0}C_{ox_0}\left(W/L\right)_{M1,2} \quad (16)$$

$$B=l/T_0-\alpha_{C_{ox}}>0$$

The above conductions can be inversely applied. That means, if we set the biasing current as equation (15), then A has to be temperature-independent. Notice that here we needn't know exactly what value A is (Please refer to Conclusion 1 and Lemma 1). So equation (15) is just what we expect. In reality, the best I_{CTAT}s for different input voltages are not completely the same, however, they are almost coincided, as shown in Figure3.

Obviously, the slope of I_{CTAT} with respect to temperature should be negative, and can be supplied by V_{BE} of a BJT.

5. Generation of I_{CTAT}

A CTAT biasing current source shown in Figure4 realizes the I_{CTAT}. We can get:

$$I_{M6}=\frac{S_6}{S_1}\frac{V_b}{R_3},I_{M7}=\frac{S_7}{S_5}\frac{2}{\mu_n C_{ox}R_4^{\,2}}\left(\frac{1}{\sqrt{S_5}}-\frac{1}{\sqrt{S_4}}\right)^2 \quad (17)$$

where $S_i=\left(W/L\right)_i, i=1,2,3...$ (18)

As we know,

$$V_b=V_{BE}=V_{BE0}\left[1+\alpha_{V_{BE}}\left(T-T_0\right)\right]$$
$$R_i=R_{i_0}\left[1+\alpha_R\left(T-T_0\right)\right],i=1\sim4 \quad (19)$$

where the expression of V_{BE} is obtained through the first-order approximation of Taylor series expansion. Then, expression (17) can be rewritten as:

$$I_{Mi}=I_{Mi_0}\left[1+tc_{I_{Mi}}\left(T-T_0\right)\right],i=6,7 \quad (20)$$

where

$$I_{M6_0}=\frac{S_6}{S_1}\frac{V_{BE0}}{R_{3_0}},I_{M7_0}=\frac{S_7}{S_5}\frac{2}{\mu_{n0}C_{ox0}R_{4_0}^{\,2}}\left(\frac{1}{\sqrt{S_5}}-\frac{1}{\sqrt{S_4}}\right)^2 \quad (21)$$

$$tc_{I_{M6}}=\alpha_{V_{BE}}-\alpha_R,tc_{I_{M7}}=l/T_0-\alpha_{C_{ox}}-2\alpha_R$$

Thus:

$$I_{M8}=I_{M6}-I_{M7}$$
$$=\left(I_{M6_0}-I_{M7_0}\right)\left[1+\frac{I_{M6_0}tc_{I_{M6}}-I_{M7_0}tc_{I_{M7}}}{I_{M6_0}-I_{M7_0}}\left(T-T_0\right)\right] \quad (22)$$

Since $\alpha_{V_{BE}}<0$, $\alpha_{C_{ox}}<0$ and $\alpha_R>0$ ($\alpha_R=5.79\times10^{-4}$/℃, using n^+ poly resistor under charted 0.35μm CMOS mixed signal technology), $tc_{I_{M6}}$ is negative and $tc_{I_{M7}}$ positive.

Thus I_{M8} has a negative temperature coefficient ($I_{M7_0}<I_{M6_0}$), which can be tuned by the size of *M4, M5, M7* and *R4*. Finally, the required I_{CTAT} can be achieved by a current mirror:

$$I_{CTAT}=\frac{S_{15}}{S_{10}}\frac{S_{14}}{S_8}I_{M8} \quad (23)$$

The realized I_{CTAT} curve, obtained using the structure shown in Figure4, is also plotted in Figure3. It reveals that the CTAT biasing current source does provide an excellent fit to the required I_{CTAT} for whole temperature range.

6. Simulation Results

A ring-ADC using the proposed fixed-number-based algorithm together with the CTAT current biasing technique is simulated through mentor ADMS simulator, under charted 0.35μm CMOS mixed signal technology.

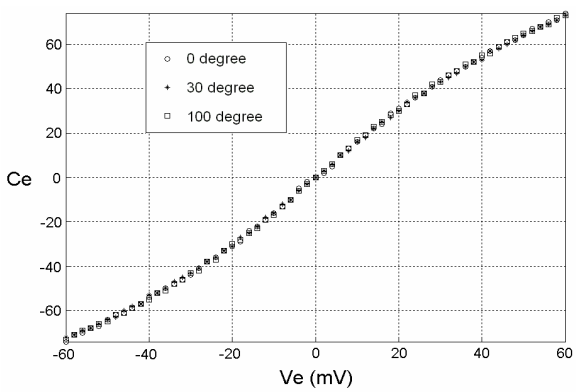

Figure 5. C_e vs V_e under different temperature using the proposed technique.

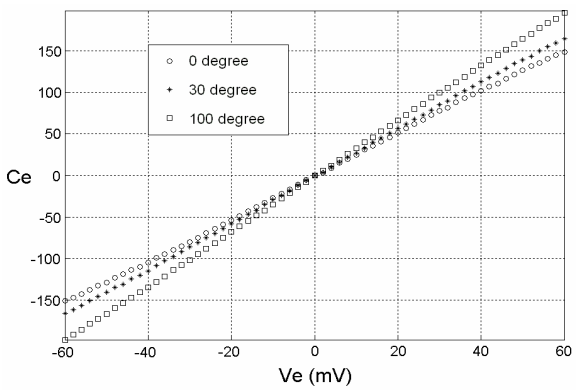

Figure 6. C_e vs V_e under different temperature using fixed-time-based algorithm and conventional biasing current source.

The fixed-number is assigned to 128 and the sampling rate is set to 10μs. Meanwhile, a traditional ring-ADC, which employs a fixed-time-based algorithm and a conventional biasing current source, is also simulated for comparison, with its fixed time set to 10μs. Both two ring-ADCs are simulated under three temperatures, 0℃, 30℃ and 100℃, respectively. Results are plotted in Figure5 and Figure6, with their Y-axis representing C_e. Obviously, the former reveals a great stability of the digital output C_e under different temperatures, while the latter shows severe variations, especially at large input voltage error. The proposed technique does provide an excellent temperature-independent characteristic for ring-ADCs.

If considered under a certain temperature, our temperature compensation technique leads to a decreased output linearity, as shown in Figure5, however, if considered within the temperature range of 0℃ to 100℃, our technique achieves much better output linearity than the traditional one, resulting a much higher converted resolution. Simulation results reveal that our ring-ADC can reach a 2-mV quantization bin size while the traditional ring-ADC only 16-mV [5]. A typical high-performance digital DC-DC chip, *ISL6592* [9] requires the quantization bin size of 3.125-mV.

Tab.1 provides a summary of the comparisons. It should be emphasized that all the results are obtained across the temperature range of 0℃ to 100℃. By applying the proposed technique, ring-ADCs do not need any additional digital calibration to compensate the temperature variation.

Tab.1: Summary of ring-ADC Characteristics. (Across a temperature range of 0℃ to 100℃)

Parameters	**with temperature compensation**	**without temperature compensation**
Technology	Charted 0.35μm CMOS mixed signal technology	
Sampling frequency	f_S= 100KHz	
Input voltage span	120mV	
Resolution	2mV/LSB	16mV/LSB
Number of bits	6 bits	3 bits

References

[1] B. J. Patella, A. Prodic, A. Zirger, and D. Maksimovic, "High-frequency digital PWM contoller IC for DC-DC converters", *IEEE Transactions on Power Electronics*, Jan. 2003, vol. 18, pp. 438-446.

[2] G. Y. Wei, J. Kim, D. Liu, S. Sidiropoulos, and M. Horowitz, "A variable-frequency parallel I/O interface with adaptive power-supply regulation", *IEEE Journal of Solid-State Circuits*, Nov. 2000, vol. 35, pp. 1600-1610.

[3] W. Takamoto, M. Tamotsu, and M. Yasuaki, "An all-digital analog-to-digital converter with 12-μV/LSB using moving-average filtering", *IEEE Journal of Solid-State Circuits*, Jan. 2003, vol. 38, pp. 120-125.

[4] J. M. Guo, K. Zhang, M. Kong, and W. H. Li, "A novel ADC architecture for digital voltage regulator module controllers", *Chinese Journal of Semi-conductors*, Dec. 2006, vol. 27, pp. 2112-2117.

[5] J. Xiao, A. V. Peterchev, J. Zhang, and S. R. Sanders, "A 4-uA quiescent-current dual-mode digitally controlled buck converter IC for cellular phone applications", *IEEE Journal of Solid-State Circuits*, Dec. 2004, vol. 39, pp. 2342-2348.

[6] T. Watanabe, and H. Isomura, "A time A-D converter LSI for accurate measurement of multitime-interval by digital processing", *Electronics and Communications in Japan*, Feb. 1996, vol. 79, pp. 98-108.

[7] B. Razavi, *Design of analog CMOS integrated circuits*, Mc-Graw-Hill, New York, 2001.

[8] Y. Cheng, C. Hu, *MOSFET modeling & BSIM3 user's guide*, Kluwer Academic Publishers, Boston, 1999.

[9] *ISL6592 Data Sheet*. Intersil, Jan., 2006:13