Bootstrapped Full–Swing CMOS Driver for Low Supply Voltage Operation

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Abstract

This paper reports a high speed and low power consumption direct–indirect bootstrapped full–swing CMOS inverter driver circuit (bfi–driver). The simulation results, based on $0.13\mu m$ *triple well CMOS technology, show that, when operated at* $1V$*, bfi–driver is* 94% *faster and consumes* 22% *less power compared to a counterpart direct bootstrap circuit [1].*

1. Introduction

Driving large capacitive loads limits the performance of CMOS circuits at low voltages. Use of standard high speed BiCMOS drivers in not viable in low voltage portable electronic systems. In this paper, a combined direct and indirect bootstrapped inverter driver circuit in triple well CMOS technology is proposed and analyzed. The features of *bfi–driver* is compared to a counterpart direct bootstrapped full–swing circuit. The chosen counterpart circuit of Fig. 1 is a fully CMOS re–implementation of BiCMOS driver scheme in [1] where NMOS transistors `M8` and `M9` are the replacement for the original NPN bipolar transistors.

1.1. Previous Work

Full–swing BiCMOS/BiNMOS logic circuits using bootstrapping in the pull–up section for low supply voltage down to $1V$ were proposed in [1] to outperform other driver circuits when fanout or the load capacitance is high. A bootstrapped circuit for CMOS and BiCMOS dynamic logic gates to enhance the speed performance was reported in [2]. The bootstrapping techniques proposed in [2] and [3] have been shown to give high performance at low supply voltages.

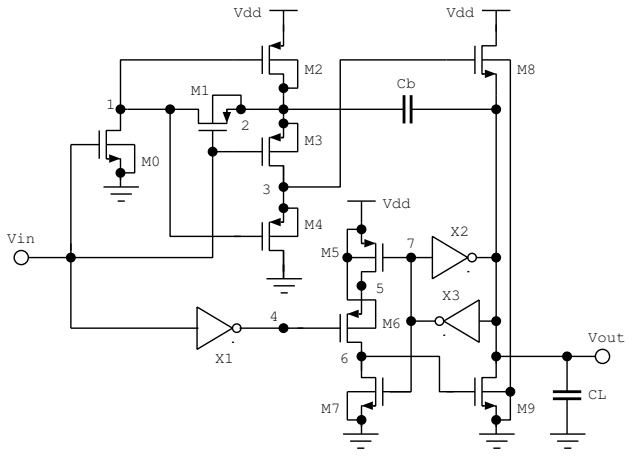

Figure 1. Circuit structure of bootstrapped CMOS in [1].

2. Driver Circuit Structure

Fig. 2 presents the circuit structure for *bfi–driver*. In this driver circuit, we use two bootstrap capacitors `Cb1` and `Cb2`, and only one inverter `X0`. `M0` and `M3` are used to charge the bootstrap capacitors `Cb1` and `Cb2`, respectively. `M1` and `M4` are the bootstrap transistors. `M2` forms the pull–down network, while `M5` forms the pull–up network. The parameters in Table 1 were used to design and simulate both driver circuits. `Cb`, `Cb1` and `Cb2` are realized using NMOS transistors `MCb`, `MCb1` and `MCb2`, respectively, of Table 1. The channel length of all transistors is $0.13\mu m$.

3. Circuit Operation

In the proposed circuit structure of Fig. 2, when `Vin` is high, the node `1` is set to low via the inverter `X0`, and `M0` is turned on. As a result, the bootstrapping capacitor `Cb1` is charged to `Vdd` (node `2` at `Vdd` and node `1` at ground po-

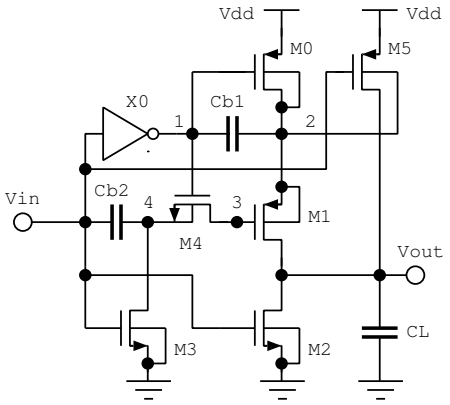

Figure 2. Schematic of the proposed bootstrapped full–swing CMOS inverter driver.

tential). M1, M4 and M5 are all turned off. M3 transistor is turned on causing Cb2 to charge (node Vin at Vdd and node 4 at ground potential). At the same time, M2 is driven by Vin and *bfi–driver* is pulled down, the output Vout is set to low. When Vin goes low, the node 1 is set to high, M0, M2, and M3 are turned off. M5 is turned on to pull–up the output. Simultaneously, M4 turns on allowing the gate of M1 to be strongly driven low due to the bootstrapping effect of Cb2. Meanwhile, the opposite bootstrapping effect of Cb1 directly couples to the output node Vout further assisting in the pull–up, and improving the switching speed.

4. Comparative Evaluation

Both driver circuits were implemented using UMC triple well $0.13\mu m$ $1.2V/3.3V$ CMOS process. Active areas for the proposed circuit and the circuit in [1] are $35.86\mu m^2$ and $44.17\mu m^2$, respectively. The circuits were simulated at $500MHz$ input frequency with $100ps$ rise and fall times, at supply voltages of $1V$ and $1.2V$, and output capacitive load in the range of 10 to $100fF$. Simulation results show that at the power supply of $1V$ our *bfi–driver* is 94% faster ($19ps$ delay at $100fF$ load), and its power consumption ($1.28mW$) is 22% lower than the driver in [1]. Fig. 3 illustrates Figures of Merit (delay power product) versus load capacitance for two drivers. As seen the Figure of Merit for *bfi–driver* is 23.6–37.5 times smaller.

5. Conclusions

This paper presented a new high performance low power direct–indirect CMOS bootstrapped driver design (*bfi–driver*). Under a condition of $1V$ voltage power supply and a capacitive loading of $100fF$, the delay and the power consumption associated with *bfi–driver* are $19ps$ and $1.28mW$, respectively.

Driver in [1]			*bfi–driver*		
Transistor(s)	Type	Width (μm)	Transistor(s)	Type	Width (μm)
PX1, PX3, M1	PMOS	0.28	PX0	PMOS	5
NX1	NMOS	5	NX0	NMOS	0.28
PX2	PMOS	15	M0	PMOS	14
NX2	NMOS	0.28	M1	PMOS	10
NX3	NMOS	0.5	M2	NMOS	19
M0, MCb	NMOS	50	M3	NMOS	0.28
M2	PMOS	1	M4	NMOS	80
M3	PMOS	2	MCb1	NMOS	60
M4	PMOS	0.28	MCb2	NMOS	100
M5	PMOS	50	—	—	—
M6	PMOS	5	—	—	—
M7	NMOS	35	—	—	—
M8	NMOS	1	—	—	—
M9	NMOS	60	—	—	—

Triple well $0.13\mu m$ $1.2V/3.3V$ process technology from UMC.

Table 1. Channel widths for driver transistors.

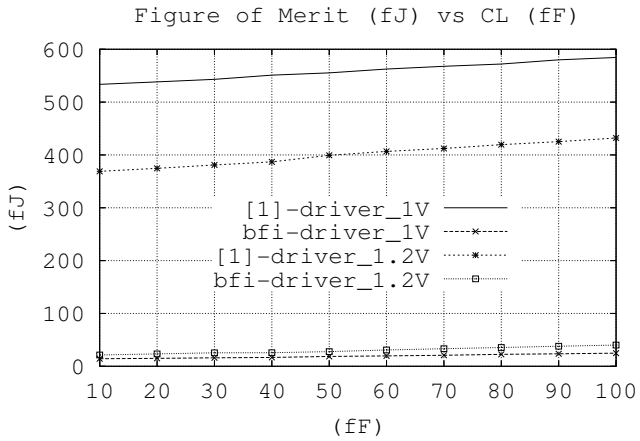

Figure 3. Delay $\times$ power versus loading.

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