Dynamic Critical Resistance: A Timing-Based Critical Resistance Model for Statistical Delay Testing of Nanometer ICs

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Abstract

As CMOS IC feature sizes shrink down to the nanometer regime, the need for more efficient test methods capable of dealing with new failure mechanisms increases. Advances in this domain require a detailed knowledge of these failure physical properties and the development of appropriated test methods. Several works have shown the relative increase of resistive defects (both opens and shorts), and that they mainly affect circuit timing rather than impacting its static DC behavior. Defect evolution, together with the increase of parameter variations, represents a serious challenge for traditional delay test methods based on fixed time delay limit setting. One alternative to deal with variation relies on adopting correlation where test limits for one parameter are settled based on its correspondence to other circuit variables. In particular, the correlation of circuit delay to reduced V_{DD} has been proposed as a useful test method. In this work we investigate the merits of this technique for future technologies where variation is predicted to increase, analyzing the possibilities of detecting resistive shorts and opens.

1. Introduction

CMOS IC scaling has provided remarkable improvement in electronic circuits performance during the last decades. However, as the silicon industry is moving towards the end of the roadmap, controlling the fabrication of these small devices is becoming a great challenge. In achieving the primary goals of device scaling such as performance, density and reliability, some other side effects appear like (i) Newer technologies are more susceptible to defect introduction, reliability and soft error problems, and (ii) Scaling increases the variations in device parameters such as channel length and width, oxide thickness, threshold voltage, etc. Consequently a large variation in performance (power consumption, delay, leakage, etc…) among different chips, and even different regions within the die, is expected.

It has been extensively shown that parameter variations and noise-induced fluctuations, aggravated in nanometer technologies, have a significant impact on the variation of signal paths delay from die to die and within die. Although there can be some deterministic components in the parameters influencing delay such as topological dependencies of device and interconnect processing or lithography correlation, their complexity in large designs together with the impact of environmental effects (such as supply voltage fluctuations, temperature, etc.), and the existence of real random variables (random doping fluctuation) makes it more appropriated to treat these variations as random. These increasing variations pose several challenges to parametric test methods based on setting a limit value on the test observable, like delay or I_{DDQ}, because such a limit value changes in practice not only from die to die, but also for different paths or regions within the same circuit.

Different test techniques have been developed to cope with the problem of parameter variations, among which those based on parameter correlations have been shown to provide good results in identifying outliers from the normal distribution [1]. These techniques correlate the test observable to other parameters in the circuit for which the fundamental physical relationships are well known. Correlation methods are based on the fact that intrinsic circuits will define a normal population distribution, while defective parts will fall out of such a distribution and will show up as outliers.

One of the proposed methods that received a significant attention is based on correlating the supply voltage reduction to the induced change on the circuit delay. The relative increase of the circuit delay when the supply voltage is lowered provides a distribution that can be used to identify possibly failing parts. Several techniques have been proposed based on this principle by either identifying the minimum supply voltage for which the part will run [1], or analyzing the dependency of the circuit delay on the supply voltage [2]. However, less attention has been given to the delay variation dependence with the progressive lowering of the supply voltage. In this work we analyze such a dependency showing that, as the supply voltage gets close to the device threshold voltage, the relative impact of parameter variations on the delay increases significantly. This effect introduces more uncertainty on the predicted path delay at reduced V_{DD}, thus making delay testing at low supply voltages less effective.

2. Background

2.2 Low V_{DD} testing

Low V_{DD} testing has been used to expose the presence of defects causing small extra delay at nominal voltage since the relative delay increase at lower supply voltages is more pronounced [2][5].

Another application of this concept lowers the supply voltage at a given clock frequency, and measures the minimum value of the supply voltage at which the circuit still works. This technique

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is referred to as MinV_{DD} [6]. The drawbacks of this technique for production testing relate to the increase in test time, and the cost of performing a search for the minimum supply voltage test for at which the die still passes the test. To overcome the search time penalty of the MinV_{DD} test, a three-step process was proposed based on MinV_{DD} to detect outliers and a posterior statistical process for outlier screening [7]. Although the impact of supply voltage lowering on the circuit delay has been extensively analyzed, less attention has been given to the impact of parameter variations [8].

2.3 Delay Variance at reduced V_{DD}

One of the main limitations of delay testing in nanometer technologies comes from the increase in parameter variations observed for these circuits. The relative increase of both within-die and die-to-die parameter variations with respect to older technologies represents a challenge to traditional delay testing since the adoption of a fixed time delay limit for all the circuits is not valid. Moreover, the adoption of a given delay test strategy within a supply voltage reduction scenario requires not only a careful analysis of the delay variation with the supply voltage, but also the consideration of the delay spread variation at the different supply voltages considered.

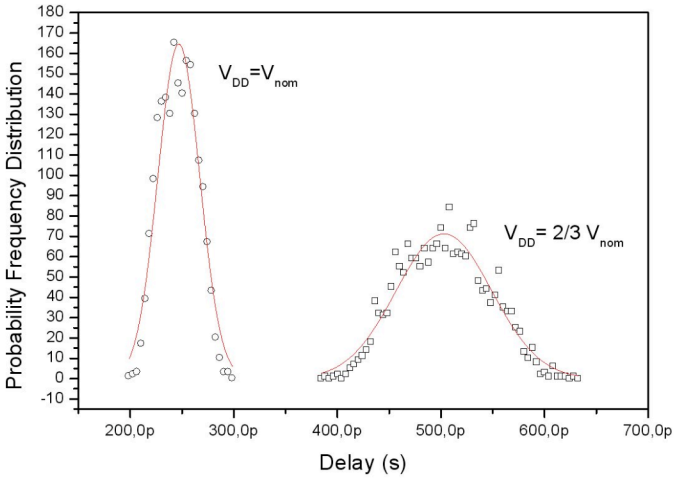

Figure 1. Path delay distribution for a 130 nm 12 inverters chain at two supply voltages. Gaussian fitting of the distribution gives A=4E-9, μ=2.47E-10, σ=1.75E-11 at the nominal supply voltage V_{nom} = 1.2 V, and A=8E-9, μ=5.04E-10, σ=4.14E-11 at 2/3V_{nom}.

Determining the dependence of the delay spread with the supply voltage reduction is crucial to develop an efficient delay test strategy, as it will have a direct impact on the method used to determine the delay limits settled for each path. A miss consideration of this effect may lead to an incorrect limit setting, and may therefore lead to defect escapes or, conversely, mark as defective a fault-free circuit thus contributing to overkill. Figure 1 shows the path delay distribution for a 12 inverters chain obtained from Montecarlo analysis for a 120nm technology at both the nominal 1.2 V, and at a reduced 0.8 V [8]. Not only the net (mean) delay increases, but also does the delay variance.

This effect can be understood by analyzing the dependency of the circuit delay when lowering the supply voltage considering (as a first approach) that the main contribution to the delay variation comes from the devices through the threshold voltage fluctuation [9]. The conventional form of the MOSFET drain current (I_d) is typically related to the gate delay T_{pd} using the set of equations from [10]:

$$I_d \propto (V_{DD} - V_T)^{\alpha} \quad (1)$$

$$T_{pd} \propto \frac{V_{DD}}{I_d} \propto \frac{V_{DD}}{(V_{DD} - V_T)^{\alpha}} \quad (2)$$

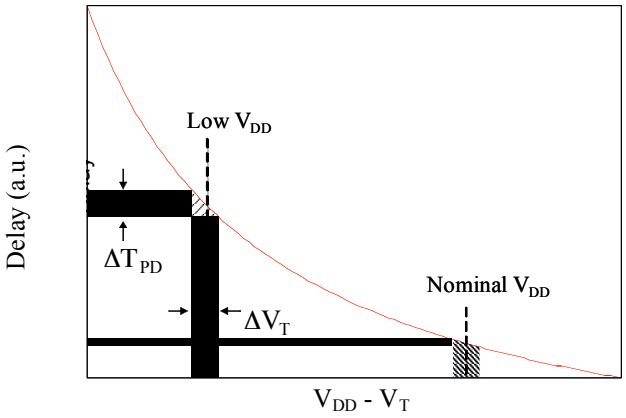

Figure 2. Illustration of the impact of a fixed V_T variation (ΔV_T) on the circuit delay for the nominal V_{DD} and a low V_{DD} voltages.

Depending on the technology, α ranges between 1 and 2. In [8] it is shown that for the 130nm technology used in this work Equation (2) provides an excellent description of the circuit delay if α =1.5 and V_T = 290 mV. A plot of this dependence (Figure 2) illustrates the impact of a fixed transistor threshold voltage variation (ΔV_T) on the circuit delay by representing the delay vs. (V_{DD} – V_T). It is shown that the same amount of V_T variation leads to a much higher circuit delay variation at a reduced V_{DD} with respect to the nominal supply voltage.

The relative impact of the delay variations when scaling V_{DD} can be quantified by differentiating T_{pd} with respect to V_T in Equation (2) thus obtaining the relationship between the circuit speed scattering and ΔV_T

$$\Delta T_{pd} \propto \frac{\Delta V_T \cdot V_{DD}}{(V_{DD} - V_T)^{\alpha+1}} \quad (3)$$

This relationship indicates that the V_T key role in circuit performance is even more important as V_{DD} is scaled down towards V_T. The exponent of α+1 in the delay variation equation denominator also shows the impact of V_{DD} reduction on ΔT_{pd} increase. Moreover, as V_{DD} approaches V_T the impact of V_T fluctuations are also magnified.

3. Impact of Shorts on delay at reduced V_{DD} - Dynamic critical resistance

We present a detailed study about the impact of two types of defects on a CMOS circuit delay at different supply voltages: resistive opens, and node to V_{DD}/GND resistive shorts. Opens have been shown to represent common failure mechanisms in nanometer technologies (resistive vias and opens [11]), while resistive shorts model spot-like defects. The node-to-node

resistive short can be descried as a straightforward extension of the node-to-rail case as shown later.

We analyze the impact of these defects on delay, and investigate their testability by means of delay testing. The goal of the work is to determine if the application of delay testing for a given circuit at a reduced voltage increases the sensitivity of the test with respect to the nominal supply for the defects considered. Having this in mind we analyze the relative impact of the defect on the delay at different supply voltages by determining its *dynamic critical resistance (DCR),* defined as the value of the defect resistance (either for open or short) for which the delay of a given circuit path increases up to the value of the 3σ distribution at a given supply voltage. The definition of DCR is illustrated in Figure 3. The analysis of the DCR dependence with the supply voltage will determine the benefit of applying a given delay test methodology at reduced supply voltages. Note that the goal of this analysis is not to guarantee a detection of a given short in a circuit by using delay testing, but to provide a comparative analysis to determine the benefit of lowering the supply voltage to expose resistive defects.

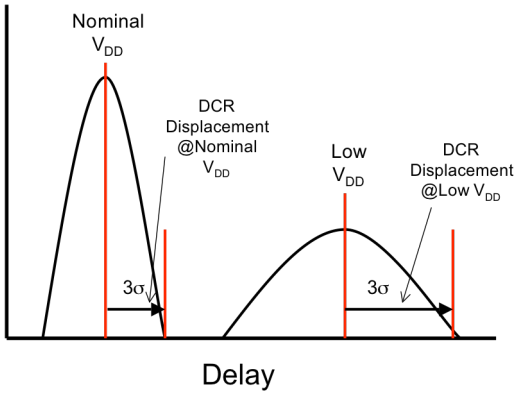

Figure 3. DCR concept for two different supply voltages.

To carry this analysis we derive an analytical expression for the DCR by placing a short to a circuit whose fault free delay is the mean delay of the distribution, and equating its faulty circuit delay expression to the 3σ delay of the distribution. The solution of such an equation provides an expression for the DCR. The dependence of such an expression with the supply voltage will determine the feasibility of low voltage delay testing for that particular defect.

3.1 Gate Delay Model

Using the model developed in [12] for deep submicron technologies, the delay of a CMOS gate occupying position *i* in a chain of N elements is expressed in terms of the input slew time (related to the input capacitance C_{i-1}), and the gate fan-out (related to the output capacitance C_i). The delay also depends on the supply voltage V_{DD} and the transistor threshold voltage V_{TH}, and is given by [12]:

$$t_D = \frac{C_{i-1}V_{DD}}{K_{i-1}\left(V_{DD}-V_{TH_{i-1}}\right)^{\alpha_{i-1}}}\left[\frac{1}{2}-\left(1-\frac{V_{TH_i}}{V_{DD}}\right)\frac{1}{1+\alpha_i}\right] + \ln(2)\tau_i \qquad (4)$$

The upper term in (4) depends on the input transition characteristics, while the bottom one is depends on the gate output load ($\tau_i=R_iC_i$). R_i is the effective resistance of the pull-up (or pull-down) transistors and is given by [12]:

$$R_i = \frac{V_{DD}}{2\ln(2)K_i\left(V_{DD}-V_{TH_i}\right)^{\alpha_i}} \qquad (5)$$

where K_i is related to the conductance of the pull-up (or pull-down) transistors. If the pull-up (pull-down) network consists of a N series-connected transistors, then K_i is given by:

$$K_i = \frac{K_{N(P)}}{1+\kappa(N-1)} \qquad (6)$$

Parameter $K_{N(P)}$ is related to the transistor conductance, and the drain saturation current is given by:

$$I_{DS_{N(P)}} = K_{N(P)}\left(V_{GS}-V_{TH_{N(P)}}\right)^{\alpha_{N(P)}} \qquad (7)$$

Parameter κ in (6) depends on process parameters:

$$\kappa = \frac{3V_{D0}\alpha(1+\gamma)}{5\left(V_{DD}-V_{TH}\right)} \qquad (8)$$

where V_{D0} is the gate saturation voltage, α is the velocity saturation index (Sakurai's exponent), γ is the linealized body effect parameter, and V_{TH} is the transistor's threshold voltage.

3.2 Including the effect of parameter variations

Eq. (4) describes the dependency of the gate delay with technology and design parameters, and the supply voltage. If any of these parameters, say **x**, is subjected to variation, then the delay $t_D(\mathbf{x})$ is also subjected to variation and when **x** increases by Δ**x** to **x**+Δ**x,** the delay changes to $t_D(\mathbf{x}+\Delta\mathbf{x})$ within the parameter distribution. From Eq. (4) the expression of the delay when **x** lies at the edge of the distribution (denoted as $\mathbf{x_{nom}}+3\sigma_x$) is given by:

$$t_D(\mathbf{x}_{nom}+3\sigma_{\mathbf{x}}) \approx t_D(\mathbf{x}_{nom})\left[1+\frac{3\sigma_{TH}}{V_{DD}-V_{TH}}+\frac{3|\sigma_K|}{K_i}\right] \qquad (9)$$

where σ_{TH} and σ_K, are the standard deviations of the threshold voltage and gate conductivity K_i (related to gate length, gate oxide thickness , gate width or carriers' mobility variations). The delay of a given path in the circuit will have an expression similar to Eq. (9), given by:

$$t_{path}(\mathbf{x}_{nom}+3\sigma_{\mathbf{x}}) \approx t_{path}(\mathbf{x}_{nom})\left[1+\frac{3\sigma_{TH}}{V_{DD}-V_{TH}}+\beta\right] \qquad (10)$$

Where t_{path} is the path delay, and β is a supply-voltage independent parameter.

3.3 Resistive open

The inline resistive open and the equivalent circuit used to compute the delay are shown in Figure 4. The output impedance

of the gate driving the interconnect line is described through its output resistance R_i as detailed in the previous subsection. R_{DEF} is the open defect resistance, while the capacitors C_1 and C_2 model the node capacitances of the interconnect portions between the gate output and the defect site, and the defect site and the gate load respectively. The total output capacitance is $C_i = C_1+C_2$ and is equal to the total output capacitance of the gate in the fault free circuit.

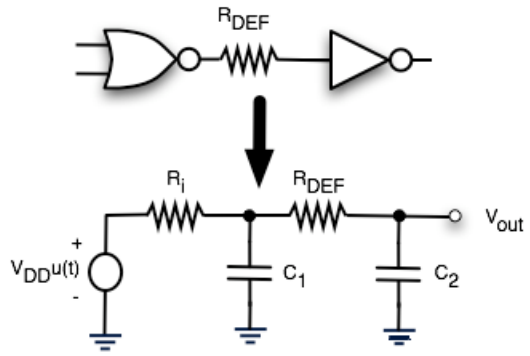

Figure 4. Illustration of the in-line resistive open and the equivalent circuit used to compute the delay.

As a first approach we consider a step input transition of the form $V_{DD}u(t)$ (u(t) being the Heaviside function) that will be modified later to have a non-zero transition time. The output response is obtained using simple circuit theory analysis, leading to:

$$V_{out}(t) = V_{DD}u(t) + \frac{V_{DD}A}{p_+(p_+ - p_-)}e^{p_+ t} + \frac{V_{DD}A}{p_-(p_- - p_+)}e^{p_- t} \tag{11}$$

where parameters A, p_+, and p_- are given by:

$$A = \frac{1}{R_i R_{DEF} C_1 C_2}$$
$$p_\pm = -\frac{AK}{2}\left[1 \pm \sqrt{1 - \frac{4}{AK^2}}\right] \tag{12}$$
$$K = \left(R_i C_i + R_{DEF} C_2\right)$$

Equation (11) has a real solution if $AK^2>4$. When $AK^2=4$ the circuit output voltage is given by:

$$V_{out}(t) = V_{DD}u(t) + V_{DD}e^{pt} + V_{DD}pte^{pt}$$
$$with \quad p = -\frac{2}{R_i C_i + R_{DEF} C_2} \tag{13}$$

The gate propagation delay is obtained equating (11) or (13) to $V_{DD}/2$. The delay obtained from (11), if $p_+>>p_-$, is given by:

$$t_D = -\frac{\ln(2)}{p_-} = \frac{\ln(2)}{\frac{(\tau_i + \tau_2)}{2\tau_1\tau_2}\left(1 - \sqrt{1 - \frac{4\tau_1\tau_2}{(\tau_i + \tau_2)^2}}\right)} \tag{14}$$

where τ_1, τ_2, τ_i are:

$$\tau_i = R_i C_i \quad \tau_1 = R_i C_1 \quad \tau_2 = R_{DEF} C_2 \tag{15}$$

A closed delay formula cannot be obtained from Eq. (13) since a transcendent expression is obtained, but it is possible to obtain a value for which the output variation is maximum (typically very close to $V_{DD}/2$). This value is obtained equating the second derivative of the output voltage to zero:

$$t_D = \frac{\tau_i + \tau_2}{2} \tag{16}$$

Solutions (14) and (16) provide the two limit values of the propagation delay (case $p_+>>p_-$ and case $p_+=p_-=p$). To simplify our analysis we take the lineal approximation to (14) at $R_{DEF}=0$ getting:

$$t_D = \ln(2)(\tau_i + \tau_2)\left[1 - \frac{\tau_1\tau_2}{(\tau_i + \tau_2)^2}\right] \tag{17}$$

Eq. (17) has been obtained assuming a zero input transition time. For the real case of nonzero input transition time, an additional term must be added to (17), that depends on the input gate capacitance and the pull-up (or pull-down) resistance of the previous gate (R_{i-1}). This term is similar to the upper term in Eq. (4). Adding this input transition time dependence to (17), the total delay is given by:

$$t_D = \frac{C_{i-1}V_{DD}}{K_{i-1}\left(V_{DD} - V_{TH_{i-1}}\right)^{\alpha_{i-1}}}\left[\frac{1}{2} - \left(1 - \frac{V_{TH_i}}{V_{DD}}\right)\frac{1}{1+\alpha_i}\right]$$
$$+ \ln(2)(\tau_i + \tau_2)\left[1 - \frac{\tau_1\tau_2}{(\tau_i + \tau_2)^2}\right] \tag{18}$$

Note that Eq. (18) leads to Eq. (4) for the fault free case (i.e. no open defect: $R_{DEF} = 0$) as expected.

Eq. (18) provides the delay degradation dependence for a CMOS gate driving an interconnect line having a resistive open with resistance R_{DEF}. The DCR expression is therefore obtained equating the delay given by Eq. (18) to the expression of the delay at the limit of the distribution given by Eq. (10) ($t_D(\mathbf{x_{nom}}+3\boldsymbol{\sigma}_\mathbf{x})$). The obtained DCR will be the open resistance that degrades the propagation delay from the mean delay to its 3σ value. The delay expression Eq. (18) for the limit of $C_1= 0$, leads to the well known Elmore delay:

$$t_D(R_{DEF}) \approx t_D(R_{DEF} = 0) + \ln(2)R_{DEF}C_2 \tag{19}$$

The DCR for the whole path is obtained equating the delay increment in Eq. (10) due to parameter variations and the delay increment due to the defect providing:

$$DCR = \frac{t_{path}(V_{DD})}{\ln(2)C_2}\left(\frac{\sigma_{TH}}{V_{DD} - V_{TH}} + \beta\right)$$
$$\approx N\frac{\bar{C}}{2\bar{K}\ln(2)C_2}\frac{V_{DD}}{(V_{DD} - V_{TH})}\left(\frac{\sigma_{TH}}{V_{DD} - V_{TH}} + \beta\right) \tag{20}$$

where t_{path} is the path delay of the fault free circuit, N is the number of gates in the path, and C and K are mean values for the gate capacitance and gate conductance in the path. Eq. (20) provides the supply voltage dependence of the DCR. The expression obtained shows that, as the supply voltage is reduced toward V_{TH} (the transistor threshold voltage), the DCR increases and tends to diverge. Such a dependency indicates that as the circuit supply voltage is reduced, the value of the open resistance that increases the mean delay out of the delay distribution also increases. Therefore, the impact of a given resistive open on the

circuit delay will be relatively smaller as the supply voltage is lowered because of the delay variation increase.

3.4 Node to rail short

Figure 5 illustrates the node to rail (GND in this case) short, and the equivalent circuit used to compute the impact of the defect on the gate delay. The defect is modeled as a pull-down resistance. The extension of this defect model to a node-to-node short is straightforward: the defect resistance would be connected to GND through an additional resistance (say R'_i) corresponding to the output impedance of the gate driving the other shortened node. We assume that the gate input voltage is and ideal step (for a non-zero rising/falling input transition to the gate an additional term will be added as done with (18)). Using circuit analysis, the gate delay is derived from $V_{out}(t)$ and takes the form:

$$V_{out}(t) = V_{DD}\frac{R_{DEF}}{R_{DEF}+R_i}\left(1-e^{-\frac{R_{DEF}+Ri}{R_i R_{DEF} C_L}t}\right) \quad (21)$$

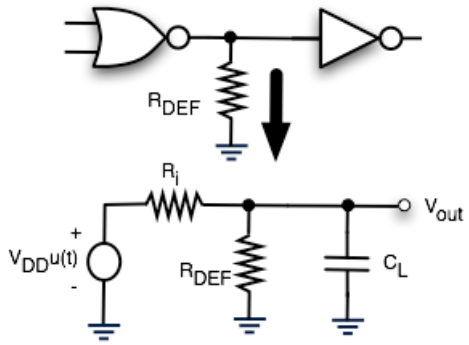

Figure 5. Node to GND short and equivalent circuit used to model the impact on delay.

The propagation delay is obtained from (21) as:

$$t_D = \ln\left(\frac{2R_{DEF}}{R_{DEF}-R_i}\right)\frac{R_{DEF}}{R_{DEF}+R_i}R_iC_L \quad (22)$$

For the case of interest where the short impacts mainly the delay ($R_i << R_{DEF}$) such a delay is given by:

$$t_D = R_iC_L\left(\ln(2)+\frac{R_i}{R_{DEF}}(1-\ln(2))\right) \quad (23)$$

Therefore, as a first approach (neglecting the input slew time, i.e. $C_{i-1}= 0$) from Eq. (4) we can write Eq. (23) as:

$$t_D \approx t_D(R_{DEF}=\infty)\left(1+\frac{R_i}{R_{DEF}}0{,}443+\left(\frac{R_i}{R_{DEF}}\right)^2 0{,}27\right) \quad (24)$$

Similarly to the previous case we compute the DCR equating (24) to the worst case propagation delay due to parameter variations (Eq. (10)). The solution of this equation is a complex function that has been used to compute the exact value of the DCR reported in the following section. To get a trend of the DCR dependence with the supply voltage, we analyze the first order solution of such an equation, given by:

$$DCR = 0{,}32\frac{V_{DD}}{K_i\left(\sigma_{TH}+\beta\left(V_{DD}-V_{TH}\right)\right)} = R'\frac{V_{DD}}{\left(\sigma_{TH}+\beta\left(V_{DD}-V_{TH}\right)\right)} \quad (25)$$

where R' is a supply-voltage independent resistance value. Note that in this case the dependence of the DCR with V_{DD} does not diverge when the supply voltage is reduced toward the threshold voltage. Eq. (25) indicates that the behavior of DCR is smooth with respect to V_{DD}, and depends on actual technology parameters. In the following section we explore this dependency for a 130nm technology using the full delay expression.

4. Experimental Validation

To verify the validity of the models derived we simulated the impact of resistive opens and node-to-rail shorts on the delay of a 10-gate chain on a 130nm technology. This number of gates was used to emulate the typical gate depth of today designs. The fault free path delay was first simulated both at the nominal 1.2 V and at a reduced 0.8 V supply voltages on a Montecarlo simulation for 1000 circuits to get the delay distributions at these two supply voltages. Then a defect resistance was placed on a particular node and its impact on the delay was simulated for a range of defect values at the two supply voltages.

4.1 Resistive open

Figure 6 shows the results for the resistive open defect model plotting the chain delay vs. the defect resistance for the two supply voltages. The nominal delay at the nominal supply voltage is 250 ps, while the 3σ delay value is at 300 ps. The intersection of the 3σ delay limit with the defect induced delay gives DCR = 20 kΩ at the nominal supply voltage. The nominal delay at 0.8 V increases to 478 ps and its 3σ delay distribution value is at 602 ps. At this supply voltage, the intersection between the defect-induced delay and the 3σ value occurs at DCR = 50 kΩ.

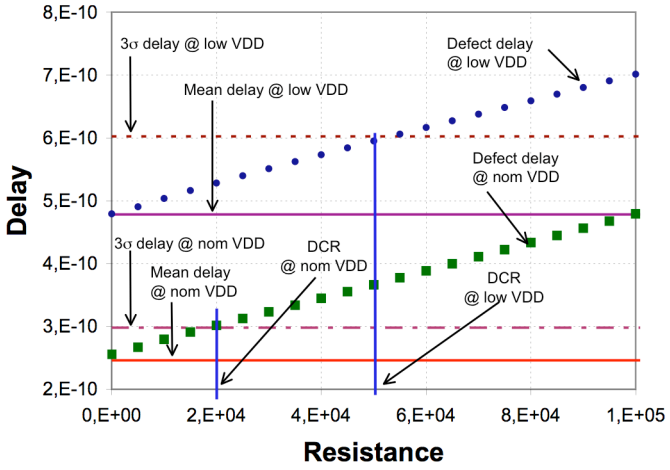

Figure 6. Impact of a resistive open on the circuit delay at two supply voltages (nominal V_{DD} and 2/3 of nominal V_{DD}) for a 130 nm circuit. The Dynamic Critical Resistance at nominal V_{DD} is 20 kΩ, while at the reduced V_{DD} it increases to 50 kΩ.

Since the lower the DCR value, the higher the defect detection capability, the observed increase in DCR at reduced supply voltages follows the dependency given by Eq. (20), and indicates a lower chance to detect this defect at reduced supply voltages. We computed the actual values of the DCR provided by the model developed in the previous section for the 120nm technology. The fault free delay curves were properly described from Eq. (10) setting σ_{TH}=0,054V, and β=0,15. Using these parameters we obtained the DCR values shown in Table I showing a very good agreement with Spice simulations since the maximum error is 10%.

Table I. Comparison of Spice simulations and the developed model of the DRC values for for a 130 nm technology.

		Resistive open	% err	Node to rail short	% err
1.2 V	Spice	20 kΩ	10	18 kΩ	2.7
	Model	22.4 kΩ		18.5 kΩ	
0.8 V	Spice	50 kΩ	6	20 kΩ	2.5
	Model	53.3 kΩ		19.5 kΩ	

4.2 Node to V_{DD} short

We repeated the simulation experiment inserting a resistance between the same circuit node short and the supply voltage (Figure 7). The values of the typical delays and 3σ values at the nominal and reduced supply voltages are the same than in the previous subsection since the circuit is the same. The intersection of the 3σ delay limit with the defect induced delay increase with respect to the typical delay value gives DCR = 18 kΩ at the nominal supply voltage, while at the reduced supply voltage the DCR = 20 kΩ. Note that in this case, the larger the DCR value, the higher the defect detection capability, since the fault-free case would correspond to an infinite defect resistance (in the previous case it was the opposite).

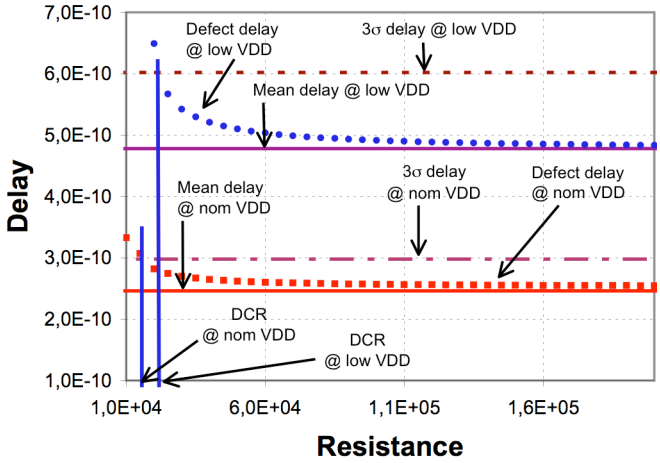

Figure 7. Impact of a node to V_{DD} short on the circuit delay at two different supply voltages (nominal V_{DD} and 2/3 of nominal V_{DD}) for a 130 nm circuit. The Dynamic Critical Resistance at nominal V_{DD} is 18 kΩ, while at the reduced V_{DD} it increases to 20 kΩ.

Therefore, for the node-to-rail short the application of the delay test at reduced supply voltage provides a better coverage, although the gain in defect sensitivity is moderate, since the DCR improvement is about 10%. Similarly to the previous case we computed the actual values of the DCR provided by the model developed in the previous section for the 120nm technology, using the parameters obtained for the fault free delay case, obtaining the values shown in Table I. Results show that for this defect the model provides even a better results since the error is below 3%.

5. Conclusions

Multi-V_{DD} test can be a powerful approach to detect resistive open/shorts in digital circuits. We have shown that the impact of process variations on delay testing at reduced V_{DD} may limit the sensitivity of this technique for nanoscale CMOS ICs. This reduced sensitivity comes from the increased spread of delay variations at supply voltages below the nominal supply values. This has been verified for resistive opens, observing that the relative value of the defect resistance required to displace a given fault free path delay out of the delay distribution is higher at reduced supply voltages. For the case of a node-to-rail resistive short the tendency is opposed, but the relative increase in defect sensitivity is moderate. This analysis pose a question about the advantages of running delay testing at supply voltages below the nominal value for a given technology.

References

[1] R. Madge, et. al. , "Obtaining High Defect Coverage for Frequency-Dependent Defects in Complex ASICs" IEEE Design and Test of Computers, Sept.-Oct. 2003, pp. 46-53.

[2] H. Hao and E. McCluskey, "Very-low voltage testing for weak CMOS logic ICs," *IEEE In.l Test Conference*, pp. 275-284, 1993.

[3] J. Segura and C. Hawkins, "CMOS Electronics: how it works, how it fails" IEEE Press – John Wiley & Sons, 2004.

[4] Y. Haihua and A. Singh, "A delay test to differentiate resistive interconnect faults from weak transistor defects", IEEE Int. Conf. VLSI on Design, 2005. 47 – 52, 2005.

[5] H. Yan, G. Xu, A. Singh, "Low voltage test in place of fast clock in DDSI delay test", Sixth Int. Symposium on Quality Electronic Design (ISQED), 2005.

[6] C.W. Tseng, R. Chen, P. Nigh, E.J. McCluskey "MINVDD Testing for Weak CMOS ICs". VTS 2001, 339-344.

[7] R. Madge, et. al., "Screening MinVDD outliers using feed-foward voltage testing analysis," IEEE International Test Conference (ITC), pp. 673-682, 2002.

[8] S. Bota, M. Rosales, J.L. Rosselló and J. Segura, "Low VDD vs. Delay: is it really a good correlation metric for nanometer ICs?", IEEE VLSI Test Symposium, 2006.

[9] S.W. Sun, G.Y. Tsui. "Limitations of CMOS supply-voltage scaling by MOSFET Threshold-Voltage variation". IEEE Journal of solid-state circuits, vol. 30, nº 8, 1995, pp 947-949

[10] T. Sakurai, A.R. Newton "Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas"IEEE Journal of solid-state circuits, vol. 25, 1990, pp 584-594.

[11] B. Benware, et. al., "Affrodable and effective screening of delay defects in ASIC using the inline resistance fault model" IEEE Int. Test Conference, pp. 1285 – 1294, 2004.

[12] J. L Rossello and J. Segura, "A Compact Charge-Based Crosstalk Induced Delay for Submicronic CMOS gates" XIII Int. Workshp. on Power and Timing Modeling (PATMOS 2003), Sept 2003.