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Dear Colleague,

Welcome to the DATE 07 Conference Proceedings. DATE combines the world’s leading electronic systems design conference and Europe’s leading international exhibition for electronic design, automation and test, from system level hardware and software implementation right down to integrated circuit design. The DATE 07 event features a technical program with 78 sessions covering the latest in system design and embedded software, IC design methodologies and EDA tool developments, together with an exhibition with the leading EDA, silicon and IP providers showing their new products and services. Challenges that you all face or soon will face in your daily practice are the increasing design complexity of highly integrated systems, the introduction of reconfigurability and embedded software, and the control of power, reliability and variability in nanometer IC designs. All these issues will be addressed in this year’s DATE event.

At its tenth anniversary, DATE 07 has again reached a record number (933) of submissions, compared to previous years and compared to other EDA conferences worldwide. With submissions coming from all five continents and almost fifty countries, DATE has truly become an international conference. DATE is now the world’s premier event in electronic system design. The submissions have been reviewed by the more than 600 members of the Technical Programme Committee. After a thorough review and selection process (with an average of 4.6 reviews per paper), finally 208 papers were selected for presentation at the conference. In addition, 57 papers were selected for Interactive Presentations, which highlight quality work in progress. Together with the invited special sessions (panels, embedded tutorials and hot topic sessions) this has resulted in a high-quality technical programme with 78 sessions covering the latest in system design and embedded software, IC design methodologies and EDA tool developments. One of the main strengths of the conference is a wide but high-quality coverage of design, design automation and test topics, from the system level (including PCB and FPGA) to the integrated circuit level. In addition, for the third year a special embedded software track is offered to allow for the increasing importance of software in embedded systems. Compared with previous years, submissions in design, test and embedded software have grown significantly, showing a clear trend toward a holistic view and a comprehensive system design focus. This year, papers are organized in 4 major areas:

- D – Design Methods, Tools, Algorithms and Languages
- A – Application’s Design
- T – Test Methods, Tools and Innovative Experiences
- E – Embedded Software

The DATE week opens on Monday April 16, 2006 at the Acropolis, Nice, France, with the offer of pre-conference tutorials. This year the five full-day tutorials cover topics of great interest to industrial designers. The first tutorial reviews the current state-of-the-art in NoC research and elaborates the main challenges for research and industrial applications. The second one provides detailed knowledge about the development of reconfigurable embedded systems from architecture and basic mechanisms up to high-level tools for system integration and application exploitation. The third tutorial discusses interactions between layout and manufacturability for devices and interconnects. Toward the system level, the tutorial discusses how on-die and on-wafer test and calibration structures can accelerate yield learning and adaptivity. The fourth tutorial introduces state-of-the-art technologies based on Simulink/Matlab for the design of multiprocessors on chip. The fifth tutorial starts by motivating the needs for and opportunities of Software Defined Radios, then discusses the trends and most promising approaches to implement reconfigurable digital baseband processing as well as reconfigurable RF front-ends and finally concludes by showing how a cross-layer optimization methodology can be used to translate the flexibility and energy-scalability into low-energy operation. Furthermore, six half-day tutorials are also proposed, three in the morning and three in the afternoon, covering aspects related to system-level design, test, analog and mixed signal design, packaging and bio-electronics.
The main conference opens on Tuesday April 17, 2007 with two very interesting keynote speeches. Tohru Furuyama, General Manager at Toshiba, will talk about the challenges of digital consumer and mobile SoCs, and Alan Naumann, CEO of CoWare, will challenge Darwin’s law by questioning whether design evolution stopped at RTL level. On the same day, the completely revamped Executive Track offers a series of panels with executives discussing their design needs: the fables companies, the consumer electronics market and the embedded automotive system designers.

On Wednesday April 18, 2007 a special full-day track is devoted to Ubiquitous Communication and Computation. Ubiquitous computing and communications bring the era where computing is part of everyday practices and natural environments at home, at work and in public spaces. By embedding computing resources and communicating seamlessly with them, we can hide the technology and provide services that are natural for humans to use. What was standard for a desktop computer technology in the early 80’s is available for numerous embedded devices that are used in the devices, rooms and buildings. Connecting anything, anywhere all the time opens possibilities for numerous new services and solutions. The many options and opportunities set challenges for the design, interoperability and verification for these systems. The design process is one key success factor in creating these heterogeneous systems. To manage the high design complexity and to manage the high variety of the systems and technologies the design and test tools have to support the abstraction of heterogeneous implementations, distributed specification, interoperability testing and test activities in general. Also, the design of efficient communications solutions, co-design on several abstraction levels, and system architectures as well as the development and integration of standards are major success factors. This special day focuses on some key technical challenges and potential uses of the ubicomp concepts. The sessions focus specifically on the applications, system architecture, communication and interoperability, security issues, power supply and power management issues.

New this year and to emphasize that DATE is the major event for the designers, DATE07 features two invited sessions where Europe’s famous consumer industry presents their best designs and design practices.

On Thursday April 19, 2007 a second special full-day track focuses on Space and Aeronautics applications. Space and Aeronautics have been innovative and technology pioneering industries in safety critical embedded systems for a long time, transferring state of the art concepts and technologies to other industries and setting standards in systems and software engineering. Recently, the fast growth of new high tech industries with mass markets has opened more and more opportunities for the space and aeronautics industries to transfer back a broad range of generic and high performance technologies, particularly in information and communication. Each transfer path has its own challenges, linked to different characteristics of each industry. The special day is illustrating these transfer challenges, and analyses what makes a difference in terms of:
- the value expected from the technology
- the nature and severity of the requirement set for the technology
- the role of the technology in the product context, being its hierarchy or its life-cycle
- the way technology is managed in the industrial context, being the development process or the 10
- internal and supply chain organisation

The special day is articulated around a keynote address, given by an executive representative of the European space and aeronautics industry. It introduces the strategic stakes and the international competitive landscape, for further development and understanding of the sizing dimensions of technology transfer all along the special day.

Seven special sessions complement the main conference program, with embedded tutorials, hot topics and panels on the most interesting issues today in electronic design. A first session looks at microprocessor architectures in the era of terascale integration. This raises the question addressed in a second session whether testing systems with multiple billions of transistors will be feasible. The increasing NRE cost of deep sub-micron silicon designs leads to the increased use of flexible application domain specific systems. This is discussed in two
sessions, one looking at heterogeneous systems on chip and systems in package, the other covering the future of customizable processors. The evolution to nano-scale semiconductor process technologies ripples through into the design area. Two panels discuss its influence on mixed signal and digital design, respectively. A last special session sketches the pivotal place EDA takes in the European Technology Platforms Artemis and Eniac, which structure the European government funded research in enabling hardware and software technologies for embedded systems.

Friday April 20 is the day for the DATE workshops. DATE offers the possibility to attend workshops as a complement to the regular conference. Seven workshops will run in parallel, covering emerging and important design topics including UML for SoCs, software and compilers for embedded systems, secure embedded implementations, embedded system design, diagnostic services for networks-on-chip, FPGAs and reconfigurable systems, and robust computing with nano-scale devices. Each workshop is structured into presentations from highly distinguished academic and industrial researchers.

Finally, throughout the conference days the DATE Exhibition is open to designers. The more than hundred exhibitors include the leading EDA, silicon, FPGA and IP providers showing their new products and services. This year, we welcome a record number of start-up companies, clearly showing the healthiness of the community. In addition, there is an Exhibition Theatre featuring talks from engineering managers of the leading electronic manufacturers on first-hand design experiences of commercial EDA tools. This year, the PCB symposium will also take place on Thursday afternoon as part of the exhibition theatre programme. The exhibition program offers also designers’ solutions workshops, which are short training sessions organized by vendors on specific topics such as closing the gap between design and test teams, transaction level modeling, IP verification, combining SystemC with SystemVerilog and DSP implementation techniques for FPGAs. The DATE week will also be a possibility for students and universities to show their research works, through the PhD Forum on Monday and the University Booth in the exhibition where hardware and software demonstrations will be shown by different universities on a rotation schedule. New this year is that the university booth is also open to demonstrate the pre-commercial results obtained in government funded projects.

The DATE 07 event’s program will be particularly attractive to industrial designers, both at IC, FPGA and embedded system level, to researchers and academics as well as to design managers, and an increasing attendance is anticipated.

We therefore invite you to take full advantage of the many opportunities offered to you by DATE 07, to improve and extend your knowledge and/or business in electronic system’s design and for socializing with peers and colleagues. We hope that you will fully enjoy this 10th anniversary of DATE.
Each year the Design, Automation and Test in Europe Conference presents awards to the authors of the most outstanding papers of the previous year's conference. The selection is performed by an award committee, based on the results of the reviewing process, the quality of the final paper and the quality of the presentation.

The paper selected as the most outstanding in the field of Design Methodologies is:

**Optimizing Sequential Cycles through Shannon Decomposition and Retiming**

*by S Soviani, O Tardieu and S A Edward, Columbia University, USA*

The paper selected as the most outstanding in the field of Test is:

**An Effective Technique for Minimizing the Cost of Processor Software-Based Diagnosis in SoCs**

*by P Bernardi, E Sanchez, M Schillaci, G Squillero and M Sonza Reorda, Politecnico di Torino, Italy*

The paper selected as the most outstanding Interactive Presentation is:

**Dynamically Reconfigurable Packet-Switched Network-on-Chip**

*by T Pionteck, C Albrecht and R Koch, Luebeck University, Germany*

**Congratulations to the winners!**
Tutorials

A  NoC at the Age of Six: Advanced Topics, Current Challenges and Trends
Organiser: Axel Jantsch, Royal Institute of Technology, SE
Speakers: Axel Jantsch, Royal Institute of Technology, SE
Luca Benini, DEIS – Bologna U, IT
Timothy M Pinkston, National Science Foundation and USC, US
Kees Goossens, NXP Semiconductors, NL
Pieter van der Wolf, NXP Semiconductors, NL
Alain Fanet, Arteris, FR
Marcello Coppola, STMicroelectronics, FR

The tutorial briefly reviews the current state of the art in NoC research and what has been accomplished during the last six years. The main challenges for research and industrial applications are elaborated.
Memory organisation: The pressing need to integrate the communication architecture with the memory architecture is analysed in the context of multimedia applications.
Design for performance: The tutorial presents a throughput-driven NoC design and evaluation approach that enables the designer to reason about various network design trade-offs.
Quality of Service: For many applications not only average but also worst case performance matters. Concepts and techniques for providing guaranteed bandwidth and latency.
Middleware: The software environment, middleware services and abstractions, required to efficiently support NoC-based platforms will be discussed in detail.
Finally, two industrial NoC based platforms, Arteris and Spidergon, are discussed and analysed.
The tutorial targets researchers, engineers and teachers that want to gain a thorough understanding of the current state of the art of NoC research, of the main challenges and the near future possibilities for industrial exploitation of this technology.

B  Reconfigurable Computing: Architectures, Tools and Applications
Organisers: Juergen Becker and Michael Huebner, Karlsruhe U, DE
Speakers: Juergen Becker, Karlsruhe U, DE
Michael Huebner, Karlsruhe U, DE
Andreas Herkersdord, TU Munich, DE
Walter Stechele, TU Munich, DE
Adam Donlin, Xilinx, US

Recent methods and reconfigurable architectures provide an increased design space by exploiting the dynamic and partial reconfiguration of hardware. The multi-adaptivity of this heterogeneous reconfigurable architectures reaches from adaptation to performance, to power consumption in relation of energy budgets, and to real-time adaptation for on-demand user requirements. The tutorial presents major issues in multi-adaptive system design:
- Hardware and techniques providing multi adaptivity during operation.
- Abstraction levels for operating dynamically reconfigurable architectures, incl. system level tool support.
- Efficient application exploitation of provided architectures and methods.

A detailed knowledge about the development of reconfigurable embedded systems will be provided by presenting a bottom-up approach from architecture and basic mechanisms up to high-level tools for system integration incl. application exploitation. The tutorial is addressed to hardware and system engineers as well as to researchers.

C  DFM Challenges and Practical Solutions in 65nm and 45nm
Organiser: Andrew B Kahng, UC San Diego, US
Speakers: N S Nagaraj, Texas Instruments, US
Jean-Pierre Schoellkopf, STMicroelectronics, FR
Mike Smayling, Applied Materials, US
Ban P Wong, Chartered Semiconductor, US
Andrew B Kahng, UC San Diego, US
In the 65nm and 45nm nodes, DFM tools and methodologies must solve growing challenges of systematic and random manufacturing variations, leakage power, reliability, and random defectivity - while remaining consistent with productivity and flow requirements. This tutorial will first discuss interactions between layout and manufacturability for devices and interconnects, including circuit impacts of both intrinsic and transient variability. Special circuits (analogue, SRAM), layout techniques (layout regularity, restricted design rules, new router capabilities, high-yielding cell libraries), modelling (stress and strain engineering), and IP development techniques (integration in arbitrary SoC density contexts) will be discussed.

Toward the system level, the tutorial will discuss how on-die and on-wafer test and calibration structures can accelerate yield learning and adaptivity, as well as the process abstractions used by design optimisations. Also treated will be the topic of IP qualification, portability and integratability in the face of fab-specific manufacturing challenges. Finally, the tutorial will review current and emerging DFM tools and methodologies (e.g., “yield score” metrics, parametric yield optimisations, and design for reliability), along with concrete opportunities for high-ROI DFM deployment.

The tutorial is targeted to IC and SOC designers and product engineers, IP core providers and integrators, R&D engineers in EDA and mask/equipment supplier industries, foundry interface engineers, and managers who are trying to solve parametric and defect yield challenges, and who would like to learn how DFM techniques can help.

D Simulink for Design and Programming Multiprocessor SoC
Organiser: Ahmed Jerraya, TIMA Laboratory, FR
          Pieter Mosterman, The MathWorks, US
          Janos Sztpanovits, Vanderbilt U, US
          Edward Power, SELEX Sensors and Airborne Systems, UK
          Tom Pitchforth, SELEX Sensors and Airborne Systems, UK
          Ahmed Jerraya, TIMA Laboratory, FR
          Gabriela Nicolescu, Ecole Polytechnique de Montreal, CA

Multi-processor SoC (MPSoC) are required for many emerging applications such as multimedia, telecommunication, and even consumer and automotive. Simulink/Matlab is emerging as the solid candidate for MPSoC design and programming. This tutorial introduces state-of-the art technologies based on Simulink/Matlab for the design of MPSoC:

- Prof. Wolf will give a brief introduction for designing and programming MPSoC.
- Dr Mosterman will talk about using Matlab/Simulink for embedded system design.
- Prof. Sztpanovits will talk about applying model-based techniques to refine Simulink models.
- Edward Power and Tom Pitchforth will detail a case study using Model Driven Design Techniques
- Dr Jerraya will introduce an approach using Simulink to program heterogeneous MPSoC.
- Prof. Nicolescu will present the usage of Simulink for modelling and simulation of heterogeneous systems.

E Software Defined Radios: Design for Scalability and Low Energy
Organisers: Liesbet Van der Perre and Bruno Bougard, IMEC, BE
Speakers: Trevor Mudge, U of Michigan, US
          Kees Van Berkel, NXP, NL
          Gerd Vandersteen, VUB/IMEC, BE
          Bruno Bougard, IMEC, BE
          Liesbet Van der Perre, IMEC, BE

“Anything, anywhere, anytime”, still, the motto having celebrated its 10th anniversary, today ubiquitous broadband wireless communication bringing multimedia services is not yet fully available. One of the major bottlenecks is the need for low cost, low power, multi-purpose chipsets. Indeed, the variety of wireless standards is large and evolving rapidly. Multi-mode terminals will be needed to provide optimised access according to virtually all those standards.
Software Defined Radios (SDRs) turn out to be the only valid solution to enable such versatile chipset in deeper submicron technology. Low power consumption SDR architectures are a vital asset of multi-mode wireless multimedia terminals.

In this tutorial, we will first introduce and motivate the needs and opportunities for SDRs. Next, we will go deeper into the technological challenges. Energy-aware SDRs require both an energy-scalable reconfigurable digital baseband modem and a energy-scalable reconfigurable RF section. The trends and most promising approaches to implement reconfigurable digital baseband processing will be first discussed. Special focus will be set on opportunistically partitioned heterogeneous MPSOC platform, SIMD processor architecture dedicated to baseband processing and hybrid coarse-grain-array/SIMD accelerators. Next, technologies and challenges to design reconfigurable RF front-end will be discussed. We will then show how a cross-layer optimisation methodology and a multi-level adaptive control approach can be used to translate the flexibility and energy-scalability into low-energy operation. Last but not least, we will analyse the consequence of the design paradigm shift induced by SDR on the design flow and tools, also identifying missing technologies towards future generations of SDRs.

Target audience: The tutorial is targeted towards designers (system, architectures, circuits, methods and tools) with interest in integrated wireless systems.

**F1 Microfluidic Lab-on-a-Chip Systems: Emerging Opportunities for EDA Researchers and Practitioners**

Organiser: Krishnendu Chakrabarty, Duke U, US  
Speakers: Krishnendu Chakrabarty, Duke U, US  
S (Krish) Krishnamoorthy, CFD Research Corporation, US

Advances in microfluidic technology have opened up non-traditional applications for electronic circuits and systems. Miniaturised lab-on-chip systems, which combine microfabrication and microfluidics with biological/chemical sciences, can be used for DNA sequencing, immunoassays, blood chemistry, environmental monitoring, etc.

This tutorial will first provide an introduction to microfluidics, underlying physical principles, applications, and advances in design automation techniques. Attendees will learn about continuous-flow systems, where tiny quantities of samples and reagents flow through microchannels and are subjected to analysis. Component level design issues involving filling, dispensing, mixing, dispersion, separation, heating, and biochemical assays will be illustrated, and solution strategies will be assessed with the help of simulations. The next part of the tutorial will focus on “digital” microfluidics, where discrete droplets are manipulated on-chip. The “digital core” of a lab-on-a-chip system can be viewed as a programmable processor, while the continuous-flow components can be used to implement specialised tasks such as chemical separation.

This tutorial is targeted towards EDA researchers and practitioners who are interested in the emerging area of microfluidic lab-on-a-systems, and who are looking for exciting new application areas for EDA algorithms.

**G1 Modelling, Analysis and Design of Bus-based SoC Communication Architectures**

Organiser: Nikil Dutt, UC Irvine, US  
Speakers: Nikil Dutt, UC Irvine, US  
Kanishka Lahiri, NEC Laboratories America, US  
Sudeep Pasricha, UC Irvine, US

On-chip communication architectures often dominate and critically affect the performance, power and cost of SoC (System-on-Chip) designs. Bus-based on-chip communication architectures that are frequently used in SoC designs today are evolving rapidly due to the combined effect of rapid changes in VLSI technology, coupled with the need to map ever more complex applications on to SoCs. This tutorial covers modelling abstractions suitable for communication-centric design, analysis techniques for estimating power, performance and reliability of different communication configurations, and the synthesis of current bus protocols and standards such as AMBA, CoreConnect and OCP-IP. We will also focus on advanced architectural concepts in bus-based communication architecture design, and present design examples from industry.
The tutorial is intended for designers, architects, managers, CAD tool developers, researchers and students interested in System-on-Chip design, platform-based design methodologies, interconnect issues at the system level and trends in on-chip communication architectures. Attendees should have a basic (undergraduate-level) knowledge of VLSI Design and SoC design flows. No specific knowledge of CAD tools or modelling languages is required for this tutorial.

**H1  Scan Delay Testing of Nanometer SoCs**
Organisers: Dimitris Gizopoulos, Piraeus U, GR and Kaushik Roy, Purdue U, US  
Speaker: Adit D Singh, Auburn U, US

Scan based delay testing is being widely considered as a cost effective solution for detecting delay defects that are emerging to be a major problem in nanometer technologies. This tutorial presents the basics of the scan based delay test methodology, including application of launch-on-capture and launch-on-shift patterns, and timing issues associated with the scan enable control signal. We also discuss challenges in effectively applying scan delay tests, including addressing poor test coverage, multi-cycle faults, false paths, power supply noise, clock stretching etc. Recently proposed methods to enhance delay test effectiveness, including targeting small delay defects, is also be presented. Prerequisites are basic familiarity with test and DFT.

The tutorial is targeted at designers and DFT engineers of integrated circuits (ICs) and system-on-chips (SoCs), IP core providers and integrators, test engineers, researchers, and managers responsible for ensuring the tested quality and reliability of advanced semiconductor components.

This tutorial is part of the annual IEEE Computer Society TTTC Test Technology Educational Program (TTEP)

**F2  Die and Package Power Delivery Analysis and Design for High-Performance and Low-Power Systems**
Organiser: Eli Chiprout, Intel Strategic CAD Labs, US  
Speakers: Byron Krauter, IBM Corp., US  
Rajendran Panda, Freescale Semiconductor, US  
Eli Chiprout, Intel Strategic CAD Labs, US

Power supply fluctuations can result in loss of performance or even system failure. This tutorial covers the underlying impact, analysis and design of a power delivery network (PDN) from the die to the package. It describes the impact of reliability, performance, and signal integrity constraints on PDN design. It covers electrical modelling approaches used on die, the tradeoffs involved and the dynamic impact of a die-wide model including interaction with the package. It includes practical modelling and analysis from an industrial point of view. Additionally, it covers recent progress in simulation-based and static PDN excitation approaches.

The tutorial is targeted at designers of power delivery constrained systems, engineers wishing to learn about power delivery issues and solutions, and CAD developers and researchers.

**G2  ESL, New Models and Methods to Advance System Level Design**
Organiser: Sandeep K Shukla, Virginia Tech, US  
Speakers: Arvind, MIT, US  
Rajesh Gupta, UC San Diego, US  
Sandeep K Shukla, Virginia Tech, US

ESL can be an enabler for advancing system level design, especially for effective SoC integration. In this tutorial, we examine recent advances in models, and methods that can lead to meaningful ESL tools. Some of these are incremental, e.g., enhancements to high-level modelling languages such as SystemC. Some represent ongoing work in improving abstraction and reuse of IP blocks. We focus on innovations being pursued related to capture and use of meta-data, meta-modeling and reflection mechanisms for reuse. We discuss how these can lead to easier system
modelling. Another area we cover is the paradigm of atomic action-oriented modelling for high level concurrency control, corresponding behavioural synthesis, and trade-offs. In particular, we will cover Bluespec’s programming model for a powerful ESL methodology that relieves designers from concurrency control concerns, thereby increasing productivity.

The tutorial targets designers of integrated circuits (ICs) and system-on-chips (SoCs), IP core providers and integrators, researchers, and managers who are involved in embedded system design at the system level.

H2 Practices in Analogue, Mixed-Signal and RF Testing
Organisers: Dimitris Gizopoulos, Piraeus U, GR and Kaushik Roy, Purdue U, US
Speakers: Salem Abdennadher, Intel Corporation, US
Saghir A Shaikh, Sun Microsystems, US

This tutorial describes the existing industry ATE-, DFT- and BIST-based testing solutions for mixed-signal and RF SoCs. Firstly, it looks at the basic concepts in analogue and RF measurements (i.e. eye diagram, jitter, gain, power compression, harmonics, noise figure, phase noise, BER, etc.). Secondly, it presents several examples of production testing of wired (SERDES) and wireless transceivers, as well as high-speed IO interfaces (e.g. PCI-Express and XAUI, etc). In addition, block-DFT solutions are also discussed for PLLs, equalisers, filters, mixers, AGCs, LNAs, DACs and ADCs.

A prerequisite for this tutorial is a basic knowledge of the design and production-test flows for mixed-signal devices. The tutorial is aimed specifically at design, test and DFT engineers involved in the actual implementation of mixed-signal and wireless devices and systems. However, architects and engineering managers would also benefit considerably from this session.

This tutorial is part of the annual IEEE Computer Society TTTC Test Technology Educational Program (TTEP)
The EDAA/DATE PhD Forum offers the opportunity for PhD students to present their thesis work to a broad audience in the design automation and test community from both academia and industry. During the presentation at the DATE Conference it helps students to establish contacts when entering the job market. On the other side, representatives from industry and academia get a glance of state-of-the-art research in design automation and test.

This year we received a total of 125 submissions out of which 53 have been accepted for presentation at a dinner reception. The review process was conducted by a team of 10 internationally renowned reviewers. Our thanks go to all presenters, the PhD Forum Committee and all who were involved in conducting the review process and arranging and organizing the Forum event at DATE in Nice. We also thank the EDAA and DATE organizers and representatives for making this Forum possible.

Jörg Henkel  
Chair 2007 EDAA/DATE PhD Forum

PhD Forum Committee  
J. Henkel (Chair), Univ. Karlsruhe, Germany  
R. Buchty, Univ. Karlsruhe, Germany  
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A. Shrivastava, Arizona State University, USA  
F. Slomka, Univ. Oldenburg, Germany  
Y. Xie, Penn. State University, USA

Presentations  
Angiolini, F., Univ. Bologna, “NoCs: From Idea to Implementations”  
Arteaga, A., Univ. Seville, “Digital Background Calibration of Pipeline ADCs”  
Bacivarov, I., ETH Zürich, “Performance evaluation for heterogeneous MPSoC design”  
Bombieri, N., Univ. Verona, “A TLM Design for Verification Methodology”  
Braun, A., Univ. Tübingen, “A semi-automated heuristics for guided performance optimization”  
Dopatka, F., Univ. Siegen, “A Framework for Implementing Realtime Industrial Ethernet Networks with Variable Compatibility to Standard Ethernet including Hot-Pluggable Asynchronous Devices”  
Faurax, O., Lab. SESAM Gardanne, “Model and tools for the evaluation of circuit robustness against fault attacks”  
Fawaz, N., HS Offenburg, “Biomedical Telemetry Application of an Electronic Capsule with Enhanced Performance”  
Fey, G., Univ. Bremen, “Increasing Robustness and Usability of Circuit Design Tools by Using Formal Techniques”  
Gorden-Ross, A., Univ. California Riverside, “Dynamic Optimization of Highly Configurable Caches for Reduced Energy Consumption”  
Hack, S., Univ. Karlsruhe, “Register Allocation for Programs in SSA-Form and possible Implications for Processors”
Harutyunyan, G., Yerevan Univ. Armenia, “Minimal March Tests for Fault Detection. Location an Diagnostics of Static and Dynamic Faults in SRAMS”
Kikkeri, N., South. Meth. Univ. Dallas, “Towards efficient Formal Hardware Verification by Theorem Proving”
Klingauf, W., Univ. Braunschweig, “Transaction-level HW/SW System Modeling with SystemC”
Lange, S., Univ. Leipzig, “Concepts and Methods for Hyperreconfigurable Architectures”
Ma (Ms.), M., McGill Univ. Montreal, “Model Order Reduction Methods for Efficient Modeling and Simulation fo Interconnect Networks”
Morra, C., Univ. Karlsruhe, “A flexible framework for hardware/software design space exploration using rewriting logic”
Muenker, C., Infineon Munich, “Spectral PLL BIST for Integrated Cellular Transceivers”
Narayanan, S., Penn. State Univ., “DATE 2007 PhD Forum Submission”
Neumann, B., RWTH Aachen, “Design and quantitative analysis of ASIPs with eFPGA-based accelerators as flexible ISA-extension”
Paci, G., Univ. Bologna, “Exploring temperature-aware design in low-power MPSoCs”
Padmanabhan, A., Lindquist Center Iowa, “SOG: A Self-organized Grouping Infrastructure for Grid Resource Discovery”
Rodriguez, F., Univ. Madrid, “Avoiding CAM structures on memory-disambiguation hardware”
Ruggiero, M., Univ. Bologna, “Abstract”
Shukla, S., Univ. Queensland, “QUKU: A Coarse Grain rSoC Architecture on FPGA”
Soffke, O., Univ. Darmstadt, “Modeling and Simulation of Printed RFID Tags in Inductively Coupled Systems”
Stitt, G., Univ. California Riverside, “Synthesis from Software Binaries”
Telando, V., Lab.Mat. & Microel. Toulon, “On-chip Voltage Regulator Protecting Smart Cards Against Power Analysis Attacks”
Troeger G., Univ. Heidelberg, “Improving Radiation Tolerance of FPGAs in High-Energy Physics applications”
Viana P., Univ. Bosque, Brasil, “A Methodology to Explore the Design Space of Memory Hierarchies for Embedded Systems”
Wang F., Penn. State Univ., Reliable “System Design atop of Unreliable Components”
Wedler M., Univ. Kaiserslautern, “Model generation for SAT-based property checking”
Wei Y., Univ. Stony Brook, “Research Abstract”
Zhu G., Univ. Waterloo, “Nonlinear Circuit Sensitivity Calculation and Distortion Decomposition”
Call for Papers

Scope of the Event
The 11th DATE conference and exhibition is the main European event bringing together designers and design automation users, researchers and vendors, as well as specialists in the hardware and software design, test and manufacturing of electronic circuits and systems. It puts strong emphasis on both ICs/SoCs, reconfigurable hardware and embedded systems, including embedded software.

Structure of the Event
The five-day event consists of a conference with plenary invited papers, regular papers, panels, hot-topic sessions, tutorials, workshops, two special focus days and a track for executives. The scientific conference is complemented by a commercial exhibition showing the state-of-the-art in design and test tools, methodologies, IP and design services, reconfigurable and other hardware platforms, embedded software, and (industrial) design experiences from different application domains, such as automotive, wireless, telecom and multimedia applications. The organisation of user group meetings, fringe meetings, a university booth, a PhD forum, vendor presentations and social events offers a wide variety of extra opportunities to meet and exchange information on relevant issues for the design and test community. Special space will also be allocated for EU-funded projects to show their results. More details are given on the website.

Areas of Interest
Within the scope of the conference, the main areas of interest are: embedded systems, design methodologies, CAD languages, algorithms and tools, testing of electronic circuits and systems, embedded software, applications design and industrial design experiences. Topics of interest include, but are not restricted to:

- System Design Methods, Algorithm and Tools
- Reconfigurable Computing
- System Level Specification and Modeling
- Innovative and Emerging Technologies, Systems and Applications
- System Synthesis and Optimization
- Simulation and Validation
- Design of Low Power Systems
- Power Estimation and Optimization
- Formal Verification
- Multi Processor and Network on Chip
- Microarchitectural and Architectural Design
- Architectural Synthesis
- Logic and Technology Dependent Synthesis for Deep-submicron Circuits
- Physical Design and Verification
- Analogue and Mixed A/D Systems
- Analogue and Mixed Signal Design, Symbolic Techniques
- Interconnect, EMC and Packaging Modeling
- Design and Application Case Studies
- System and Industrial Test
- BIST and Design for Testability
- Test Generation, Simulation and Diagnosis
- On-line Testing, Fault Tolerance and Reliability
- Testing of Analogue, Mixed-Signal, RF and Heterogeneous Circuits and Systems
- Defect-based Testing and Test of Regular Structures
- Real-time Systems and Middleware
- Compilers, Architectures, and Software Synthesis for Embedded Systems
- Model-based Design for Embedded Systems
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