Proven correct monitors from PSL specifications

Katell Morin-Allory, Dominique Borrione
Tima Laboratory, 46 avenue Félix Viallet 38031 Grenoble Cedex, France
katell.morin@imag.fr, dominique.borrione@imag.fr

Abstract

We developed an original method to synthesize monitors from declarative specifications written in the PSL standard. Monitors observe sequences of values on their input signals, and check their conformance to a specified temporal expression. Our method implements both the weak and strong versions of PSL FL operators, and has been proven correct using the PVS theorem prover. This paper discusses the salient aspects of the proof of our prototype implementation for on-line design verification.

1. Introduction

The design of VLSI Systems on a Chip increasingly involves the use and interconnection of large pre-existing components that are provided and validated by separate groups of engineers. In this context, assertion-based design [10] can be viewed as a unifying methodology across design teams and design description levels [12].

Assertions state functional and temporal properties about a component’s interface elements and/or state variables. Written in declarative form, they can be adapted to the syntax of various design description languages without any impact on their semantics (this is the approach taken by Accelera with PSL) [3]. The advantage is that asserted properties can be carried along the design steps, and serve a wide range of usages: specify the constraints for correctly using an IP, specify the result delivered by an IP, specify the expected correct behavior from the design at hand, generate and control test data, etc.

As a design property that is declared to be true, an assertion can be evaluated by one or more techniques among simulation, emulation or formal verification. An assertion can also be seen as a high level functional specification for a circuit primarily intended for snooping on events over time. Whether intended for design validation or for online embedded testing, a common technique can be applied: synthesize from the assertion a property monitor under the form of a RTL sequential circuit, and interconnect the design and the monitor via the monitored variables. This paper describes our method for providing efficient and proven correct property monitors for a formally defined yet user-understandable assertion language.

Our mechanism applies to a subset of PSL very close to what is referred to as its "simple subset" [3]. Intuitively, we only accept properties that can be evaluated “on the fly” by fixed size monitors during simulation or execution. A formal characterization of the largest PSL subset that satisfies this constraint still remains to be done. We initially selected this language for its clean and formal trace semantics. The method is based on a library of primitive digital components, and a technique to interconnect them. The resulting digital module can be properly connected to the signals of interest in the system under scrutiny, it runs concurrently with it, and notifies its environment when the property checking is terminated with a value true or false, or whether the property is still being evaluated. Both the weak and strong version of the PSL operators are covered. This paper discusses how we proved the correctness of monitors.

To the knowledge of the authors, the implementation and the proof of a solution for the strong version of the PSL operators has not been published before.

Related works

PSL originates from the Sugar input language to the RuleBase [6] symbolic model checker from IBM. M. Gordon played an essential role in the validation of the semantic definition. He performed a “deep embedding” of PSL in the HOL proof assistant, and used this mechanized system to demonstrate theorems about the semantics, and derive correct-by-construction mathematical observers for PSL properties [11]. Building on this seminal work, Tůrk translated a small unclocked subset of PSL FL expressions to LTL, still using HOL [15]: the interest of this work is only theoretical, as the resulting automata suffer from combinational explosion. Claessen and Martensson proposed an operational semantic definition guided by the structure of the PSL formula [8]; they exhibited some inconsistencies in the interpretation of a special class of regular expressions, and their work was useful for understanding. The published work only covered weak operators.

In automata-theoretic approaches, the transformation of PSL assertions to automata is exponential in the number of operators. Hardware design approaches are more usable in practice, as they construct a sequential machine whose memories encode rather than enumerate its reachable states. Using IBM’s FoCs [2] triggered our interest in the generation of monitors. From a PSL assertion, FoCs produces a source HDL process that acts as an internal monitor to the design under verification (DUV); the presence of error reporting statements makes FoCs output better fit for verification than for emulation and synthesis. Safelogic Verifier (now part of JasperGold) was another formal verifi-
cation tool taking a large subset of PSL as input. In both cases, weak operators only are recognized, and the formal method underlying the model extraction from PSL was not published.

Many more products are publicized to support PSL for model checking, simulation waveform generation, emulation and debug; many plug-in products add assertion support to pre-existing verification tools (see [1,5,9] for a list). To our knowledge, in most tools, the coverage of PSL primitives is very restricted, and the majority of companies advertise no formal guarantee that the PSL semantics are correctly supported. In contrast, this paper discloses a proven correct technology.

2. Principles of the FL Monitors Construction

In the PSL terminology, a property satisfaction level, on a finite execution path, may be one of:

- **Holds strongly**: No bad states have been seen. All future obligations have been met. The property will hold on any extension of the path
- **Holds (but does not hold strongly)**: Same as above except that the property may or may not hold on any given extension of the path
- **Pending**: No bad states have been seen. Future obligations have not been met. The property may or may not hold on any given extension of the path
- **Fail**: A bad state has been seen. The property will not hold on any extension of the path.

The main temporal operators of the “foundation language” (FL operators) have a strong and weak version. Intuitively, a property built on weak operators that is still pending at the end of a finite trace is considered satisfied. Conversely a terminating condition should have happened before the end of the trace (the property should at least hold) for strong operators.

The monitors we build reflect these definitions. When implemented in hardware, the monitor outputs display the property satisfaction level, and the indication that the answer is no longer pending may be used as an interrupt to trigger further actions. For technical reasons, the validity result is latched, and thus available on the output one clock cycle after it is known. This small delay is acceptable for all practical purposes. Note that a property satisfaction is not binary, and the negation of a strong operator is weak. Consequently, FL expressions may not be negated or “ored” in our subset (but they may be “anded”).

A monitor for a property \( P \) is built as a module that takes as inputs the reset, the synchronization signals (clock, handshake, etc.), a signal \( \text{Start} \) that triggers the evaluation, and the signals of the DUV that are operands of the FL operators in \( P \) (see Figure 4). The three monitor outputs have the following significance:

- **Checking**: a 1 indicates that output \( \text{Valid} \) is effective at the next synchronization time;
- **Valid**: provides the evaluation result (1 means absence of error, 0 means error);
- **Pending**: a 1 indicates that the monitor has been started and that the satisfaction result is pending; this is significant for strong operators.

![Figure 1. Interface of a monitor](image)

The “weak” version of the PSL operators are a simplified subcase of the “strong” version, so we shall only discuss the construction and the proof of monitors for the strong operators. In the following, we use the VHDL flavor of PSL, but the principles apply to other syntax as well. In the text and the figures, 0 and 1 are used both for bits ‘0’ and ’1’, and for Booleans False and True.

**Example 1** Assume we are interested in the behavior of signals \( A, B, C \) in a design synchronized by the rising edges of its master clock \( \text{Clk} \). We want to observe that signals \( A, B, C \) satisfy property \( P \), expressed as:

\[
P \text{ is an invariant, which states that whenever } A \text{ is 1, starting from two cycles later, it must be the case that } B \text{ takes the value 1 before } C \text{ takes the value 1.}
\]

![Figure 2. Waveforms for signals A, B, C](image)

Figure 2 gives two possible sequences of values observed on signals \( A, B, C \). The vertical dotted lines represent the successive rising edges of \( \text{Clk} \), which have been numbered for the purpose of this explanation. \( \text{Start, Checking, Valid} \)
Construction of complex monitors by interconnection of primitive components For complex properties, primitive single operator monitors are interconnected to construct a complex monitor. The method is based on the syntax tree of the property, where a node represents a PSL operator, a leaf represents a basic operand (signal or constant value), and the edges connect an operator with its operands. Some operators have two operands, some have only one.

- **Operators:** For each node in the tree structure of a property, a corresponding operator monitor is needed.
- **Operands of Boolean and Temporal operators:** The result of a simple Boolean expression (not a, a or b, ...) is directly connected to the corresponding operand input of the operator monitor. If the operand is a FL formula composed of other temporal operators, connect value 1 to the corresponding input of the monitor to disable the evaluation function within the monitor (it is done by other monitors).
- **Connection of consecutive FL operators:** For two operators N1 and N2 such that N2 is an operand of N1, the two monitors are connected in the following way (Fig. 3).
  - Output Checking of N1 is fed to input "start" of N2.
  - Output Valid of N1 is useless, and unconnected.
  - The clock and reset are shared by N1 and N2.
- **Initial State Generation:** A module "gen_init" is added to generate the initial state signal “init_cycle” one cycle after power up reset. This signal triggers the evaluation of the whole property, and is fed into input start of the root monitor.
- **Primary outputs:** Checking and Valid are those of the rightmost FL operator, Pending is the “or” of the Pending outputs of all the “strong” monitors.

In terms of post synthesis area, this solution is efficient for complex temporal properties [7], a significant advantage for online monitoring of embedded systems, specially on FPGA.

3. Principles of the proof of Correctness
The proof of correctness of both the library components and the interconnection method, with respect to the formal semantics of the PSL reference manual was done with the
The primitive monitors are written in the RTL synthesizable subset of VHDL. To prove each monitor correct, we first extract the finite state machine (FSM) model for the component, and translate it in the PVS input formalism. This process has been automated, with the help of symbolic simulation (see Figure 4).

We use THEOSIM [4] that takes as input a clock synchronized sequential circuit, and computes the state transition functions and output functions in a normalized conditional format. This tool performs a static stabilization of combinational circuits between clock edges (provided there is no combinational loop). This simulator defines the symbolic value of a signal as a function of the previous symbolic value of all signals of its cone of influence. Since bit-vectors are handled globally (i.e. represented by only one symbol), we can handle parameterized bit-vectors.

The translation of the symbolic expressions computed by the symbolic simulator into PVS input syntax is fully automated. It is essentially a simple transcription, except that VHDL objects are considered functions in the PVS model, both in their structural and temporal dimensions. More precisely, signals are modelled by bit vectors and therefore represented by a mapping from \( \mathbb{N} \) to their type. Since vectors are modelled by functions too, a bit vector is a mapping from \( \mathbb{N} \times [i,j] \) (where \( i, j \) are the first and last index of the bit-vector) to Boolean.

Then, the PSL semantics are represented in PVS, and we generate automatically several theorems for each operator. All theorems are proved with PVS (Figure 4).

**Example 2** The following VHDL text (left of Figure 5) is an excerpt from a primitive monitor RTL description. The output Valid is combinationally connected to an internal signal Valid_t (first line). The rest of the code is a sequential process that computes Valid_t at each rising edge of Clk, as a function of signals Reset_n, Check_en and some expression expr. The evaluate_expr process and the assignment of Valid are concurrent, and require two simulation iterations to stabilize at each rising clock edge. The right part of Figure 5 gives the representation in PVS of signal Valid.

```vhdl
valid <= valid_t;
begin
  if clk’event and clk=’1’ then
    if reset_n’event and reset_n=’0’ then
      valid_t <= ’1’;
    else
      if check_en = ’1’ then
        valid_t <= expr;
      else valid_t <= ’1’;
    end if;
    end if;
  end if;
end process;
```

**Figure 5. VHDL excerpt and translation into PVS**

### 3.2. Modeling the PSL semantics in PVS

The semantics of PSL are defined on the traces of all the observed signals on a time range \([t_0, T]\). Let \( \mathcal{FL} \) denote the set of FL expressions. Semantics are modelled by a mapping \( \text{Sem} \) from \( \mathcal{FL} \times \mathbb{N} \times \mathbb{N} \) to Boolean. Let \( \varphi \) be a FL expression, then \( \text{Sem}(\varphi, t_0, T) \) is inductively defined on the syntactic tree of \( \varphi \) on the time range \([t_0, T]\) for each operator \( \Omega \), we define a function \( \text{Sem}_\Omega \) implementing the semantics of \( \Omega \) and depending on function \( \text{Sem} \). Functions \( \text{Sem} \) and \( \text{Sem}_\Omega \) are mutually dependent. When \( \varphi \) is only a Boolean, \( \text{Sem}(\varphi, t_0, T) \) is defined by the value of \( \varphi \) at \( t_0 \).

**Example 3 (Semantics function of next_e)** The \( \text{next}_e[i,j] \) operator is a strong operator. It specifies that there is a next cycle, i.e., that the length of the trace on which the signal are observed is greater than \( i + 1 \), and that the property holds on cycle \( i + 1 \).

The modeling of this operator semantics in PVS gives us:

\[
\text{Sem}_{\text{next}_e}(\varphi, i, j, t_0, T) = \exists k \in [i, j], \text{Sem}_{\text{next}}(\varphi, k, t_0, T)
\]

### 3.3 Equivalence modeling

Let \( M \) be the monitor implementing a FL property \( \varphi \). The equivalence deals on the one hand with \( \text{Sem}(\varphi, t_0, T) \), on the other hand with the output signals of \( M \): \( \text{Checking}_M \) and \( \text{Valid}_M \) (relevant one cycle after \( \text{Checking}_M \) takes value 1) and \( \text{Pending}_M \). More formally, the equivalence can be modelled by the following expression:

\[
\forall \varphi, \forall t_0 \in \mathbb{N}, \forall T \geq t_0, H(\varphi, t_0, T) \implies S(\varphi, t_0, T) \iff (V(\varphi, t_0, T) \land P(\varphi, t_0, T))
\]

where \( S(\varphi, t_0, T) \) denotes an expression dealing with \( \text{Sem} \), \( V(\varphi, t_0, T) \) an expression dealing with \( \text{Valid}_M \).
and Checking, \( P(\varphi, t_0, T) \) an expression dealing with Pending\(_M\) and \( H(\varphi, t_0, T) \), the hypothesis under which the equivalence can be proved.

Let us define formally these four expressions. The value of the semantics of expression \( \varphi \) is relevant only if \( \text{Start}\_M \) was true at time \( t_0 \). As a first approximation, assume that \( S(\varphi, t_0, T) \) is defined by \( \text{Start}\_M(t_0) \implies \text{Sem}(\varphi, t_0, T) \).

**Expression of V** Expression \( V \) specifies that no bad states have been seen. By definition of monitors, the relevance of Valid\(_M\) is given by an active Checking\(_M\) at the previous cycle. Since Checking\(_M\) just represents the signal computed by the checking window, and since Valid\(_M\) is defined by True when this signal is not active, for all cycles \( t \) and for all monitors Checking\(_M(t) \implies \text{Valid}\_M(t + 1) \) is equivalent to \( \text{Valid}\_M(t + 1) \). This property is generated and verified for each monitor in PVS.

If \( S(\varphi, t_0, T) \) is verified, signal Valid\(_M\) must be verified during some cycles. But we cannot know a priori when Checking\(_M\) (and therefore Valid\(_M\)) is active. For some operators, it depends only on a parameter (e.g. next with delay), for others it depends on the activity of an event (e.g. next_event). To unify our modeling on all properties, we look at Valid on the whole time range \([t_0, T]\).

\[
V(\varphi, t_0, T) = \forall t \in [t_0, T], \text{Valid}\_M(t + 1) \tag{2}
\]

**Expression of P** Signal Pending is 1 when some future obligations have not been met. If Property \( \varphi \) should hold (or hold strongly) then at the end of the trace, all the future obligations must have been met. Since the computation of Pending is delayed by one cycle, \( P(\varphi, t_0, T) \) is defined by:

\[
P(\varphi, t_0, T) = \neg\text{Pending}(T + 1) \tag{3}
\]

**Expression of S** On \([t_0, T]\), Valid\(_M\) can depend on several active Start\(_M\). In our first approximation of \( S(\varphi, t_0, T) \), the semantics took into account only one active Start\(_M\) at \( t_0 \). We generalize this definition to the occurrence of several active Start\(_M\) on the studied range. We thus give the following definition:

\[
S(\varphi, t_0, T) = \forall t \in [t_0, T + 1], \text{Start}\_M(t) \implies \text{Sem}(\varphi, t, T) \tag{4}
\]

**Expression of H** The two previous paragraphs give us the expression of the equivalence between the operator semantics and the monitor output valuations. Let us now examine the hypothesis under which this equivalence is verified.

- Signals Checking and Valid are active only when signal Reset\(_M\) is not active, i.e. Reset\(_M\) is 1. We need Reset\(_M\) to be not active on \([t_0, T]\).
- The second hypothesis deals with Start. On \([t_0, T]\), Valid\(_M\) might depend on an active Start\(_M\) occurring before \( t_0 \); in that case, the equivalence would not be verified. To exclude this irrelevant case, we may either assume that Start\(_M\) was never active before \( t_0 \) (this is too strong an assumption), or assume that Start\(_M\) was never active since the last active Reset\(_M\). We use the second assumption.

These two hypotheses give us:

\[
H(\varphi, t_0, T) = \exists t' \in [0, t_0], \neg\text{Reset}\_M(t') \land \forall t_1 \in [t', T], \text{Reset}\_M(t_1) \land \forall t_2 \in [t' + 1, t_0], \neg\text{Start}\_M(t_2) \tag{5}
\]

### 3.4. Proof of Correctness

In this section, we break up the main lines of the proof of equivalence between the PSL formal operator semantics and the results delivered by their associated monitor. A complete proof can be found in [13]. It is is done by induction on the depth of Formula (1), whatever FL operator is considered. Let \( \Omega_1, \ldots, \Omega_n \) be \( n \) FL operators, and \( \varphi_n = \Omega_n \ldots \Omega_1 \text{op}_1 \ldots \text{op}_n \), a FL expression where \( \text{op}_i \) is a list of operands for \( \Omega_i \). Parameter \( n \) represents the depth of the formula (denoted \(|\varphi_n|\)).

Let \( M \) be the monitor implementing \( \varphi_n \). It is composed of \( n \) basic monitors \( M_1, \ldots, M_n \) (cf. Fig. 3). We denote \( \text{Start}_i, \text{Checking}_i, \text{Valid}_i \) and \( \text{Pending}_i \) the input and outputs of \( M_i \). Input Start\(_M\) is input Start\(_i\). Similarly output Valid\(_M\) is output Valid\(_i\). The Reset input of all monitors are connected to the global Reset\(_M\) input. In Formula (1), the terms \( H(\varphi_n, t_0, T), S(\varphi_n, t_0, T), V(\varphi_n, t_0, T) \) and \( P(\varphi_n, t_0, T) \) can be rewritten into:

\[
H_n(\varphi_n, t_0, T) = \exists t' \in [0, t_0], \neg\text{Reset}\_M(t') \land \forall t_1 \in [t', T], \text{Reset}\_M(t_1) \land \forall t_2 \in [t' + 1, t_0], \neg\text{Start}\_M(t_2)
\]

\[
V_n(\varphi_n, t_0, T) = \forall t \in [t_0, T], \text{Valid}\_M(t + 1)
\]

\[
S_n(\varphi_n, t_0, T) = \forall t \in [t_0, T + 1], \text{Start}\_M(t) \implies \text{Sem}(\varphi_n, t, T)
\]

\[
P_n(\varphi_n, t_0, T) = \forall t \in [t_0, T], P_{n-1}(\varphi_{n-1}, t_0, T) \land \neg\text{Pending}_n(T + 1)
\]

Our induction hypothesis is given by:

\[
I(n) = \{ \forall \varphi_n = n, \forall t_0 \in \mathbb{N}, \forall T \geq t_0, H(\varphi_n, t_0, T) \implies (S(\varphi_n, t_0, T) \iff (V(\varphi_n, t_0, T) \land P(\varphi_n, t_0, T))) \}
\]

**Base Case**: The first step is the proof of \( I(1) \). The expression \( \varphi_1 \) has only one operator, the operands of which are Boolean: we deal with a primitive monitor. Since the induction is done whatever \( \varphi_n \), we must prove \( I(1) \) for all FL operators. We thus generate and prove in PVS a theorem corresponding to expression \( I(1) \) for each operator and its primitive library monitor.

**Inductive Case** Assuming \( I(n - 1) \), we want to prove \( I(n) \). The proof of this implication is based on two facts:

- First, due to the interconnection method, Checking\(_n\) is equal to Start\(_n-1\).
- Second, we can rewrite expression \( \varphi_n \) into:

\[
\varphi_n = \Omega_n(\varphi_{n-1}, \text{op}_n)
\]

By definition of Sem, we have

\[
\text{Sem}(\varphi_n, t_0, T) = \text{Sem}\_\Omega_n(\varphi_{n-1}, \text{op}_n, t_0, T)
\]
In the function defining $\text{Sem}_{\Omega_{\text{new}}}$, $\varphi_{n-1}$ is always used as a parameter of the $\text{Sem}$ function. Furthermore, operand $\varphi_{n-1}$ of $\text{Sem}_{\Omega_{\text{new}}}$ can be a Boolean expression. It may be substituted by $\lambda t. \text{Sem}(\varphi_{n-1}, t, T)$. This lambda term is a Boolean function, and is generalized to any Boolean function.

These two rewritings are the salient aspects of the inductive proof. For each operator, we simplify the proof in two equivalences, the conjunction of which is stronger than $I(n - 1) \implies I(n)$.

3.5. Results

To gain experience, we first proved the weak version of the primitive monitor library, then extended the model to the strong version of the FL operators and performed the proof of the strong monitors. No errors were found in the weak library. For one strong operator, $\text{next}_e$, the base case proof lead to an error in the proof of $I(1)$. Since the weak version of this monitor was correct, the error had to come from the implementation of the $\text{Pending}$ signal: this signal was not significant at cycle $T + 1$ the end of the trace, but at $T + j - i$ (where $j$ and $i$ are parameters of this operator). This error was corrected and the new correctness proof succeeded.

For each operator, we defined a theory in which we specify several theorems. It represents approximately 270 lines of code. Then this theory is automatically type checked: this generates roughly 10 instructions: from the catch-all strategy “grind” that automatically completes a proof branch by installing rewritings and simplifications, to the “inst” that instantiates a quantified variable by a given expression or the use of an intermediate lemma. For $\text{next}_e$, we use a thousand instructions. For a family of operators, the intermediate lemmas and proof strategies could largely be reused.

4. Conclusion and current works

In this paper, we proved a methodology to generate monitors from PSL assertions. The technology is based on a library of primitive components that implement the weak and strong FL operators of PSL. Monitors for complex expressions are built by structurally interconnecting these basic blocks. Thanks to the use of theorem proving techniques, we obtain a proof that is independent of the valuation of the temporal parameters (number of cycles, or time interval) present in many operators.

A prototype implementation automatically synthesizes a monitor from a PSL property, as a RT-level VHDL component net-list. One or more monitors can be linked to the DUV, for formal verification, simulation, emulation, or online testing. Recent improvements to the prototype have included a user interface to help identify these interconnects, and the instrumentation of the synthesis on a FPGA platform with several software modules. The history of the observed signals can be saved, extracted, and viewed as waveforms, to help debug the DUV when a monitor outputs a property failure. Systematic experiments and measurements, reported in [7], show that the area of our monitors increases gracefully with the number of nested PSL operators, and the upper bound of the observation window of the ($\text{next}, \text{next}_e$) operators.

Future works in this area aim at applying the same principles on designs described at a more abstract level. The difficulty lies in correctly connecting synthesizable monitors with asynchronous communication mechanisms.

Acknowledgements The authors thank Y. Wolfsthal, E. Zarpas and G. Shapiro from the IBM Haifa Research Laboratory for their interest and for giving them free access to RuleBase and FoCs. Miao Liu was the main author of the primitive monitors library.

References