Systematic Methodology for Designing Reconfigurable ΔΣ Modulator Topologies for Multimode Communication Systems

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Abstract

This paper proposes a methodology for designing reconfigurable continuous-time ΔΣ modulator topologies. The methodology is based on the concept of generic topology that expresses all possible signal paths in a reconfigurable topology. Topologies are optimized for minimizing the complexity of the topologies, maximizing the sharing of circuitry for different modes, maximizing the topology robustness with respect to circuit nonidealities, and minimizing total power consumption. The paper presents a case study for designing topologies for a three mode reconfigurable ΔΣ modulator, and compares topologies with state-of-the-art design.

1. Introduction

With the emergence of new wireless communication standards, the circuitry in future personal wireless communication systems must support multiple operating modes, such as AMPS, GSM, CDMA, WCDMA, and UMTS [1, 2, 3]. A promising trend is to use reconfigurable receiver-on-a-chip that meets the resolution and bandwidth requirements of different communication standards [4]. In this approach, a main task is developing high performance, compact multimode analog to digital converters (ADC), in which the circuit netlists for different modes share as many analog cells as possible [1].

Reconfigurable multimode ADCs have two main advantages as compared to having a collection of single-mode ADCs: (1) Reconfigurable ADCs are much more compact [1]. (2) Design time, hence cost, is reduced. In reconfigurable ADCs, many blocks are shared between different modes. In the future, reconfigurable ADCs might be used in software controlled reconfigurable communication systems (software radio) that graciously adapt to new communication standards and performance constraints.

There is few work on reconfigurable multimode ADCs [1, 2, 3, 4]. Work is mostly on reconfigurable continuous-time ΔΣ modulators due to their power efficiency, superior linearity at low bandwidths, and inherent bandwidth resolution tradeoff in the noise-shaping characteristic. So far, the design of reconfigurable multimode ΔΣ modulators is manual and unsystematic. There is little understanding on how to develop optimal reconfigurable topologies for a new set of modes. Also, to improve design closure and reduce cost, topology design must contemplate a fair amount of circuit nonidealities. Existing techniques are either customized to a few single-mode topologies [5, 6], or consider ideal systems without any nonidealities [7, 10]. In conclusion, more efficient methodologies are needed for systematically designing reconfigurable ADCs while contemplating nonidealities early in the design flow.

This paper proposes a methodology for designing reconfigurable continuous-time ΔΣ modulator topologies. Topologies are optimized for minimizing the complexity of the topologies, maximizing the sharing of circuitry for different modes, maximizing the topology robustness with respect to circuit nonidealities, and minimizing total power consumption. The methodology is based on the concept of generic topology that expresses all possible signal paths in a reconfigurable topology. We present the modeling of generic topologies including four types of nonidealities: (1) integrator related, (2) quantizer related, (3) feedback DAC related and (4) circuit related nonidealities. Models are used in the methodology to set up a set of nonlinear equation sets. Equations are solved for finding efficient reconfigurable topologies. Found topologies are then refined using Simulink simulation of models with more detailed nonidealities.

The paper is organized as follows. Section 2 summarizes related work. Section 3 is on modeling of modulator nonidealities for design. Section 4 presents the proposed topology design methodology. Section 5 discusses the case study. Finally, conclusions are offered.

2. Related work

There is currently no work on methodologies for systematic design of reconfigurable ΔΣ topologies. Existing
research [1, 2, 3, 4] presents design cases, but no methodology is introduced.

Current design methodologies are for single-mode $\Delta \Sigma$ only. Most of the work is on topology parameter optimization with limited modification of a modulator topology. Medeiro et al. [5] propose a design flow based on extensive analysis and modeling of the nonidealities that degrade the $\Delta \Sigma$ modulator performance. However, their methodology is limited to the four single-mode, discrete-time topologies supported by CAD tools – SDOPT and FRIDGE. Francken et al. [6] describe an approach for high-level simulation and synthesis of discrete-time $\Delta \Sigma$ modulators. Behavioral models for integrators, quantizer, and feedback digital-to-analog converter (DAC), are integrated in a synthesis tool (DAISY) that selects the modulator topology with the lowest power consumption for a given specification and constraints for the building blocks. An analytical integration method for the simulation of continuous-time $\Delta \Sigma$ modulators is suggested in [8]. However, the set of allowed topologies is not complete, thus optimal solutions might be missed. Tang et al. [7] present a synthesis algorithm that finds the optimal topology for a given specification by solving a mixed-integer nonlinear programming (MINLP) problem with a cost function expressing the signal path complexity, sensitivity, and power consumption of the topology. This method considers only single-mode $\Delta \Sigma$ modulators built out of ideal blocks.

Design methodologies for single-mode $\Delta \Sigma$ modulators cannot be directly used for developing reconfigurable multimode ADCs, because they lack any capability of conducting global optimizations across the multiple modes. Hence, while solutions might be optimal for each mode, they are hard to be integrated into a reconfigurable ADC that shares as many blocks as possible between its different modes.

3. Modeling for reconfigurable topology design

This section presents the system and circuit models used in reconfigurable $\Delta \Sigma$ modulator topology design. The design methodology is discussed in Section 4.

3.1. Generic reconfigurable topology

As shown in Section 4, reconfigurable $\Delta \Sigma$ modulator topologies are designed starting from a generic topology. The generic topology contains all possible signal paths in the reconfigurable modulator. The generic topology is shown in Figure 1. Blocks $I_1$ to $I_N$ are nonideal integrators.

The state-space description of the generic topology is expressed as equations (1) and (2):

$$
\begin{bmatrix}
Y_1 \\
Y_2 \\
\vdots \\
Y_N \\
N_{11} \\
N_{12} \\
\vdots \\
N_{NN}
\end{bmatrix} =
\begin{bmatrix}
-F_{11} & -F_{12} & \cdots & -F_{1N} \\
F_{21} & -F_{22} & \cdots & -F_{2N} \\
\vdots & \vdots & \ddots & \vdots \\
F_{N1} & F_{N2} & \cdots & -F_{NN}
\end{bmatrix}
\begin{bmatrix}
I_1 \\
I_2 \\
\vdots \\
I_N \\
N_{11} \\
N_{12} \\
\vdots \\
N_{NN}
\end{bmatrix}
$$

(1)

And,

$$
V_i = U_i + N_j
$$

(3)

Where, $U$ and $V$ are the input and output of the modulator, respectively. $Y_i$ is output of $i^{th}$ integrator. $E_q$ is the quantization noise. $a_i$ denotes the path from the feedback DAC to the input of the $i^{th}$ integrator, $b_i$ is the path from the input signal to the input of the $i^{th}$ integrator, and $t_{i,j}$ represents the path from the output of the $i^{th}$ integrator to the input of the $j^{th}$ integrator.

By solving the state-space equations, the transfer function of the modulator is written as (4) [9]:

$$
V = L_0U + L_1V + E
$$

(4)

Variables $L_0$ and $L_1$ are loop filters, which can be symbolically derived from the state-space equations, similar to [7].

The proposed state-space description is different from the one used in [9], in the sense that four kinds of nonidealities are captured: (1) $I$ is the nonideal transfer function for the $i^{th}$ integrator. (2) $N_{i1}, \ldots, N_{iN}$ denote the circuit noise in each integrating stage. (3) $N_j$ accounts for the jitter noise in the feedback DAC. (4) Also, the nonlinearity can be modeled by calculating the transfer function at the harmonics of the input signal. By incorporating nonidealities in the state-space description of the generic topology, their impact on the modulator performance can be derived as closed form expressions, and thus tackled early in the design flow.

We next discuss circuit nonideality modeling.

3.2. Modeling of circuit nonidealities

We grouped the circuit nonidealities into four categories: (1) integrator related, (2) quantizer related, (3) feedback DAC related, and (4) circuit related nonidealities.

1. Integrator related nonidealities

Finite gain and bandwidth was modeled by including finite gain ($A_{hi}$) and poles/zeros ($p_{hi}$, $p_{h2}$, $z_{h1}$) in the transfer
Since the coefficient of jitter noise $n_j$ is $L_1$, which is set by the design parameters (order, OSR, bits, NTFtype) of the modulator. Therefore, the effect of clock jitter cannot be minimized by optimizing the signal paths.

### IV. Circuit related nonidealities

Circuit noise is modeled as white noise, as in equation (1). The noise of all the integrating stages is

$$\tilde{V} = L_0U + L_1\tilde{V} + \sum_{n=1}^{N} \left( \frac{c_n N^N}{L_{1,den}} \times n_{h,n} \right) + E$$

Variable $L_{1,den}$ denotes the denominator of the ideal loop filter function $L_1$, and $c_{n,j}$ is the symbolic coefficient of $n^j$ for stage $n$. Therefore, the following term in the cost function (13) captures the circuit noise

$$h_{m,k} = N \sum_{i=1}^{N} |c_{n,j}| + \sum_{i=1}^{N} |c_{d,j}|$$

Nonlinearity can be modeled by calculating the frequency responses at different harmonic frequencies. The goal is to minimize the variation in $L_1$ in the presence of harmonic distortion. For example, let assume that only the second order nonlinear component ($k_2$) of the first stage is considered. We represented the frequency response at $2f_0$ of the ideal and nonlinear modulator by $L_{1,o2}$ and $L_{1,o2}$, respectively.

$$L_{1,o2} = L_{1,o2,den} + k_2 \left( \sum_{n=1}^{N} c_{n,j} f_0 \right)$$

Hence, the term in the cost function (13) is

4. Methodology for design reconfigurable $\Delta\Sigma$ modulator topology

Reconfiguration of a modulator may occur at three levels: (1) topology reconfiguration, (2) topology parameter reconfiguration, and (3) cell circuitry reconfiguration [4]. The proposed reconfigurable design methodology focuses on the first two reconfiguration levels as well as deriving the design requirements for the cell circuitry reconfiguration. The design goal for the reconfigurable $\Delta\Sigma$ modulators is to (1) minimize the complexity of the reconfigurable topology, (2) increase the robustness of the system with respect to circuitry nonidealities, and (3) minimize total power consumption.

The design flow in shown in Figure 2. It consists of two steps: (1) topology synthesis by NLP solving, and (2) topology refinement by simulation of the detailed modulator model. The steps are discussed next.
4.1. Topology design based on NLP solving

The input to the topology design methodology is a set of M specifications for the M-mode reconfigurable ΔΣ modulator. For each target specifications, such as dynamic range (DR), a set of solutions that can achieve the target DR are found by using the ΔΣ toolbox [10]. Each solution has four parameters: (i) the order of the loop filter, (ii) the over sampling ratio (OSR), (iii) the internal quantizer bits, and (iv) the NTF type. The order of the loop filter ranges from 2 to 5, and OSR is chosen from the set {16, 24, 32, 40, 56, 64, 80, 96, 112, 128} due to the implementation constraints of the decimation filter. Internal quantizer bits range from 1 to 6. In our experiment, only single bit quantizer was considered, due to its inherent linearity and ease of implementation. The NTF type can be Butterworth or inverse Chebyshev. Then, the \( m^M(0 \leq n \leq N) \) solution for the \( m^M(1 \leq m \leq M) \) mode can be written as \( S_{m,n} = (\text{order}, \text{OSR}, \text{bit}, \text{type})_{m,n} \). Theoretically, any solution for a single mode can be combined with the solution for another single mode to build a multimode ADC.

Then, a set of possible candidates for the M-mode reconfigurable ADC are generated by combining M design parameters for each of the M modes, each of which can be written in the form \( S_k = S((m_1,a_1),(m_2,a_2),\ldots,(m_M,a_M)) \). Each candidate can be implemented using different topologies, and optimal topologies are generated by the proposed methodology.

For a given set of parameters \( (\text{order}, \text{OSR}, \text{bit}, \text{type}) \), the corresponding NTF is calculated by the ΔΣ toolbox [10]. Let's assume that the signal transfer function (STF) is unity, and the loop filters \( L_0,d \) and \( L_1,d \) are calculated from STF and STF [9], which are then transformed into the s-domain. Then, the desired continuous-time loop filter functions \( L_{0,c} \) and \( L_{1,c} \) are derived.

Next, symbolic expressions for \( L_{0,c} \) and \( L_{1,c} \) of the loop filter are derived from the state-space equations of the generic topology. By equating the symbolic and numerical coefficients of \( L_{0,c} \) and \( L_{1,c} \), for an M-mode reconfigurable continuous-time ΔΣ modulator, let's suppose that the order of the \( m^M \) mode is \( N_m \), then there are in total \( \sum_{m=1}^{M}N_m+1 \) equations with \( \sum_{m=1}^{M}(N_m+1) \times (N_m+2) \) unknowns. For a cost function \( f \), the reconfigurable topology design problem can be formulated as

minimize cost \( f = f(x_{m,i}, w_{x_{m,i}}); \) subject to: \( g(x_{m,i}) = 0; \) subject to: \( x_{m,i} \geq 0, w_{x_{m,i}} \in \{0,1\}; \)

Where, unknown \( x_{m,i} \) denotes any of the unknown coefficient \( a_i, b_i, \) and \( t_{i,j} \) for the \( m^M \) mode. Unknown \( w_{x_{m,i}} \) denotes whether the signal path with coefficient \( x_{m,i} \) is present or not. \( g \) are the \( \sum_{m=1}^{M}3 \times (N_m+1) \) equality constraints obtained from equating symbolic \( L_{0,c} \) and \( L_{1,c} \) to the desired loop filter functions for all M modes.

Figure 3. Nonideal blocks in Simulink

Table 1. Design specifications

<table>
<thead>
<tr>
<th>Mode</th>
<th>Dynamic Range (bits/dB)</th>
<th>Channel Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>UMTS</td>
<td>11.5/90</td>
<td>1.92MHz</td>
</tr>
<tr>
<td>CDMA2000</td>
<td>15/90</td>
<td>615kHz</td>
</tr>
<tr>
<td>GSM</td>
<td>15/90</td>
<td>190kHz</td>
</tr>
<tr>
<td>EDGE</td>
<td>14/5/97</td>
<td>270kHz</td>
</tr>
</tbody>
</table>

The first two terms represent the topology complexity of the modulator: the first is the absolute complexity (considering the total number of signal paths in the topology) and the second is the relative complexity (accounting for the changes of signal paths when the modulator is reconfigured). \( w_{x_{m,1.i}} \) and \( w_{x_{m,2.j}} \) are the binary value of the corresponding signal paths in the two modes (0 if the path is not present and 1 if the path is present). The second term attempts to maximize the circuit sharing between modes.

The third term minimizes the sensitivity of the modulator with respect to circuitry nonidealities. \( h_{m,k} \) is the function of \( x_{m,1.i} \) that minimizes the impact of nonidealities on NTF. As explained in Section 3, four kinds of nonidealities are formulated in this function. Experiments show that this term is crucial to the performance of the final topologies.

By formulating the topology synthesis problem as MINLP and including the above four nonidealities into the cost function, a set of topologies, (each of which is optimal solution for the particular candidate \( T_k = T((m_1,n_1),(m_2,n_2),\ldots,(m_M,n_M)) \)), are generated.

4.2. Simulation based topology refinement

In this step, the reconfigurable topology is tuned based on more detailed simulation. Hence, only local optimization is conducted. Simulink models showed in Figure 3, are used in this step. First, the modulator is scaled such that the voltage swings at the output of each integrator are within a certain range. Then, all nonidealities discussed in Section 3 are simulated in Simulink.

Power consumption is estimated from two considerations. On one hand, power consumption of each integrating stage is proportional to the unity-gain bandwidth (e.g.
<table>
<thead>
<tr>
<th>Order</th>
<th>GSM-EDGE</th>
<th>CDMA2000</th>
<th>UMTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>48</td>
<td>128</td>
<td>96</td>
</tr>
<tr>
<td>3</td>
<td>48</td>
<td>64</td>
<td>64</td>
</tr>
<tr>
<td>4</td>
<td>40</td>
<td>48</td>
<td>64</td>
</tr>
<tr>
<td>5</td>
<td>28.32</td>
<td>40</td>
<td>48</td>
</tr>
</tbody>
</table>

Table 2. Design parameters

<table>
<thead>
<tr>
<th>complexity</th>
<th>opt1</th>
<th>opt2</th>
<th>opt3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$N_p$</td>
<td>36</td>
<td>17</td>
<td>22</td>
</tr>
<tr>
<td>$N_{pp}$</td>
<td>6</td>
<td>10</td>
<td>11</td>
</tr>
<tr>
<td>$N_r$</td>
<td>11</td>
<td>11</td>
<td>14</td>
</tr>
<tr>
<td>$N_{rr}$</td>
<td>9</td>
<td>9</td>
<td>6</td>
</tr>
<tr>
<td>$N_{p,r}$</td>
<td>11</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>$N_{r,r}$</td>
<td>39</td>
<td>39</td>
<td>33</td>
</tr>
<tr>
<td>$N_c$</td>
<td>12.2%</td>
<td>22.4%</td>
<td>13.3%</td>
</tr>
<tr>
<td>$P$</td>
<td>0%</td>
<td>0%</td>
<td>13.3%</td>
</tr>
</tbody>
</table>

Table 3. Design complexity

$G_m/C_k$ of the integrator. On the other hand, power consumption is proportional to the biasing current of the circuit, which has to be large enough to suppress the nonlinearity of the transconductor into required range. This relationship is analyzed in detail in [11]. As a result, $P \sim (K_01(G_m/C_k), K_{pp}/HD_{3,k})$. The power consumption of the reconfigurable $\Delta\Sigma$ modulator is estimated by the sum of the power consumption of active circuit cells, like transconductors and integrators, for all the modes.

Finally, a set of optimal solutions are generated in terms of topology complexity, robustness, and power consumption. Meanwhile, the design requirement for each building block is also derived.

5. Case study: reconfigurable $\Delta\Sigma$ modulator topology design for multimode communication system

[1] discusses a state-of-the-art multimode continuous-time $\Delta\Sigma$ modulator. Table 1 summarizes the bandwidth and dynamic range specifications for the different modes. We compared the systematically generated topologies with the one in [1]. We noticed that the DR requirement for GSM-mode and EDGE-mode are very close (0.5 bit). We merged the GSM-mode and EDGE-mode into a single mode, considering that different bandwidth requirements can be achieved by modifying the sampling frequency. So, three different DR/BW specifications for the three modes were used as input to the design flow in Figure 2.

Next, the possible design parameters for each mode was produced, as shown in Table 2. The table gives the OSR requirements for different orders of the modulator in order to achieve the DR specification. In total, 60 possible combinations of design parameters were generated for the three modes.

Then, all optimal topologies were found by NLP solving. All the optimal topologies were passed to the next step, where detailed, nonideal models are used. The modulator was simulated and scaled. Finally, several optimal topologies were produced. One of the optimal topologies is shown in Figure 4.

Table 3 presents the comparison between three of the optimal solutions and the topology in [1], as well as a non-reconfigurable topology that includes three single mode modulator. The comparison is in terms of the topology complexity and design effort. Topology opt1 has order 5 for all its three modes, while topology opt2 and opt3 have order <5, 4, 4> and <5, 4, 3> for the three modes, respectively. The complexity of the system is analyzed from number of signal paths ($N_p$), the number of non-reconfigurable cells ($N_{p,r}$), and the number of reconfigurable cells ($N_{r,r}$). It can be seen that reconfigurable ADC are much more compact than the three single mode architecture. Also, the complexity of the produced topology is very similar to the state-of-the-art design in [1].
third order harmonic distortion (HD3) in the first integrating stage. We can see that the generated topology is more robust than a recent state-of-the-art reconfigurable ∆Σ design [1]. Finally, our reconfigurable topologies are more robust to circuit noise and third order harmonic distortion than the reconfigurable ∆Σ design in [1].

6. Conclusion

This paper presents a systematic methodology for designing topologies for reconfigurable continuous-time ∆Σ modulators. To the best of our knowledge, this is the first attempt for systematically designing reconfigurable ∆Σ modulators. The design methodology includes following sequence of steps: system-level design parameter exploration for the multiple design specifications, topology design based on solving nonlinear equations expressing four kinds of circuit nonidealities (finite gain and bandwidth, circuitry noise, distortion and clock jitter) and topology refinement using simulation of more detailed circuit nonidealities, like comparator offset and hysteresis, integrator slew rate and maximum swing limit.

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