Panel

Structured/Platform ASIC Apprentices Which Platform Will Survive Your Board Room?

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Abstract

Moore's law delivers higher performance and lower cost for FPGAs and ASICs alike, but at the 90nm process node and below, design schedules using the traditional cell-based ASIC design methodology hit a wall of uncertainty. At 90nm and below an emerging alternative ASIC design platform is either Platform ASIC or FPGAs. Which way will the cell-based ASIC designer turn for their next design?

Over time, FPGAs and structured/platform ASICs are together poised to replace today's cell-based ASIC market, but which is the real answer to future digital design? Can companies really use these platforms to achieve the system cost reduction and functionality that they need to stay competitive? Which applications will migrate to these platforms the fastest? Is it possible to just tweak the existing cell-based methodology to more efficiently reach the benefits of 90nm process nodes and below? This lively panel will discuss whether it is FPGAs, structured/platform ASICs, or something else that stand to gain the most ground from the projected $25B ASIC market, and why.

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Corporate Position Statements:

LSI Logic, Chris Hamlin -- Moore's Law carries a corollary, which is Compound Complexity. This phenomenon coupled with escalating fixed design costs is forcing reconsideration of some basic assumptions; for ASICs, this means new formal approaches to architecture and abstraction will eventually redefine what it means to 'design' a high complexity device.

Synopsys, Raul Camposano -- ASIC design starts have declined lately and many voices speak of fundamental changes as a result of increasing design costs, predicting even the extinction of ASIC design altogether. ASICs and ASSPs have been a formidable economic force, accounting for over one third of the semiconductor market. Standard cell based designs have also been the major consumer of EDA tools and design technology. However, raising NRE costs which stand at more than $10M to design an ASIC at the 90nm technology node, the cost of respins, the lack of flexibility (compared to programmable solutions) and the increasing time to market have prompted the search for other design styles. These include structured ASICs, FPGAs, processor arrays and "platforms", which are all trying to fill the void left by the slowing of ASIC design starts. The reality however is that all these alternatives remain niche players, because they are either a poor economic choice or because their performance constraints the application space. Rather than replacing ASIC designs, the data suggests instead that these alternative solutions are reviving cell-based design by adding flexibility to traditional ASIC design in the form of embedded programmable blocks.

Synplicity, Ken McElvain -- Much has been said recently about the decline of ASIC design starts sighting rising costs and the indeterminate timing for completion. However, less is said about

the change that's been underway where product development teams are finding new ways to overcome these cost and time to market issues associated with traditional standard-cell ASIC design. Today's ASIC design market is alive and well, it's just changing over to FPGAs and Structured ASICs whose design platforms are reinvigorating ASIC design.

Tensilica, Steve Leibson -- Moore's Law has exerted a powerful forcing function that has transformed IC design methodologies for nearly 40 years and will continue to do so. This irresistible driver has forced IC designers to successively abandon Rubylith, Mylar, and X-acto knives; Calma, Applicon, and ComputerVision computer-aided drafting systems; and schematic-based design systems once offered by Daisy, Mentor, and Valid. All of these design tools were abandoned when IC-fabrication abilities inevitably outstripped the abilities of the then-current design methodology to express achievable IC design complexity in a manner that fit within the limitations of human brain capacity. The industry is at this inflection point once more with cell-based IC design, RTL representations, and mega-gate ICs. Rising chip complexity has once again forced design teams to move up a level of abstraction. Designers now employ high-level languages such as C, C++, and Matlab to express system and algorithmic behaviors and then manually translate these descriptions into RTL. It's the slow, costly, error-prone process of manual translation into RTL that's got to go—to be replaced with fast, reliable, automated ways of transforming high-level system and algorithmic descriptions into hardware. This evolution of design methodology is orthogonal to the implementation fabric; it is feasible across the full range of IC design from FPGAs, through structured ASICs, standard-cell ASICs, and all the way to custom ASSPs. Developing implementation fabrics that lower NRE costs is nice, but just lowering NRE costs without addressing the design productivity and risk issues is like having the Internet without developing the World Wide Web.

Toshiba America, Rich Tobias -- Cell-based custom SoCs will enable scores of very high-volume new products in the next few years and is far from a tired technology. Our customers continue to see a big return from their investment in cell-based SoCs in 90nm and beyond. Many of them have considered structured arrays as a way to reduce costs, but feel the compromise is too much. They are not willing to give up the differentiation a cell-based SoC affords them in performance, complexity, mixed-signal capability and low unit cost. Instead, they are asking us to help improve their profitability by making cell-based SoCs less expensive. The Toshiba SoCMosaic(TM) custom chip program saves our customers millions of dollars in development costs for IP-rich designs by using soft IP platforms to reduce front-end design time down to a few months, and by running the customer's software on an FPGA emulation of the design before tape-out to reduce re-spin risk.

Xilinx, Ivo Bolson -- Due to the challenges imposed by designing and manufacturing deep submicron chips, today, people would have to invent FPGAs if they didn't already exist. FPGAs are implementing all rules of best practice to benefit from Moore's Law. Alternative approaches such as structured ASICs are introducing many new problems ranging from inventory management to tool support. But, if you are not part of the solution you can still make money by extending the problem.