Variation-Tolerant Circuits: Circuit Solutions and Techniques

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ABSTRACT
Die-to-die and within-die variations impact the frequency and power of fabricated dies, affecting functionality, performance, and revenue. Variation-tolerant circuits and post-silicon tuning techniques are important for minimizing the impacts of these variations. This paper describes several circuit techniques that can be employed to ensure efficient circuit operation in the presence of ever-increasing variations.

Categories and Subject Descriptors
B.7.1 [**Integrated Circuits**]: Hardware – *Types and design styles*.

General Terms: Design, Reliability, Performance

Keywords: Parameter variation, high-performance design, body bias.

1. INTRODUCTION
Process variations are expected to worsen in future technology generations due to difficulties with printing nanometer-scale geometries using standard lithography [1]. A major source of variation in CMOS circuits is due to variation in the channel length of the devices, although other factors such as dopant fluctuation and non-uniformity in etching and polishing of interconnect layers also play an important role. These variations include die-to-die as well as within-die components, and impact the maximum clock frequency (Fmax) and leakage of microprocessor dies. For some variation-sensitive circuits, such as SRAM arrays and dynamic logic, process variations can result in functionality issues and yield loss.

In addition to process variations – which are mainly static – circuits also need to operate correctly under dynamic fluctuations of supply voltage, temperature, and noise [2]. As processor power consumption and frequency continue to rise, it is becoming increasingly difficult to deliver the required power with minimum voltage transients. These voltage transients, which occur when there is a step change in the current demand for the processor, reduce the effective supply voltage, and hence, the processor Fmax. This effect has typically been mitigated by a combination of circuit techniques (e.g., decoupling capacitors), architectural techniques (e.g., staged clock gating) and simple margining of the frequency. Similarly, microprocessors can experience a wide range of operating temperatures, but must be designed to operate correctly under the worst-case condition. If the frequency is set by the worst-case temperature, the processor is operating sub-optimally whenever the temperature is lower.

As both static and dynamic variations increase, techniques are necessary at the system, architecture, and circuit level to reduce the impact of these variations while providing the highest performance for the given power constraints. This paper gives an overview of the effect of variations, and then describes several circuit techniques that can be applied post-silicon for variation tolerance.

2. VARIATION TRENDS
Functionality, Fmax, and power consumption of individual dies are influenced by both die-to-die (D2D) and within-die (WID) variation components. The impact of within-die variation, which causes differences in path delays fabricated on the same die, is heavily influenced by circuit optimization decisions such as transistor sizing, threshold voltage assignment, and number of critical paths in the design. Figure 1 shows that as the number of independent critical paths increases, the mean of the maximum critical path delay (which corresponds to the Fmax) increases as well. The magnitude of the WID variation also depends on critical path depth, where paths with fewer logic stages experience less averaging of random variations resulting in larger variability. Due to increasing complexity and performance requirements for microprocessor designs, the number of critical paths increases with each generation while the logic depth typically decreases. Both trends worsen the impact of within-die variations.

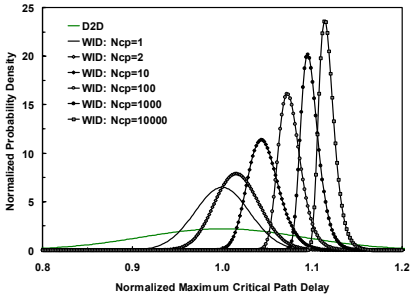

Figure 1. Impact of within-die variations on product performance, as a function of the number of statistically-independent critical paths (N_{CP}).

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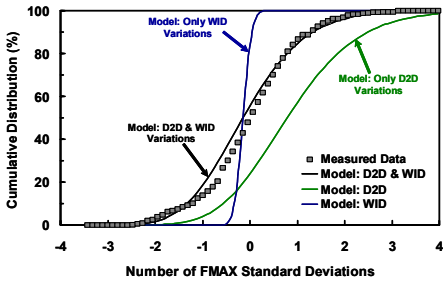

Figure 2. Individual contributions of D2D and WID variations.

Figure 2 demonstrates the interaction between die-to-die and within-die variation components. The variance of the combined distribution is determined mainly by the die-to-die component, while the mean Fmax is primarily a function of within-die variations. These variations combine to affect the frequency and power distributions for the fabricated dies, and therefore both are important to consider when optimizing a design for performance, power, and revenue. Typically, these variations are handled by a combination of design margining (which can lead to a worst-case design which operates inefficiently under normal conditions) and frequency binning (which impacts revenue and yield). When frequency binning is done, dies with a slow Fmax are either discarded or sold at a reduced price, while dies with excessive leakage or total power will violate the system power specification and must be discarded. Thus, the amount of process variations directly impacts the revenue.

3. CIRCUIT TECHNIQUES

One useful technique for reducing the impact of these variations at the circuit level is substrate or body biasing, where a non-zero voltage is applied between the body and source of a transistor. Depending on the voltage applied, the threshold voltage is either increased (which reduces the leakage) or reduced (which increases the Fmax). Thus, adaptive body bias (ABB) can be used after fabrication to compensate for the effects of process variations – each die receives a unique bias voltage which maximizes the frequency of that die subject to power constraints. Figure 3 shows the native leakage vs. Fmax distribution as well as the resulting distribution after ABB is applied. ABB reduces the sigma of the frequency variation by 6X and moves over 30% of the dies into the highest frequency bin.

ABB is effective at compensating for die-to-die variations, but within-die variations cannot be handled using only a single bias value per die. Instead, the die can be divided into multiple regions, each of which can potentially receive a different body bias voltage after fabrication. Figure 3 shows that this within-die ABB technique further reduces the frequency variation and moves 97% of the dies into the highest bin.

It is possible to use supply voltage as a method of reducing the impacts of process variations as well. Both switching and leakage power have a super-linear dependence on supply voltage; therefore, total power and frequency can be modulated by choosing the optimum supply voltage. Figure 4 demonstrates the binning improvement possible with an adaptive V_{DD} technique, where the number of dies in the top two frequency bins improves by 45%. Since switching power and leakage power respond differently to supply voltage and threshold voltage, the combination of ABB and adaptive V_{DD} is more beneficial. As process variations become more important, circuit designers will likely include additional circuit features which may be tuned post-silicon for variation tolerance.

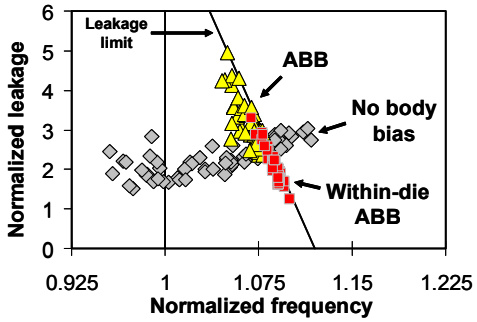

Figure 3. Leakage vs. Fmax distribution for dies without body bias, ABB, and with WID-ABB.

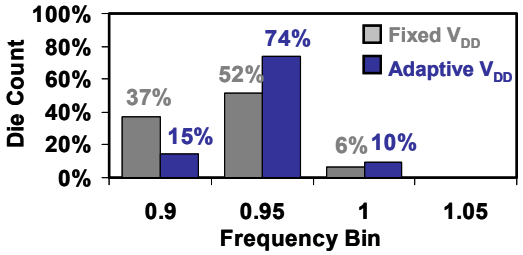

Figure 4. Binning improvement for adaptive V_{DD}.

4. CONCLUSION

Circuit design techniques that account for variation effects will increasingly become important as variations worsen. Optimizations at different levels of the design – system, architecture, and circuits – provide opportunities to reduce the impact of these variations. At the circuit level, adaptive body bias and adaptive supply voltage techniques have been shown to reduce the variation in frequency of fabricated dies, improving the mean frequency and number of dies in the highest bin.

5. REFERENCES

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