Is Methodology the Highway Out of Verification Hell?

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PANEL SUMMARY

Few would disagree that verification takes the lion's share of today's project resources. If we examine the available research, we quickly discover that verification is a significant pain point that consumes massive amounts of time and resources across a multitude of market segments. Per Gary Smith at Gartner Dataquest, verification consumes 30% to 70% of total schedule, depending on design size. According to Collett International Research, Inc., a majority of ASICs and integrated circuits (ICs) require at least one respin with 71% of respins are due to functional bugs "verification should have caught".

With such statistics, it is easy to understand why many contend that the verification challenge is growing at a double exponential rate (that is, exponential with respect to Moore's law). Given verification's importance and its significant impact on fundamental design quality and time-to-market demands, what is our industry doing in response? This panel explores where the methodology highway is taking us - is the destination heaven or just another level of Dante's inferno?

Respected authors and experts in verification methodology will share their insights and opinions of the two methodologies used today: verify-after-the-fact (traditional) and verify-as-you-design (emerging). For decades, simulation has necessitated a verify-after-the-fact methodology and yet we can see from the industry research that a high percentage of silicon requires respins. With the latest advances in simulation testbenches and languages, can the verify-after-the-fact approach scale? Or, is it time for a move to a higher level of abstraction that enables a verify-as-you-design methodology?

Industry leading chip and systems companies will discuss the methodologies they employ today to address the enormous challenge of functional verification. Questions to be addressed by our esteemed panelists include: How can we bring in schedules? What can we do to increase design quality? What cultural and organizational changes have to take place to bring quality back to the forefront of design? Where is the measurable proof of quality? What are the questions that managers should be asking themselves? What are the engines being used? What formal techniques deliver the greatest success? How important is HW/SW verification? What are the processes or methodologies being used to overcome tool or technology limitations? What is the value of assertions? How does a geographically dispersed engineering team impact design quality? What are the metrics being used to measure progress and success? And how do you know when you are done?

Today we currently don't design quality in – we TEST it in (using simulation). But, what would happen if quality was designed in from the beginning? How much could we improve the overall quality level and reduce verification time, and what would this take to do it? Finally, can migration to a new methodology be the highway out of verification hell?

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B 5.2 Design aids
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1. PANELISTS VIEWPOINTS

Harry Foster, Jasper Design Automation

Imagine a time 30 or 40 years ago, when the primary means of ensuring quality in the automobile manufacturing world was to inspect quality in. Over time, we've learned that inspection for the purpose of identifying defects is costly, unreliable, and ineffective. In the world of design verification, we are now at a juncture where existing verification methods that depend on inspection after-the-fact suffer the same inherent problems that plagued the automobile industry years ago. It is time for a new way of thinking that involves designing quality in from the start and incrementally proving that design blocks meet 100% actual

coverage prior to integration. Some people contend that new languages, such as SystemVerilog, with its integrated testbench capabilities will lead us to new methodologies that will chart a course out of verification hell. Others claim that only methodologies that use functional coverage models and assertion-based Languages, such as PSL, are the road to success. However, I contend that these techniques just patch simulation pot-holes in what is already an inherently flawed and incomplete approach to verification. Today, there is a better way that is based on formal verification of high-level requirements.

Janick Bergeron, Synopsys
Verifying complex IC designs without a coherent methodology is like driving down a busy icy highway without driver training or any rules of the road – out of control with a good chance of crashing or not reaching the destination. A good verification methodology will help new engineers get things done right the first time, avoiding the mistakes of their predecessors, provide insight and predictability to the verification process, scale with complex designs, enable verification to start and finish sooner, and improve productivity by enabling a high degree of reuse both within project and between projects. A complete methodology will also be supported by a comprehensive set of pre-written, proven verification building blocks and interoperable VIP to speed creation of a solid environment. In the end, a good methodology will help engineers escape "verification hell" by finding more bugs, with fewer resources and less time.

Masayuki Nakamura, Sony Corporation
In order to keep our quality on consumer electronic devices, we rely heavily on design verification to achieve market success. Within the consumer electronics space, the fast moving nature and short market windows lead to frequent and last-minute specification changes, which must be accommodated in our verification methodology. In addition, we often reuse IP in many different devices, so that IP needs to be verified with 100% coverage under all possible usage contexts. In order to meet these tight schedule constraints and meet our quality goals, we need a single language which can describe the executable specification that works with all of our methods. Our methods include a combination of formal verification, assertions in the simulation, acceleration and FPGA prototyping. By achieving this, we are able to reuse the designs and verification IP across the many devices we produce quickly, while achieving the highest possible quality.

Shrenik Mehta, Sun Microsystems
Industry standards and true interoperability are powerful enablers of verification methodologies. Methodology cuts down cost in major verification components, but it does not eliminate them completely. Some core issues lying at the heart of verification cannot be dealt with by methodologies alone and must be solved by an apt mentality from the very beginning of design combined with a technology breakthrough. Methodology will not take verification out of hell to heaven, maybe to purgatory. But it is on the way out.

Laurent Ducousso, ST Microelectronics
It can definitely be "Hell" to verify 33 IP blocks for 7 SoCs within a year, especially when answering to new releases that have 96 engineering changes due to undetected bugs before delivery, pushing the committed date by 40% due to this unforeseen workload. Verification's root cause of reported bugs is equally spread within specification issues, testplan holes and the lack of randomization on the existing test. Fundamentals that may drastically change the situation for the better include moving to a higher level of abstraction for design capture, increasing the usage of pre-verified hardware (such as cores) and verification-skilled resources when new hardware is required. By relying upon a strong partnership with the internal R&D group and the CAD vendors, pilot projects are on-going on high-level synthesis, embedded cores architectures, verification speed and quality recovery. The outcome of these efforts will translate into the necessary joint involvement of architects, designers and verifiers around a common methodology for bug hunting. Formal methods are used less and less in our project's flow, due to the increased size of verified IP compared to the formal tool's capacity - payback is decreasing. Solving the tool's capacity, coverage versus simulation, as well as formal techniques to compare behavioral C specification against synthesized RTL, are open door's to significant flow improvement for both IP quality and schedule.

2. SEEKING VERIFICATION HEAVEN

In the face of shrinking market windows, ever-changing product specifications and increasing demands for greater performance and functionality, can today's leading electronics company, with help from the EDA industry, address the need for quality designs in a predictable schedule?

Getting to heaven requires significant effort, and in the case of verification, this means changing what we have been doing - from policing quality in, to building it in.

Centralizing around the theme of a methodology aimed at improving design quality and predictable schedules (such as advanced formal methods that operate at a higher level of abstraction for "verify-as-you-design" success) panelists will examine and discuss their individual viewpoints and various unique approaches out of verification hell and toward the ultimate "heaven", 100% full verification.