Wireless Platforms: GOPS for Cents and MilliWatts

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PANEL SUMMARY

In recent years, data communication has overtaken voice as the main force behind the growth in wireless. With this has come a proliferation of standards ranging from wide area networks at one end of the spectrum to personal area networks on the other end. The opportunities offered by this truly ubiquitous connectivity are tremendous, and are leading to revolutionary chances in the way computer, communication, and consumer systems operate and interact.

Providing the necessary flexibility to seamlessly interact with the multitude of emerging network models, as well as the muscle to support the demanding multimedia functionality in a mobile environment, presents some huge challenges to the developer of the wireless implementation platforms. The power budget of the mobile terminal is typically fixed by size considerations and operation time. Cost considerations further constrain the solution space.

In response to these challenges, many solutions have been floated and experimented with ranging from multi-processor architectures, advanced DSPs, reconfigurable solutions and hardwired accelerators. While these innovations break new ground in the world of embedded architectures, many questions emerge such as efficiency, flexibility and programming model.

This panel will presents a "bake-off" between a number of solutions that have emerged over the recent years.

Categories and Subject Descriptors

C.3 Special purpose and application based systems

Keywords

Wireless architectures, data communications, implementation platforms

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1. PANELISTS VIEWPOINTS

Allan Cox, 3Plus1 Technology, Inc.

Implementing new voice, video and data functions in next generation systems, requires large increases in computational "horsepower". However, mass consumption of mobile systems that include such functions depends on delivering this added horsepower, on a programmable platform, at no additional cost and with such efficiency that reduced power consumption extends battery life beyond today's limits. Performance saturation of conventional computing architectures and their associated power inefficiencies have driven multiprocessor architectures that can achieve these compute demands through concurrent operation. High efficiencies can be achievable by implementation of heterogeneous multiprocessor architectures whose structures reflect the application characteristics and optimize for low area and power. Hierarchical scaling of compute element, processor, micro-interconnect and macro-interconnect are critical factors for success. Finally the smooth integration of a single programming model software scheme, within the hardware architecture can be made, such that familiar programming tools and techniques are reusable by the applications community

Frank Lane, Flarion Technolgies, Inc.

We are still in the infancy of broadband wireless access, and as such, we are seeing developments in algorithms, protocols, and standards evolve faster than hardware design cycles. For infrastructure, which typically have a multi-year product lifetime, the only alternative is to move to a reconfigurable platform. Such a platform, comprised of multiple processors, reconfigurable logic, and flexible interconnect, and the distributed processing which operate on it, provide a significant challenge to design, development, and verification.

Rudi Lauwereins, IMEC

Ubiquitous communication requires on the same device the presence of multiple wireless modems, each supporting multiple modes, e.g. GSM (900 MHz, 1800 MHz, 1900 MHz), GPRS, Edge, UMTS, WiFi 802.11a/b/g (64QAM, 16QAm, QPSK, BPSK), DVB-H, WiMax 802.16a/d/e, Bluetooth, etc. Cost, however, may not increase substantially above the cost of implementing a single modem, especially for consumer devices.

Reconfigurable architectures that are just-flexible-enough to implement all wireless modes offer a good compromise between low cost, short time-to-market and low power consumption. For the front end, this requires innovative RF architectures, making use of novel RF-MEMS devices, with a growing importance of digital calibration and compensation. For the baseband part, compiler-friendly VLIW processors with tightly coupled coarse grain reconfigurable arrays provide a promising solution. The flexibility offered by both solutions facilitates cross layer management of parameters across the complete terminal, bridging the gap between communication and application.

Ulrich Ramacher, Infineon Technologies AG
Multiband multistandard radios don't lack an application scenario, but a systematic approach to design space exploration and architecture development. The latter depends heaviliy on the number and weight of the design criteria: area, power consumption (active, stand-by, leaky), performance, flexibility, simplicity of programming model. Every company seems to enter the design space at a preferred point in the close neighborhood of which the final architecture will materialize. Instead, separate modeling of function and application, on the one hand, and architecture, on the other hand, is recommended. Design space exploration we perform, on the one side, by means of statistics of functions and connections, and, on the other side, via cost functions for HW/SW architectural elements. This way, we arrive at a multi-processor architecture the instruction sets of which use general-purpose as well as application-specific instructions. For the next-but-one generation of smart phones, we foresee a processor core common to baseband and multimedia processing, with separate instruction extensions for baseband and multimedia.

David Witt, Texas Instruments
The next couple of years will see a substantial increase in the requirements for handset computing resources, specifically relative to audio/video compression/decompression and 3D graphics. In parallel we will see a requirement for multiple different radio protocols and modulation techniques to be handled seamlessly on the same handset. Cost and power will drive these requirements to advanced process technology, and integration, of the application processor, modem, and CMOS RF onto a single chip. Enabling this hardware in increasingly leaky process nodes at 65nm and 45nm represents extremely difficult software/system/IC development tradeoffs. This large handset development cost will likely provide a very high barrier of entry to companies attempting to compete in this space in the near future, especially those providing fractions of the total handset solutions today.

2. UBIQUITOUS CONNECTIVITY – THE PROMISE LAND

Since Mark Weiser launched the term ubiquitous computing a couple of decades ago, ubiquitous wireless connectivity has become the holy grail. Rapid developments in all areas of wireless have put this formerly lofty goal within reach.

Portable mobile communication and multimedia platforms are displacing the Personal Computer (PC) as the premier technology driver, and as a result, are profoundly changing the way we conceive computational and architect computational platforms. This panel will hence shed an illuminating light on what the future has in store for us.