Minimizing Peak Current via Opposite-Phase Clock Tree

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ABSTRACT

Although a lot of research efforts have been made in the minimization of the total power consumption caused by the clock tree, no attention has been paid to the minimization of the peak current caused by the clock tree. In this paper, we propose an opposite-phase scheme for peak current reduction. Our basic idea is to divide the clock buffers at each level of the clock tree into two sets: an half of clock buffers operate at the same phase of the clock source, and another half of clock buffers operate at the opposite phase of the clock source. Consequently, our approach can reduce the peak current of the clock tree nearly 50%. Experimental data consistently show that our approach works well in practice.

Categories and Subject Descriptors

B.7.2 [**Integrated Circuits**]: Design Aids – *Layout*, *Placement and routing*.

General Terms

Design, Reliability.

Keywords

Physical design, Clock network synthesis, Low power.

1. INTRODUCTION

In a modern VLSI circuit, the most common strategy for clock distribution is to insert a large number of buffers along the paths from clock source to flip-flops, forming a buffered-tree structure. Each transition of the clock signal changes the state of each capacitive node within the clock tree, in contrast with the switching activity in combinational block, where the change of logic states is dependent on the logic function. Therefore, the clock tree is one major source of power dissipation in a modern VLSI circuit. A lot of research efforts [1-4] have been made in the minimization of the total power consumption caused by the clock tree.

As the progress of deep sub-micron process technology, the power supply level fluctuation is exacerbated since the noise margin is considerably reduced. As a result, the control of power supply noise becomes very critical in determining the circuit performance and reliability. Thus, in addition to minimize the total power consumption, there is a demand to reduce the peak power (current). Moreover, if the peak current can be reduced, the wiring areas of power and ground distribution networks and the total number of power pads also can be saved.

Previous work [5,6] ever utilized the clock skews to reduce the peak current caused by the computations. However, they [5,6] do not attempt to minimize the peak current caused by the clock tree. To the best of our knowledge, no attention has been paid to the minimization of the peak current caused by the clock tree. In this paper, we present an opposite-phase scheme to reduce the peak current caused by the clock tree. Our basic idea is to divide the clock buffers at each level of the clock tree into two sets; thus, in each clock transition, we always have that one half of capacitance nodes in the clock tree is charging and the other one half of capacitance nodes in the clock tree is discharging. Consequently, the peak current of the clock tree can be reduced nearly 50%. Moreover, from the viewpoint of practical implementation, our approach has the following four features.

(1) Our approach can significantly reduce the peak current of the clock tree without any penalty on clock cycle time and total power consumption.
(2) Our approach can be easily implemented at the clock tree synthesis stage in the existing design flow.
(3) Our approach can be combined with the approaches [1-4] that attempt to minimize the total power consumption within the clock tree.
(4) Our approach can be combined with the approaches [5,6] that attempt to exploit the clock skews to reduce the peak current caused by the computations.

2. THE OBSERVATION

A clock tree can be implemented using clock buffers or clock inverters. Without loss of generality, here, we use a clock buffer to demonstrate our observation on peak current.

In general, a clock buffer is composed of two concatenated inverters. Using the clock buffer shown in Figure 1 (a) as an example, Figure 1 (b) and Figure 1 (c) give the block diagram and the circuit diagram, respectively. For a clock buffer, there are two types of clock transitions: *rising transitions*, i.e., the logic level of the input pin A changes from 0 to 1; and *falling transitions*, i.e., the logic level of the input pin A changes from 1 to 0. In a clock tree structure, the output pin Y of the clock buffer often drives many fan-outs with very long wiring length. Thus, the capacitance in node Y is much larger than the capacitance in node C.

Figure 2 (a) gives our analysis of the peak current caused by a clock rising transition. Since the logic level of the input pin A rises from 0 to 1, the PMOS P_1 switches off and the NMOS N_1 switches on. The capacitance in node C is discharged. A current I_1

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flows from the node C to the ground line V_{SS}. In the next stage, PMOS P_2 switches on and NMOS N_2 switches off. The capacitance in node Y is charged. A current I_2 flows from the power line V_{DD} to node Y. Since the capacitance in node Y is much larger than the capacitance in node C, the current I_2 (charging) is much larger than the current I_1 (discharging). Therefore, in each clock rising transition, the charging of large output capacitance in node Y leads to a peak current in the power line V_{DD}.

Figure 2 (b) gives our analysis of the peak current caused by a clock falling transition. Since the logic level of the input pin A changes from 1 to 0, the PMOS P_1 switches on and the NMOS N_1 switches off. Therefore, the capacitance in node C is charged. A current I_1' flows from the power line V_{DD} to the node C. Then, the PMOS P_2 switches off and the NMOS N_2 switches on. Therefore, the capacitance in node Y is discharged. A current I_2' flows from the node Y to the ground line V_{SS}. Since the capacitance in node Y is much larger than the capacitance in node C, the current I_2' (discharging) is much larger than the current I_1' (charging). Therefore, in each clock falling transition, the discharging of large output capacitance in node Y leads to a peak current in the ground line V_{SS}.

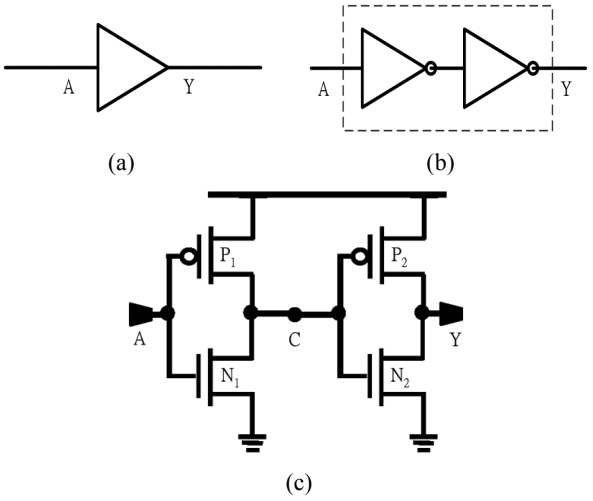

Figure 1. Clock buffer.

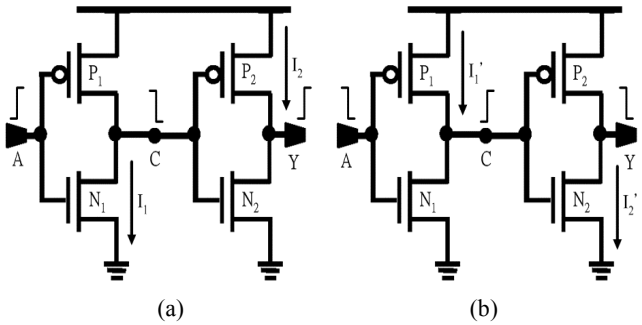

Figure 2. Analysis of the peak currents.

Based on these analyses, we have the following expectation. In the clock rising transition (in the clock falling transition), the peak current occurs in the power line V_{DD} (in the ground line V_{SS}) due to charging (discharging) the output capacitance. We perform an experiment to verify our expectation. The cell CLKBUFX4 in TSMC 0.18μm cell library is used as the clock buffer. We assume that clock transition time is 0.1 ns and the capacitance of node Y is 0.052 pf. Figure 3 gives the HSPICE simulation results. Note that the HSPICE simulation results include the short-circuit currents; however, the short-circuit current is much smaller than the current used to charge (discharge) the output capacitance. The notation $I(V_{DD})$ denotes the current flows from the power line V_{DD} to the capacitance node (for the purpose of charging). The notation $I(V_{SS})$ denotes the current flows from the capacitance node into the ground line V_{SS} (for the purpose of discharging). The HSPICE simulation results provide the following two observations.

(1) In the clock rising transition, the maximum current of $I(V_{DD})$ is 740.1 μA, while the maximum current of $I(V_{SS})$ is 240.0 μA. Therefore, the peak current occurs in the power line V_{DD}.

(2) In the clock falling transition, the maximum current of $I(V_{DD})$ is 179.8 μA, while the maximum current of $I(V_{SS})$ is 686.7 μA. Therefore, the peak current occurs in the ground line V_{SS}.

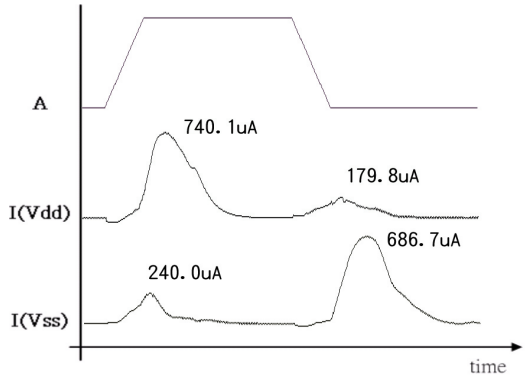

Figure 3. HSPICE simulation results of the clock buffer.

Clearly, the HSPICE simulation results are consistent with our expectation. Furthermore, with the progress of deep sub-micron process technology, the clock transition time gets smaller (due to high clock frequency) and the output capacitance gets higher (due to highly-complex design and highly-coupled interconnection). As a result, the current caused by charging (discharging) the capacitance in node Y becomes much larger and larger than the current caused by discharging (charging) the capacitance in node C.

3. A MOTIVATIONAL EXAMPLE

Let's consider the two-level binary clock tree as shown in Figure 4. As discussed in Section 2, in each clock rising transition, the peak current flow from the power line V_{DD} to charge the capacitance nodes; in each clock falling transition, the peak current flow from the capacitance nodes into the ground line V_{SS}.

Our basic idea is to divide the clock tree into two equal-sized sub-trees: a *positive tree* T_P and a *negative tree* T_N. The new two-level binary tree is implemented as shown in Figure 5. We use the clock buffer as the root of the positive tree T_P and use the clock inverter as the root of the negative tree T_N. Thus, the positive tree operates at the same phase of the clock source, while the negative tree operates at the opposite phase of the clock source. Note that all the flip-flops driven by the positive (negative) tree should be positive-edge-triggered (negative-edge-triggered).

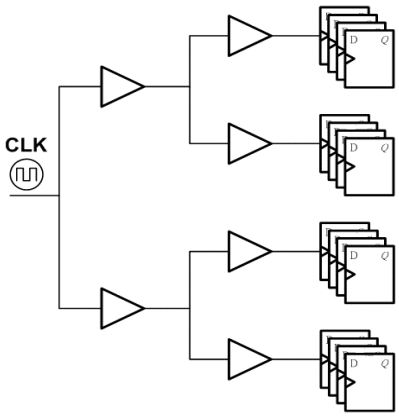

Figure 4. Two-level binary clock tree.

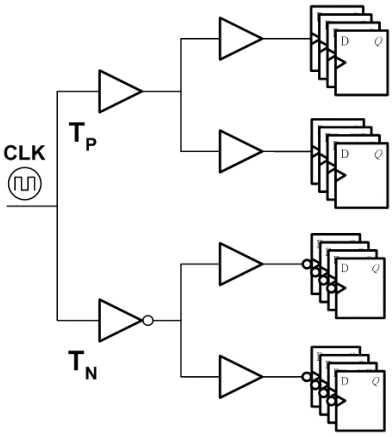

Figure 5. Our approach (using opposite phases).

The main advantage of our approach is that it balances the charging activities and discharging activities at each level of the clock tree. When the clock source has a rising transition, the peak current of the positive tree is in the power line V_{DD} due to the charging of capacitance nodes (in the positive tree), while the peak current of the negative tree is in ground line V_{SS} due to the discharging of capacitance nodes (in the negative tree) at the same time. On the other hand, when the clock source has a falling transition, the peak current of the positive tree is in ground line V_{SS} due to the discharging of capacitance nodes (in the positive tree), while the peak current of the negative tree is in the power line V_{DD} due to the charging of capacitance nodes (in the negative tree).

It is noteworthy to mention that our approach is practical. Most cell libraries provide both positive-edge-triggered and negative-edge-triggered flip-flops. Even though a cell library does not provide negative-edge-triggered flip-flops, it is very easy for us to design negative-edge-triggered flip-flops according to positive-edge-triggered flip-flops. Let's use the typical schematic of D-type flip-flop shown in Figure 6 as an example. For a positive edge-triggered D-type flip-flop, the pin C1 is connected to the clock and the pin C2 is connected to the complement of the clock; on the other hand, for a negative-edge-triggered D-type flip-flop, the pin C2 is connected to the clock and the pin C1 is connected to the complement of the clock. In other words, both the positive-edge-triggered D-type flip-flop and the negative-edge-triggered D-type flip-flop are implemented in the same circuit structure except for the opposite clocking schemes. As a result, their delay models and their power consumptions are very similar. Therefore, the clock tree shown in Figure 4 and the clock tree shown in Figure 5 have similar clock latencies and similar total power consumptions.

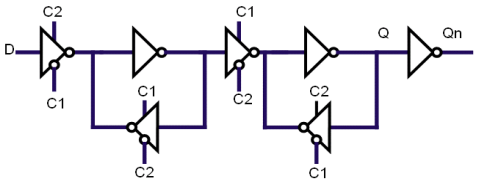

Figure 6. D-type Flip-flop.

4. THE DESIGN METHODOLOGY

The proposed design methodology is depicted in Figure 7. The details are elaborated as below. First, we assume that each flip-flop is positive-edge-triggered to perform the logic synthesis. After the logic synthesis is finished, we obtain a pre-layout gate-level netlist. Then, we partition all the flip-flops into the following two groups: one group is driven by the positive tree and the other group is driven by the negative tree. Here we try to equalize the number of flip-flops in each group. After the partitioning is finished, we replace the flip-flops in the group that are driven by the negative tree with the same type negative-edge-triggered flip-flops. Then, we use the clock tree synthesis feature provided by the automatic placement and routing tool to implement the two sub-trees: the positive tree and the negative tree. Note that the two sub-trees are implemented separately but under the same clock tree synthesis constraints. Finally, we can further adjust the timing of each sub-tree using the features provided by the automatic placement and routing tool. As a result, the wiring areas of power and ground distribution networks and the total number of power pads can be saved since the peak current is reduced.

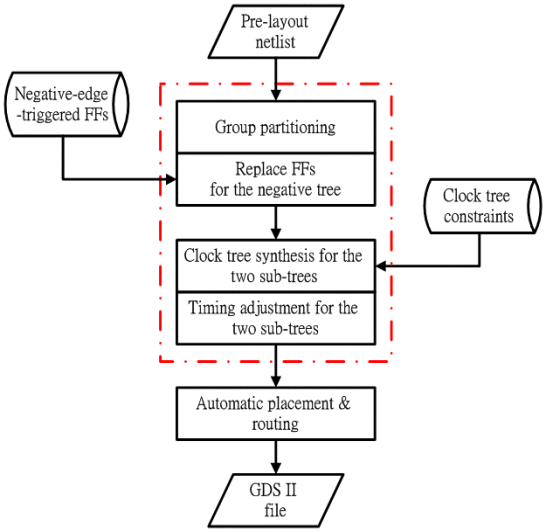

Figure 7. The proposed design methodology.

5. EXPERIMENTAL RESULTS

We use seven large circuits, including S13207, S15850, S35932, S38417, S38584, W-Band and Athena, to test the effectiveness of our approach. The circuits S13207, S15850, S35932, S38417 and S38584 are adopted from the ISCAS'89 benchmark suite and implemented by TSMC 0.18 µm cell library. The circuit W-Band is a wideband communication chip (used in the ADSL application) and implemented by TSMC 0.18 µm cell library. The circuit Athena is a 3-G application chip and implemented by TSMC 0.25

μm cell library. It is noteworthy to mention that the circuit W-Band and the circuit Athena are real industry circuits.

Table 1 tabulates the characteristics of these seven circuits. The column *Gates* gives the number of gates. The column *FFs* gives the number of flip-flops. The column *Clock Period* gives the clock period in nano-seconds (ns). The column *Tree Structure* gives the structure of clock tree, including the number of levels (denoted as *Levels*) and the number of buffers (denotes as *Bufs*). For each circuit, the constraint on the clock skew is 0.1 ns.

Table 1. Characteristics of test circuits.

Circuit	Gates	FFs	Clock Period(ns)	Tree Structure	
				Levels	Bufs
S13207	8630	669	15.0	4	10
S15850	10381	597	15.0	6	12
S35932	17832	1728	15.0	4	22
S38417	23835	1636	15.0	4	20
S38584	20722	1452	15.0	2	17
W-Band	5648	688	15.0	2	7
Athena	230520	26729	8.9	22	5147

For the purpose of comparisons, we also implement the corresponding single-phase clock tree, which only drives positive-edge-triggered flip-flops. Table 2 tabulates the comparisons between the proposed clock tree structures and the single-phase clock trees structures. We use Synopsys Powermill to perform circuit level power simulation. In addition to compare the peak currents, we also compare the RMS currents. The column *Single* gives the simulation results of single-phase clock tree structure. The column *Ours* gives the simulation results of the proposed clock tree structure. The column *Imp%* gives the relative improvement of the proposed clock tree structure over the single-phase clock tree structure, i.e., 100%-Ours/Single. Note that, in the circuit Athena, to preserve the logic hierarchy, we do not equalize the number of flip-flops in the two sub-trees. In this circuit, the positive tree has 16234 positive-edge-triggered flip-flops and the negative tree has 10495 negative-edge-triggered flip-flops.

Table 2. Experimental results.

Circuit	Peak Current			RMS Current		
	Single	**Ours**	Imp %	Single	**Ours**	Imp %
S13207	44.9	24.9	44.5	3.6	2.9	19.4
S15850	37.0	24.1	34.9	3.1	2.6	16.1
S35932	124.1	66.0	46.8	10.0	7.6	24.0
S38417	111.0	63.3	43.0	8.9	7.2	19.1
S38584	105.0	49.5	52.9	8.5	6.0	29.4
W-Band	44.3	23.8	46.3	9.1	5.4	40.7
Athena	2881	2066	28.3	635	541	14.8

Experimental results consistently show that our approach can significantly reduce the peak current. Using the proposed clock tree structure, the average peak current reduction achieves 42%. Moreover, experimental results also consistently show that our approach can significantly reduce the RMS current. Using the proposed clock tree structure, the average RMS current reduction achieves 23%. Note that the reduction of RMS current is meaningful in the control of dynamic power noise due to a smaller current change (i.e., a smaller dI/dt).

Figure 8 gives the corresponding waveforms of the circuit W-Band. The row CLK gives the voltage waveform of the clock source. The row CT gives the current waveforms drawn by the clock trees. The row CT+FF gives the current waveforms drawn by both the clock tree and flip-flops. Note that the simulation results of the single-phase clock tree structure are displayed in dotted line and the simulation results of the proposed clock tree structure are displayed in solid line. Clearly, our approach can significantly reduce the peak current caused by the clock tree (no matter flip-flops are considered or not).

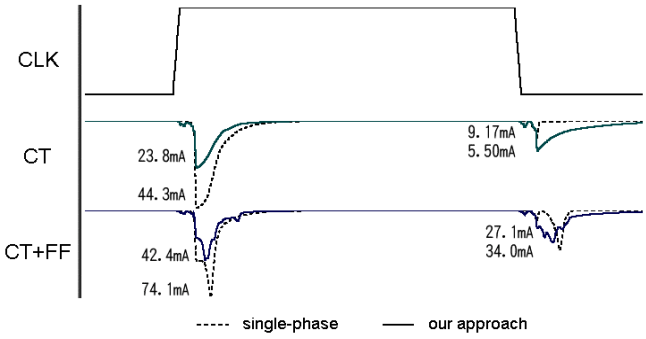

Figure 8. The waveforms of the circuit W-Band.

6. CONCLUSIONS

This paper presents a simple yet effective approach to reducing the peak current caused by the clock tree. Our approach can be easily integrated into the existing design flow. Experimental data consistently show that the peak current of the clock tree can be reduced nearly 50% without any penalty on clock cycle time and total power consumption.

7. ACKNOWLEDGEMENTS

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