Differentiate and Deliver: Leveraging Your Partners (CEO Panel)

Chair: *Jay Vleeschhouwer* - Merrill Lynch
Speakers: *Warren East* - ARM Holdings, plc, Cambridge, UK
Michael J. Fister - Cadence Design Systems, Inc., San Jose, CA
Aart De Geus - Synopsys, Inc., Mountain View, CA
Walden C. Rhines - Mentor Graphics Corp., Wilsonville, OR
Jackson Hu - UMC Corp., Hsinchu, Taiwan
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Abstract

For the past 25 years, the EDA industry has played a major role in the growth of the semiconductor industry, providing tools and services that have helped companies develop electronics products that permeate and improve every aspect of our daily lives.

As the semiconductor industry moves into the nanometer era, they face many key questions when envisioning a new product. When do they want the product to reach the market? How will that product be differentiated? Where do they develop and manufacture that product?

Less than a decade ago, these questions would have been answered completely independent of whatever EDA vendor a semiconductor company selected. However, in the nanometer era, the answers to these questions can be significantly influenced not only by EDA companies but also by the IP and pure-play foundries that make up the infrastructure of the semiconductor industry. In order to compete in a global marketplace, these companies must align their individual core competencies with those of the semiconductor industry to help IC companies create products with the optimal combination of performance, price, and time-to-market.

In this panel, the CEOs of the three major EDA vendors, along with peers from the IP and manufacturing areas discuss these fundamental changes to the semiconductor industry, and the challenges of working together to help customers successfully bring new products to market.

Jay Vleeschhouwer, a senior analyst for Merrill Lynch, will moderate a series of questions for the panelists from the customer's point of view that address how EDA, IP and pureplay foundries can impact the competitiveness of semiconductor companies and the products they develop.
Keywords: Processors, EDS, Intellectual Property, Semiconductor Fabrication, Supplier-Customer Relationships

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Logic Soft Errors in Sub-65nm Technologies Design and CAD Challenges

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ABSTRACT

Logic soft errors are radiation induced transient errors in sequential elements (flip-flops and latches) and combinational logic. Robust enterprise platforms in sub-65nm technologies require designs with built-in logic soft error protection. Effective logic soft error protection requires solutions to the following three problems: (1) Accurate soft error rate estimation for combinational logic networks; (2) Automated estimation of system effects of logic soft errors, and identification of regions in a design that must be protected; and, (3) New cost-effective techniques for logic soft error protection, because classical fault-tolerance techniques are very expensive.

Keywords: Architectural Vulnerability Factor, Built-In Soft Error Resilience, derating, error blocking, error detection, recovery, soft error

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DAC05, pages 5-10

SEU Tolerant Device, Circuit and Processor Design

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ABSTRACT

Development of highly reliable and available systems requires consideration of the occurrence of single event upsets, the effects they have on system performance, and strategies for their prevention and mitigation. Methods of systems engineering process and the application and validation of techniques for fault tolerance are discussed as elements in the elimination and mitigation of single event upsets.

Keywords: Radiation effects, single event upset, soft error rate, fault tolerant systems, error detection and correction coding, fault avoidance, fault masking, modular redundancy, temporal redundancy

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DAC05, pages 11-16

Variability and Energy Awareness: A Microarchitecture-Level Perspective

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ABSTRACT

This paper proposes microarchitecture-level models for Within Die (WID) process and system parameter variability that can be included in the design of high-performance processors. Since decisions taken at microarchitecture level have the largest impact on both performance and power, on one hand, and global variability effect, on the other hand, models and associated metrics are needed for their joint characterization and analysis. To assess how these variations affect or are affected by microarchitecture decisions, we propose a joint performance, power and variability metric that is able to distinguish among various design choices. As a design-driver for the modeling methodology, we consider a clustered high-performance processor implementation, along with its Globally Asynchronous, Locally Synchronous (GALS) counterpart. Results show that, when comparing the baseline, synchronous and its GALS counterpart, microarchitecture-driven impact of process variability translates into 2-10% faster local clocks for the GALS case, while when taking into account the effect of on-chip temperature variability, local clocks can be 8-18% faster. If, in addition, voltage scaling (DVS) is employed, the GALS architecture with DVS is 26% better in terms of the joint quality metric employing energy, performance, and variability.

Keywords: variability, power consumption, GALS design

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Energy-Efficient Physically Tagged Caches for Embedded Processors with Virtual Memory

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ABSTRACT

In this paper we present a low-power tag organization for physically tagged caches in embedded processors with virtual memory support. An exceedingly small subset of tag bits is identified for each application hot-spot so that only these tag bits are used for cache access with no perfromance sacrifice as they provide complete address resolution. The minimal subset of physical tag bits, i.e. the compressed tag, is dynamically updated following the changes in the physical address space of the application. Special support from the operating system (OS) is introduced in order to maintain the compressed tag during program execution. The compressed tag is updated by the OS to match the current set of physical memory pages allocated to the application. We have proposed efficient algorithms that are incorporated within the memory allocator and the dynamic linker in order to achieve dynamic update of the compressed tags in the cases where the mapping between virtual and physical addresses is modified; such cases include memory allocation/deallocation and swapping physical pages on the secondary memory storage. The only hardware support needed within the I/D-caches is the support for disabling bitlines of the tag arrays. An extensive set of experimental results demonstrates the efficacy of the proposed approach.

General Terms: Algorithms, Design, Experimentation, Performance

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Hybrid Simulation for Embedded Software Energy Estimation

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Abstract

Software energy estimation is a critical step in the design of energy-efficient embedded systems. Instruction-level simulation techniques, despite several advances, remain too slow for iterative use in system-level exploration. In this paper, we propose a methodology called *hybrid simulation*, which combines instruction set simulation with selective native execution (execution of some parts of the program directly on the simulation host computer), thereby overcoming the disadvantages of instruction-level simulation (low speed) and pure native execution (estimation accuracy, inapplicability to target-dependent code), while exploiting their advantages. Previously developed techniques for software energy macromodeling are utilized to estimate energy consumption for natively executed sub-programs. We identify and address the main challenges involved in hybrid simulation, and present an automatic tool flow for it, which analyzes a given program and selects functions for native execution in order to achieve maximum estimation efficiency while limiting estimation error. We have applied the proposed hybrid simulation methodology to a variety of embedded software programs, resulting in an average speed-up of 70% and estimation error of at most 6%, compared to one of the fastest publicly-available instruction set simulators.

Keywords: Embedded Software, Energy Estimation, Energy Macromodels, Hybrid Simulation, Pointer Analysis

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Cooperative Multithreading on Embedded Multiprocessor Architectures Enables Energy-scalable Design

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ABSTRACT

We propose an embedded multiprocessor architecture and its associated thread-based programming model. Using a cycle-true simulation model of this architecture, we are able to estimate energy savings for a threaded C program. The savings are obtained by voltage- and frequency-scaling of the individual processors. We port a fingerprint minutiae detection application onto this architecture, and show the resulting performance on single-, dual-, and quad-processor configurations. The energy-scaled quad-processor version results in a 77 % energy reduction over the single-processor non-scaled implementation, at only a 2.2 % degradation in cycle count.

General Terms: Design, Performance.

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DAC05, pages 31-36

Total Power Reduction in CMOS Circuits via Gate Sizing and Multiple Threshold Voltages

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ABSTRACT

Minimizing power consumption is one of the most important objectives in IC design. Resizing gates and assigning different V_t's are common ways to meet power and timing budgets. We propose an automatic implementation of both these techniques using a mixed-integer linear programming model called *MLP-exact*, which minimizes a circuit's total active-mode power consumption. Unlike previous linear programming methods which only consider local optimality, *MLP-exact* can find a true global optimum. An efficient, non-optimal way to solve the MLP model, called *MLP-fast*, is also described. We present a set of benchmark experiments which show that *MLP-fast* is much faster than *MLPexact,* while obtaining designs with only slightly higher power consumption. Furthermore, the designs generated by *MLP-fast* consume 30% less power than those obtained by conventional, sensitivity-based methods.

Keywords: Low power, linear programming, dual V_t, gate sizing

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An Effective Power Mode Transition Technique in MTCMOS Circuits

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Abstract

The large magnitude of supply/ground bounces, which arise from power mode transitions in power gating structures, may cause spurious transitions in a circuit. This can result in wrong values being latched in the circuit registers. We propose a design methodology for limiting the maximum value of the supply/ground currents to a user-specified threshold level while minimizing the wake up (sleep to active mode transition) time. In addition to controlling the sudden discharge of the accumulated charge in the intermediate nodes of the circuit through the sleep transistors during the wake up transition, we can eliminate short circuit current and spurious switching activity during this time. This is in turn achieved by reducing the amount of charge that must be removed from the intermediate nodes of the circuit and by turning on different parts of the circuit in a way that causes a uniform distribution of current over the wake up time. Simulation results show that, compared to existing wakeup scheduling methods, the proposed techniques result in a one to two orders of magnitude improvement in the product of the maximum ground current and the wake up time.

General Terms: Algorithms, Performance, Design, Reliability.

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A Self-adjusting Scheme to Determine the Optimum RBB by Monitoring Leakage Currents

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ABSTRACT
Reverse body biasing (RBB) is often used to reduce the leakage power of a device. However, recent research has shown that if this applied RBB is too high, the leakage power can actually increase due to the contribution of Band-to-Band Tunneling (BTBT) currents. Hence, there exists an optimal RBB value at which the leakage is minimum. This optimum point can vary with temperature and process variations. In this paper we show that it is desirable to operate at the optimal RBB point which minimizes total leakage. We present a scheme that monitors the total leakage current (the sum of the sub-threshold, BTBT and gate leakage) of an IC with a representative leaking device and, using this monitored value, automatically finds the optimum RBB value across temperature and process corners, using a self-adjusting circuit. Our approach has a modest placed-and-routed area utilization, and a low power consumption.
Keywords: Leakage power, Body-biasing, Self-adjusting

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Enhanced Leakage Reduction Technique by Gate Replacement

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Abstract

Input vector control (IVC) technique utilizes the stack effect in CMOS circuit to apply the minimum leakage vector (MLV) to the circuit at the sleep mode to reduce leakage. Additional logic gates can be inserted as control points to make it more effective. In this paper, we propose a gate replacement technique that further enhances the leakage reduction. The basic idea is to replace a gate that is in its worst leakage state by another library gate while keeping the circuit's correct functionality at the active mode. We also develop a divide-and-conquer approach that integrates a fast gate replacement heuristic, an optimal MLV search strategy for tree circuit, and a genetic algorithm to connect the tree circuits. We conduct experiments on the MCNC91 benchmark circuits. The results reveal that our technique can reduce additional 10% to 24% leakage over the best known IVC methods and the optimal MLV with no delay penalty and little area increase.

Keywords: Leakage reduction, gate replacement, MLV

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Automated Nonlinear Macromodelling of Output Buffers for High-Speed Digital Applications

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ABSTRACT

We present applications of a recently developed automated nonlinear macromodelling approach to the important problem of macromodelling high-speed output buffers/drivers. Good nonlinear macromodels of such drivers are essential for fast signal-integrity and timing analysis in high-speed digital design. Unlike traditional black-box modelling techniques, our approach extracts nonlinear macromodels of digital drivers *automatically* from SPICE-level descriptions. Thus it can naturally capture transistor-level nonlinearities in the macromodels, resulting in far more accurate signal integrity analysis, while retaining significant speedups. We demonstrate the technique by automatically extracting macromodels for two typical digital drivers. Using the macromodel, we obtain about 8× speedup in average with excellent accuracy in capturing different loading effects, crosstalk, simultaneous switching noise (SSN), *etc.*.

Keywords: nonlinear macromodeling, I/O buffer macromodeling

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Systematic Development of Analog Circuit Structural Macromodels through Behavioral Model Decoupling

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ABSTRACT
This paper presents a systematic methodology to create customized structural macromodels for a specific analog circuit. The novel contributions of the method include definition of the building block behavioral concept and two original algorithms to generate structural models. Experiments are offered for two-stage opamp and operational transconductor amplifier (OTA) circuits. The automatically produced models are accurate, offer design insight, and require low modeling effort.
Keywords: Analog circuits, Structural macromodel

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A Combined Feasibility and Performance Macromodel for Analog Circuits

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ABSTRACT

The need to reuse the performance macromodels of an analog circuit topology challenges existing regression based modeling techniques. A model of good reusability should have a number of independent design parameters and each parameter can vary in a large numeric range. On the other hand, these requirements can cause a large percentage of functionally incorrect designs in the design space and thus results in a sparse feasible design space. They also complicate the mathematical relationship between the performance parameters and the design parameters. In order to tackle these challenges, this paper presents a combined feasibility and performance macromodel based on Support Vector Machines (SVMs). The feasibility model identifies the feasible designs that satisfy the design constraints. The performance macromodel is valid for feasible designs. Feasibility macromodeling is formulated as a classification problem while performance macromeling as a regression problem. An active learning scheme [5] has been applied to improve the accuracy of the feasibility model much faster than only using uniformly distributed designs in the entire design space. Our experiment shows that the performance macromodels in the feasible design space are more accurate and faster to construct and evaluate than performance macromodels in the entire design space without functional or performance constraints considered.

Keywords: Performance macromodeling, feasibility models, active learning

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ESL: Tales from the Trenches

Chair: *David Maliniak* - Electronic Design, Paramus, NJ
Panelists: *Terry Doherty* – Emulex, Bothell, WA
Peter McShane - Northrop Grumman, Redondo Beach, California
Suhas A. Pai – Qualcomm, San Diego, CA
Sriram Sundararajan - Texas Instruments Inc., Dallas, TX
Dr. Soo-Kwan Eo - ST Microelectronics, SEOUL, Korea
Pascal Urard - ST Microelectronics, The Netherlands

PANEL SUMMARY

Electronic System-Level design has arrived - but can ESL provide the bridge from systems to silicon? Comprised of real world designers, this DAC ESL panel will examine and debate what works, what doesn't, and what the gaps are in the methodology and tool offerings. Panelists from a variety of industry segments, including Military/aerospace, storage area networks (SAN), wireless communications and consumer electronics, will share their experiences, lessons learned and further needs.

Does ESL bridge the gap between systems to silicon? Hear from designers about their real world experience with ESL. What worked according to expectations? What didn't? What are the gaps in the methodology and tool offerings that need to be filled, and why?

This panel of ESL design methodology users will give us a "reality check" that will enable potential users to make an adoption decision, and enable ESL design tool suppliers to evaluate their product strategies against "big picture" requirements.

Panelists will address primary areas of concern, such as:

Methodology Usage: What do you use ESL design for? Is it for algorithm development alone? Are you using it for hardware/software partitioning? Have you used it for embedded system architecture development for performance optimization and/or for SoC platform development? Are you using ESL for embedded software development, using the system architecture model as a development platform? Are you doing any highlevel synthesis of RTL? Did ESL help you with your system testbench development or HW/SW co-verification?

Industry-Level Initiatives: How has language standardization, such as SystemC, impacted your design efforts? What other industry-level initiatives would be of use - standard TLM methodology, or other?

Tools: Do you use commercial tools or open source software? What was your selection criteria? Do you use domain-specific tools for algorithm development and implementation? Did you develop your own tools - if so, why? Do your proprietary tools have specific attributes that you think can be incorporated into commercial tools? How do ESL tools compare with your original expectations?

ROI: What was your overall payback in terms of time, effort and money consumption, re-usability, risk management and overall success? How do these compare with your original expectations?

Keywords: Electronic system-level design

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Parameterized Block-Based Statistical Timing Analysis with Non-Gaussian Parameters, Nonlinear Delay Functions

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ABSTRACT

Variability of process parameters makes prediction of digital circuit timing characteristics an important and challenging problem in modern chip design. Recently, statistical static timing analysis (statistical STA) has been proposed as a solution. Unfortunately, the existing approaches either do not consider explicit gate delay dependence on process parameters [3] - [6] or restrict analysis to linear Gaussian parameters only [1, [2]. Here we extend the capabilities of parameterized block-based statistical STA [1] to handle nonlinear function of delays and non-Gaussian parameters, while retaining maximum efficiency of processing linear Gaussian parameters. Our novel technique improves accuracy in predicting circuit timing characteristics and retains such benefits of parameterized block-based statistical STA as an incremental mode of operation, computation of criticality probabilities and sensitivities to process parameter variations. We implemented our technique in an industrial statistical timing analysis tool. Our experiments with large digital blocks showed both efficiency and accuracy of the proposed technique.

General Terms: Algorithms, performance, design.

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Correlation-Aware Statistical Timing Analysis with Non-Gaussian Delay Distributions

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ABSTRACT

Process variations have a growing impact on circuit performance for today's integrated circuit (IC) technologies. The Non-Gaussian delay distributions as well as the correlations among delays make statistical timing analysis more challenging than ever. In this paper, we present an efficient block-based statistical timing analysis approach with linear complexity with respect to the circuit size, which can accurately predict Non-Gaussian delay distributions from realistic nonlinear gate and interconnect delay models. This approach accounts for all correlations, from manufacturing process dependence, to re-convergent circuit paths to produce more accurate statistical timing predictions. With this approach, circuit designers can have increased confidence in the variation estimates, at a low additional computation cost.

Keywords: Statistical timing, process variation

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Correlation-Preserved Non-Gaussian Statistical Timing Analysis with Quadratic Timing Model

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ABSTRACT

Recent study shows that the existing first order canonical timing model is not sufficient to represent the dependency of the gate delay on the variation sources when processing and operational variations become more and more significant. Due to the nonlinearity of the mapping from variation sources to the gate/wire delay, the distribution of the delay is no longer Gaussian even if the variation sources are normally distributed. A novel *quadratic timing model* is proposed to capture the non-linearity of the dependency of gate/wire delays and arrival times on the variation sources. Systematic methodology is also developed to evaluate the correlation and distribution of the quadratic timing model. Based on these, a novel statistical timing analysis algorithm is propose which retains the complete correlation information during timing analysis and has the same computation complexity as the algorithm based on the canonical timing model. Tested on the ISCAS circuits, the proposed algorithm shows 10× accuracy improvement over the existing first order algorithm while no significant extra runtime is needed.

General Terms: Algorithms, Performance, Verification

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A General Framework for Accurate Statistical Timing Analysis Considering Correlations

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ABSTRACT

The impact of parameter variations on timing due to process and environmental variations has become significant in recent years. With each new technology node this variability is becoming more prominent. In this work, we present a general Statistical Timing Analysis (STA) framework that captures spatial correlations between gate delays. Our technique does not make any assumption about the distributions of the parameter variations, gate delay and arrival times. We propose a Taylor-series expansion based polynomial representation of gate delays and arrival times which is able to effectively capture the non-linear dependencies that arise due to increasing parameter variations. In order to reduce the computational complexity introduced due to polynomial modeling during STA, we propose an efficient linear-modeling driven polynomial STA scheme. On an average the degree-2 polynomial scheme had a 7.3x speedup as compared to Monte Carlo with 0.049 units of rms error w.r.t Monte Carlo. Our technique is generic and can be applied to arbitrary variations in the underlying parameters.

Keywords: Statistical timing, variability, correlation

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Locality-Conscious Workload Assignment for Array-Based Computations in MPSOC Architectures

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ABSTRACT

While the past research discussed several advantages of multiprocessor-system-on-a-chip (MPSOC) architectures from both area utilization and design verification perspectives over complex single core based systems, compilation issues for these architectures have relatively received less attention. Programming MPSOCs can be challenging as several potentially conflicting issues such as data locality, parallelism and load balance across processors should be considered simultaneously. Most of the compilation techniques discussed in the literature for parallel architectures (not necessarily for MPSOCs) are loop based, i.e., they consider each loop nest in isolation. However, one key problem associated with such loop based techniques is that they fail to capture the interactions between the different loop nests in the application. This paper takes a more global approach to the problem and proposes a compilerdriven data locality optimization strategy in the context of embedded MPSOCs. An important characteristic of the proposed approach is that, in deciding the workloads of the processors (i.e., in parallelizing the application) it considers all the loop nests in the application simultaneously. Our experimental evaluation with eight embedded applications shows that the global scheme brings significant power/performance benefits over the conventional loop based scheme.

Keywords: Data Locality, MPSoC

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Automatic Scenario Detection for Improved WCET Estimation

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ABSTRACT

Modern embedded applications usually have real-time constraints and they are implemented using heterogeneous multiprocessor systems-on-chip. Dimensioning a system requires accurate estimations of the worst-case execution time (WCET). Overestimation leads to over-dimensioning. This paper introduces a method for automatic discovery of scenarios that incorporate correlations between different parts of applications. It is based on the application parameters with a large impact on the execution time. We show on a benchmark that, using scenarios, the estimated WCET may be reduced with 16%.

Keywords: WCET, Real-Time, Scenarios

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Memory Access Optimization Through Combined Code Scheduling, Memory Allocation, and Array Binding in Embedded System Design

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ABSTRACT

In many of embedded systems, particularly for those with high data computations, the delay of memory access is one of the major bottlenecks in the system's performance. It has been known that there are high variations in memory access delays depending on the ways of designing memory configurations and assigning arrays to memories. Furthermore, embedded DRAM technology that provides efficient access modes is actively developed, possibly becoming a mainstream in future embedded system design. In that context, in this paper we propose an effective solution to the problem of (embedded DRAM) memory allocation and mapping in memory access code generation with the objective of minimizing the total memory access time. Specifically, the proposed approach, called MACCESS-opt, solves the three problems simultaneously: (i) determination of memories, (ii) mapping of arrays to memories, and (iii) scheduling of memory access operations, so that the use of DRAM access modes is maximized while satisfying the storage size constraint of embedded system. Experimental data on a set of benchmark designs are provided to show the effectiveness of the proposed integrated approach. In short, MACCESS-opt reduces the total memory access latency by over 18%, from which we found that our memory mapping and scheduling techniques in MACCESS-opt contribute about 12% and 6% reductions of total memory access latency, respectively.

Keywords: memory access, scheduling, binding

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Dynamic Slack Reclamation with Procrastination Scheduling in Real-Time Embedded Systems

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ABSTRACT
Leakage energy consumption is an increasing concern in current and future CMOS technology generations. Procrastination scheduling, where task execution can be delayed to maximize the duration of idle intervals, has been proposed to minimize leakage energy drain. We address dynamic slack reclamation techniques under procrastination scheduling to minimize the static and dynamic energy consumption. In addition to dynamic task slowdown, we propose dynamic procrastination which seeks to extend idle intervals through slack reclamation. While using the entire slack for either slowdown or procrastination need not be the most energy efficient approach,we distribute the slack between slowdown and procrastination to exploit maximum energy savings. Our simulation experiments show that dynamic slowdown results on an average 10% energy gains over static slowdown. Dynamic procrastination extends the average sleep interval by 25% which reduces the idle energy consumption by 15%, while meeting all timing requirements.

Keywords: dynamic slack reclamation, task procrastication, leakage power, critical speed, low power scheduling, real-time systems

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Response Compaction with any Number of Unknowns using a new LFSR Architecture

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ABSTRACT
This paper presents a new test response compaction technique with any number of unknown logic values (X's) in the test response bits. The technique leverages an X-tolerant response compactor (X-compact), and forces X's that are not tolerated by X-Compact to known values. The data required to designate the X's not tolerated by the X-compactor, also called mask data, is stored in a compressed format on the tester and decompressed onchip. We applied this technique to four industrial designs and obtained 26-fold to 60-fold reduction in test response data volume with no impact on test quality.
Keywords: VLSI Test, Compression, X-compact, LFSR, BIST

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Multi-Frequency Wrapper Design and Optimization for Embedded Cores Under Average Power Constraints

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ABSTRACT

This paper presents a new method for designing test wrappers for embedded cores with multiple clock domains. By exploiting the use of multiple shift frequencies, the proposed method improves upon a recent wrapper design method that requires a common shift frequency for the scan elements in the different clock domains. We present an integer linear programming (ILP) model that can be used to minimize the testing time for small problem instances. We also present an efficient heuristicmethod that is applicable to large problem instances, and which yields the same (optimal) testing time as ILP for small problem instances. Compared to recent work on wrapper design using a single shift frequency, we obtain lower testing times and the reduction in testing time is especially significant under power constraints.

Keywords: Wrapper Design, Multiple Clock Domains, Scan Control Unit

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N-Detection Under Transparent-Scan

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Abstract

We study the quality of test sequences under a test application scheme called transparent-scan as *n* -detection test sequences. We obtain transparent-scan sequences from combinational test sets. We show that for the same number of clock cycles required to apply a compact single-detection combinational test set, a transparent-scan sequence detects faults more times than the combinational test set. We note that a transparent-scan sequence based on a combinational test set contains unspecified values. We consider several procedures for specifying the unspecified values of the transparent-scan sequence, and study their effects. We also study the extension of a transparent-scan test sequence into an *n* -detection test sequence that detects every target fault at least *n* times.

Keywords: *n* -detection test sets, scan design, test generation

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DAC05, pages 135-140

Secure Scan: A Design-for-Test Architecture for Crypto Chips

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ABSTRACT

Scan-based Design-for-Test (DFT) is a powerful testing scheme, but it can be used to retrieve the secrets stored in a crypto chip thus compromising its security. On one hand, sacrificing security for testability by using traditional scan-based DFT restricts its use in privacy sensitive applications. On the other hand, sacrificing testability for security by abandoning scan-based DFT hurts product quality. The security of a crypto chip comes from the small secret key stored in a few registers and the testability of a crypto chip comes from the data path and control path implementing the crypto algorithm. Based on this key observation, we propose a novel scan DFT architecture called secure scan that maintains the high test quality of traditional scan DFT without compromising the security. We used a hardware implementation of the Advanced Encryption Standard (AES) to show that the traditional Scan DFT scheme can compromise the secret key. We then showed that by using secure scan DFT, neither the secret key nor the testability of the AES implementation is compromised.

Keywords: Scan-based DFT, Testability, Security, Crypto Hardware

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A Green Function-Based Parasitic Extraction Method for Inhomogeneous Substrate Layers

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ABSTRACT

This paper presents a new Green function-based approach for substrate parasitic extraction in substrates with inhomogeneous layers. This new formulation allows analysis of noise coupling with sinkers, trenches and wells, - a limitation in prior Green function-based extractors. Numerical examples for sinkers and trenches are provided and compared with the results from three-dimensional semiconductor device simulations. It is shown that the proposed method is accurate and computationally efficient.

Keywords: Substrate noise, parasitic extraction, Green function

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Analysis of Full-Wave Conductor System Impedance over Substrate Using Novel Integration Techniques

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ABSTRACT

An efficient approach to full-wave impedance extraction is developed that accounts for substrate effects through the use of two-layer media Green's functions in a mixed-potential-integral-equation (MPIE) solver. Particularly, the choice of implementation for the layered media Green's functions motivates the development of accelerated techniques for both volume and surface integrations in the solver. Solver accuracy is validated against measurements taken on fabricated devices; solver efficiency is demonstrated by its 9.8X reduction in cost in comparison to the traditional integration approach.

Keywords: Impedance extraction, Substrate modeling, Integral equation solver

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Spatially Distributed 3D Circuit Models

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Abstract
Spatially distributed 3D circuit models are extracted with a segment-to-segment BEM (Boundary Element Method) algorithm for both capacitance and inverse inductance couplings rather than using the traditional net-to-net approach. Critical issues regarding the extraction efficiency and accuracy of segment-to-segment BEM capacitance models are explored. An adaptive discretization scheme is developed for segment-to-segment capacitance extraction and also applied to segment-to-segment high-frequency inverse inductance extraction. We demonstrate the limitations of the duality between capacitance and inverse inductance. Examples demonstrating the accuracy of these models are presented for real packaging cases.
Keywords: Distributed Circuit Models, Boundary Element Method (BEM), Capacitance, Inverse Inductance

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DiMES: Multilevel Fast Direct Solver based on Multipole Expansions for Parasitic Extraction of Massively Coupled 3D Microelectronic Structures

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ABSTRACT

Boundary element methods are being successfully used for modeling parasitic effects in cutting-edge circuit design. The dense system matrix generated therein presents a time and memory bottleneck. Fast iterative solver techniques, developed to address the problem, suffer from convergence issues which become pronounced for large number of right hand sides as is the case for massively coupled systems. In this paper an iteration free solution scheme is presented. The dense matrix is rendered sparse by applying multilevel multipole expansions, and the resultant sparse matrix is solved by a traditional sparse matrix solver. The accuracy and time and memory requirements for the solver are compared against the regular methods. The advantage of the presented method over the corresponding iterative scheme is also demonstrated.

Keywords: Parasitics, Multilevel, Multipole, Non-Iterative

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ICCAP: A Linear Time Sparse Transformation and Reordering Algorithm for 3D BEM Capacitance Extraction

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ABSTRACT
This paper presents an efficient hierarchical 3D capacitance extraction algorithm — ICCAP. Most previous capacitance extraction algorithms introduce intermediate variables to facilitate the hierarchical potential calculation but still preserve the leaf panels as the basis. In this paper, we discover that those intermediate variables are fundamentally much better basis than leaf panels. As a result, we are able to explicitly construct the sparse potential coefficient matrix and solve it with linear memory in linear runtime. Furthermore, the explicit sparse formulation not only enables the usage of preconditioned iterative Krylov subspace methods but also the reordering technique. A new reordering technique is proposed to further reduce over 20% of memory consumption and runtime in comparison to no reordering techniques applied. Experimental results demonstrate the superior runtime and memory consumption of ICCAP over previous approaches while achieving similar accuracy.
Keywords: Boundary element method, capacitance, parasitic extraction, interconnect, iterative methods

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Choosing Flows and Methodologies for SoC Design

Chair: *Dennis C. Wassung, Jr.* - Adams Harkness, Inc.
Speakers: *Magdy Abadir* – Freescale Semiconductor, Inc., Austin, TX
Mark Bapst – PrairieComm, Rolling Meadows, IL
Colin Harris - PMC-Sierra, Vancouver, BC

Abstract
Moving to new semiconductor technology nodes can dramatically impact the business performance of the SoC company, and its age-old design and manufacturing flows and methodologies. It can also significantly affect its choices of suppliers. This session will provide an overview of changing needs and corresponding management decision criteria to make the right choices from a pool of alternate options.

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DFM Rules!

Chair: *Naveed Sherwani* - Open-Silicon
Panelists: *Alex Alexanian* - Ponté Solutions, Mountain View, CA
Harold Lehon - KLA-Tencor, San Jose, CA
Premal Buch - Magma Design Automation, Sunnyvale, CA
Peter Rabkin – Xilinx, San Jose, CA
Carlo Guardiani - PDF Solutions, Desenzano Sul Garda, Italy
Atul Sharan - Clearshape Technologies, Sunnyvale, CA

ABSTRACT
For sub-100nm processes, predictions are putting initial process yields in the single digits. At the same time, at 130nm, we saw that two chips designed with the same methodology and same design rules could deliver completely different manufacturing yields.

This panel will discuss the reasons for these phenomena and talk about future trends in DFM that will need to be addressed for success below 100nm.
Keywords: Design for Manufacturability, Yield Optimization

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Partitioning-Based Approach to Fast On-Chip Decap Budgeting and Minimization

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ABSTRACT
This paper proposes a fast decoupling capacitance (decap) allocation and budgeting algorithm for both early stage decap estimation and later stage decap minimization in today's VLSI physical design. The new method is based on a sensitivity-based conjugate gradient (CG) approach. But it adopts several new techniques, which significantly improve the efficiency of the optimization process. First, the new approach applies the time-domain merged adjoint network method for fast sensitivity calculation. Second, an efficient search step scheme is proposed to replace the time-consuming line search phase in conventional conjugate gradient method for decap budget optimization. Third, instead of optimizing an entire large circuit, we partition the circuit into a number of smaller sub-circuits and optimize them separately by exploiting the locality of adding decaps. Experimental results show that the proposed algorithm achieves at least 10X speed-up over the fastest decap allocation method reported so far with similar or even better budget quality and a power grid circuit with about one million nodes can be optimized using the new method in half an hour on the latest Linux workstations.
Keywords: Decoupling Capacitor, IR drop, On-Chip Power/Grid Networks

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Navigating Registers in Placement for Clock Network Minimization

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ABSTRACT
The progress of VLSI technology is facing two limiting factors: power and variation. Minimizing clock network size can lead to reduced power consumption, less power supply noise, less number of clock buffers and therefore less vulnerability to variations. Previous works on clock network minimization are mostly focused on clock routing and the improvements are often limited by the input register placement. In this work, we propose to navigate registers in cell placement for further clock network size reduction. To solve the conflict between clock network minimization and traditional placement goals, we suggest the following techniques in a quadratic placement framework: (1) Manhattan ring based register guidance; (2) center of gravity constraints for registers; (3) pseudo pin and net; (4) register cluster contraction. These techniques work for both zero skew and prescribed skew designs in both wirelength driven and timing driven placement. Experimental results show that our method can reduce clock net wirelength by 16%~33% with no more than 0.5% increase on signal net wirelength compared with conventional approaches.
Keywords: Clock network, placement, low power, variation tolerance

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Minimizing Peak Current via Opposite-Phase Clock Tree

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ABSTRACT
Although a lot of research efforts have been made in the minimization of the total power consumption caused by the clock tree, no attention has been paid to the minimization of the peak current caused by the clock tree. In this paper, we propose an opposite-phase scheme for peak current reduction. Our basic idea is to divide the clock buffers at each level of the clock tree into two sets: an half of clock buffers operate at the same phase of the clock source, and another half of clock buffers operate at the opposite phase of the clock source. Consequently, our approach can reduce the peak current of the clock tree nearly 50%. Experimental data consistently show that our approach works well in practice.
Keywords: Physical design, Clock network synthesis, Low power

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A Noise-Driven Effective Capacitance Method With Fast Embedded Noise Rule Calculation for Functional Noise Analysis

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ABSTRACT

We present a noise-driven effective capacitance method for estimating the combined propagation noise and crosstalk noise. Gate propagation noise rules are efficiently calculated inside the Ceff procedure to determine a linear Thevenin model of the victim driver. A voltage-dependent current source model [2, 6] of the driver, along with a load capacitor is analyzed to generate the gate output waveform, from which noise rules are directly extracted. This method removes potential errors introduced in traditional look-up table or fitted-equation based noise rules. The linear driver Thevenin model can then be employed to analyze the propagation noise, while the same Thevenin resistance can be used to analyze the crosstalk noise. The combined coupling and propagation noise can then be estimated using superposition. In this work, we extend the popular timing-driven effective capacitance method into the noise domain. Similar to the effective capacitance method in timing analysis, this technique can successfully separate the nonlinear driver analysis from the linear interconnect analysis. In addition, the linear driver model can significantly ease the task of finding the worst-case peak alignment among all the victim and aggressor noise sources. Experimental results on both RC and RLC nets from industry designs show both accuracy and efficiency compared to SPICE results.

Keywords: Effective Capacitance, Glitch Propagation, Noise Analysis

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Constraint-Aware Robustness Insertion for Optimal Noise-Tolerance Enhancement in VLSI Circuits

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ABSTRACT

Reliability of nanometer circuits is becoming a major concern in today's VLSI chip design due to interferences from multiple noise sources as well as radiation-induced soft errors. Traditional noise analysis/avoidance and manufacturing testing are no longer sufficient to handle the dynamic interactions between various noise sources and unpredictable operational variations. Therefore, "robustness insertion" has been adopted as the supplementary approach to ensure high circuit reliability through on-line protections. However, the related design overhead is not always acceptable, especially for cost/timing-sensitive designs. In this paper, we present a novel "**constraint-aware robustness insertion**" methodology protect the sequential elements in digital circuits against various noise effects. Based on a configurable hardening sequential cell design and an efficient sequential cell robustness estimation technique, an optimization algorithm is developed to search for the optimal protection scheme under given timing and area constraints. Experiment results demonstrate that the proposed methodology is able to achieve a high degree of noise-tolerance while keeping the protection cost within limit.

Keywords: Nanometer circuits, Robustness calibration, Circuit hardening, Robustness insertion

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Temperature-Aware Resource Allocation and Binding in High-Level Synthesis

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ABSTRACT

Physical phenomena such as temperature have an increasingly important role in performance and reliability of modern process technologies. This trend will only strengthen with future generations. Attempts to minimize the design effort required for reaching closure in reliability and performance constraints are agreeing on the fact that higher levels of design abstractions need to be made aware of lower level physical phenomena. In this paper, we investigated techniques to incorporate temperature-awareness into high-level synthesis. Specifically, we developed two temperature-aware resource allocation and binding algorithms that aim to minimize the maximum temperature that can be reached by a resource in a design. Such a control scheme will have an impact on the prevention of hot spots, which in turn is one of the major hurdles in front of reliability for future integrated circuits. Our algorithms are able to reduce the maximum attained temperature by any module in a design by up to 19.6^{o}C compared to a binding that optimizes switching power.

Keywords: Binding, Temperature, Switching, Leakage

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Leakage Power Optimization With Dual-V_{th} Library In High-Level Synthesis

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ABSTRACT
In this paper we address the problem of module selection during high-level synthesis. We present a heuristic algorithm for leakage power optimization based on the maximum weight independent set problem. A dual threshold voltage (V_{th}) technique is used to reduce leakage energy consumption in a data flow graph. Experiments are performed on a data-path dominated test suite of six benchmarks. Our approach achieves an average of 70.9% leakage power reduction, which is very close to the optimal results from an Integer Linear Programming approach.
Keywords : Leakage Power, High-Level Synthesis, Dual-V_{th}, Optimization

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Incremental Exploration of the Combined Physical and Behavioral Design Space

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ABSTRACT

Achieving design closure is one of the biggest headaches for modern VLSI designers. This problem is exacerbated by high-level design automation tools that ignore increasingly important factors such as the impact of interconnect on the area and power consumption of integrated circuits. Bringing physical information up into the logic level or even behavioral-level stages of system design is essential to solve this problem. In this paper, we present an incremental floorplanning high-level synthesis system. This system integrates high-level and physical design algorithms to concurrently improve a system's schedule, resource binding, and floorplan, thereby allowing the incremental exploration of the combined behavioral-level and physical-level design space. Compared with previous approaches that repeatedly call loosely coupled floorplanners for physical estimation, this approach has the benefit of efficiency, stability, and better quality of results. For designs containing functional units with non-unity aspect ratios, the average CPU time improved by 369 %, the area improved by 14.24%, and power improved by 4 %.

Keywords: High-level Synthesis, Incremental, Floorplan

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Sign Bit Reduction Encoding For Low Power Applications

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ABSTRACT
This paper proposes a low power technique, called SBR (Sign Bit Reduction) which may reduce the switching activity in multipliers as well as data buses. Utilizing the multipliers based on this scheme, the dynamic power consumption of some digital systems such as digital filters based on CMOS logic system can be reduced considerably compared to those based on 2's complement implementation. To verify the efficacy of the SBR, a 16-bit multiplier was implemented by this scheme. The results for voice data show an average of 29% to 35% switching reduction compared to the 2's complement implementation. For 16-bit random data, this scheme decreases the switching of 16-bit multipliers by an average of 21%. Finally, the application of the technique to a 16-bit data bus leads up to 14.5% switching reduction on average.
Keywords: Switching Activity, Low Power, Signed Multiplier, Bus Encoding, Sing Extension

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A Watermarking System for IP Protection by a Post Layout Incremental Router

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ABSTRACT

In this paper, we introduce a new watermarking system for IP protection on post-layout design phase. Firstly the copyright is encrypted by DES (Data Encryption Standard) and then embedded by using an incremental router into the layout design. This watermarking technique uniquely identifies the circuit origin, yet is difficult to be detected or fabricated. The incremental router consists of a rip-up and a special re-router that inserts redundant bends into wires probabilistic. We evaluated the technique on various generated benchmark circuits to validate the completeness of the procedure. The results show it achieves almost 100% success for embedding with no extra area cost on design performances.

Keywords: Intellectual Property Protection (IPP), Post layout design, Incremental router, Watermarking

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A Side-Channel Leakage Free Coprocessor IC in 0.18μm CMOS for Embedded AES-based Cryptographic and Biometric Processing

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ABSTRACT
Security ICs are vulnerable to side-channel attacks (SCAs) that find the secret key by monitoring the power consumption and other information that is leaked by the switching behavior of digital CMOS gates. This paper describes a side-channel attack resistant coprocessor IC and its design techniques. The IC has been fabricated in 0.18μm CMOS. The coprocessor, which is used for embedded cryptographic and biometric processing, consists of four components: an Advanced Encryption Standard (AES) based cryptographic engine, a fingerprint-matching oracle, a template storage, and an interface unit. Two functionally identical coprocessors have been fabricated on the same die. The first, 'secure', coprocessor is implemented using a logic style called Wave Dynamic Digital Logic (WDDL) and a layout technique called differential routing. The second, 'insecure', coprocessor is implemented using regular standard cells and regular routing techniques. Measurement-based experimental results show that a differential power analysis (DPA) attack on the insecure coprocessor requires only 8,000 acquisitions to disclose the entire 128b secret key. The same attack on the secure coprocessor still does not disclose the entire secret key at 1,500,000 acquisitions. This improvement in DPA resistance of at least 2 orders of magnitude makes the attack de facto infeasible. The required number of measurements is larger than the lifetime of the secret key in most practical systems.

Keywords: Countermeasure, Side-Channel Attack, Differential Power Analysis, Encryption, Smart Card, Security IC

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Simulation Models for Side-Channel Information Leaks

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ABSTRACT
Small, embedded integrated circuits (ICs) such as smart cards are vulnerable to so-called side-channel attacks (SCAs). The attacker can gain information by monitoring the power consumption, execution time, electromagnetic radiation and other information that is leaked by the switching behavior of digital CMOS gates. Ever since power attacks have been introduced in 1999, many countermeasures have been proposed. Often a significant increase in security has been touted. We will show that in order to assess the effectiveness of a countermeasure, a correct simulation model of the side-channel information leaks is vital. We will show that seemingly correct approximations can lead to completely flawed results.
Keywords: Simulation Model, Countermeasure, Side-Channel Attack, Differential Power Analysis, Encryption, Smart Card, Security IC

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A Pattern Matching Coprocessor for Network Security

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ABSTRACT

It has been estimated that computer network worms and virus caused the loss of over $55B in 2003. Network security system use techniques such as deep packet inspection to detect the harmful packets. While software intrusion detection system running on general purpose processors can be up-dated in response to new attacks. They lack the processing power to monitor gigabit networks. We present a high performance pattern matching co-processor architecture that can be used to monitor and identify a large number of intrusion signature. The design consists of a bank of pattern matchers that are used to implement a highly concurrent filter. The pattern matchers can be programmed to match multiple patterns of various lengths, and are able to leverage the existing databases of threat signatures. We have been able to program the filters to match all the payload patterns defined in the widely used Snort network intrusion detection system at a rate above 7 Gbps, with memory space left to accommodate threat signatures that become available in the future.

Keywords: Network security, Intrusion, Pattern matching, Pattern search, Snort

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High Performance Encryption Cores for 3G Networks

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ABSTRACT

This paper presents two novel and high performance hardware architectures, implemented in FPGA technology, for the KASUMI block cipher; this algorithm lies at the core of the confidentiality and integrity algorithms defined for the Universal Mobile Telecommunication System (UMTS) standard. The first proposal is a pipelined design and the second implements an iterative approach. The throughput for these architectures turn out to be higher than the throughput achieved by other proposals.

Keywords: 3G, UMTS Security Architecture, KASUMI, FPGA

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Efficient Fingerprint-based User Authentication for Embedded Systems

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ABSTRACT

User authentication, which refers to the process of verifying the identity of a user, is becoming an important security requirement in various embedded systems. While conventional solutions for user authentication have relied on password-based mechanisms, they are increasingly being replaced by biometric technologies such as fingerprint, face, and voice recognition, which are known to provide higher levels of security for user authentication. This paper investigates the problem of supporting efficient fingerprint-based user authentication in embedded systems. For improving the performance of fingerprint-based authentication, we propose hardware/software enhancements that include a generic set of custom instruction extensions to an embedded processor's instruction set architecture, a memory-aware software re-design, and fixed-point arithmetic. We believe that the custom instruction set extensions proposed in this work are generic enough to speed up many fingerprint matching algorithms and even other biometric algorithms. Our experiments with an open-source, high-fidelity fingerprint authentication algorithm and a testbed featuring a commercial extensible processor show that performance is improved by a factor of 10.4X when using the proposed enhancements, while incurring modest overheads.

Keywords: User authentication, fingerprint, extensible processors

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Approximate VCCs: A New Characterization of Multimedia Workloads for System-level MpSoC Design

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ABSTRACT

System-level design methods specifically targeted towards multimedia applications have recently received a lot of attention. Multimedia workloads are known to have a high degree of variability. Therefore, designs based on a worst-case analysis of such workloads tend of be overly pessimistic. We address this issue by introducing a new concept called *approximate variability characterization curves* (or Approximate VCCs), to characterize the "average-case" behavior of multimedia workloads in a parameterized fashion. Since most multimedia applications only have soft real-time constraints, it is often possible to tolerate a small amount of performance degradation. By allowing such small degradations in the performance, large amounts of resource savings are possible. The concept of Approximate VCCs that we present in this paper allows a designer to quantitatively account for the performance degradation and the associated resource savings. We illustrate this using two typical system design cases.

Keywords: Multimedia, Workload, System-level design

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DAC05, pages 254-259

Modular Domain-Specific Implementation and Exploration Framework for Embedded Software Platforms

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ABSTRACT

This paper focuses on designing network processing software for embedded processors. Our design flow *CRACC* represents an efficient path to implementation based on a modular application description, while avoiding much of the overhead of existing component-based techniques. We illustrate results for a real-world application implementing a full IP-based DSL Access Multiplexer (IP-DSLAM) system. We quantify overhead and optimization potential incurred by our modular implementation. We also point out how CRACC can be deployed for HW-SW partitioning and design space exploration.

Keywords: Software Development, Programmable Platforms, Design Space Exploration, DSLAM, Network Processing

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DAC05, pages 260-265

Simulation Based Deadlock Analysis for System Level Designs

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ABSTRACT
In the design of highly complex, heterogeneous, and concurrent systems, deadlock detection and resolution remains an important issue. In this paper, we systematically analyze the synchronization dependencies in concurrent systems modeled in the Metropolis design environment, where system functions, high level architectures and function-architecture mappings can be modeled and simulated. We propose a data structure called the dynamic synchronization dependency graph, which captures the runtime (blocking) dependencies. A loop-detection algorithm is then used to detect deadlocks and help designers quickly isolate and identify modeling errors that cause the deadlock problems. We demonstrate our approach through a real world design example, which is a complex functional model for video processing and a high level model of function-architecture mapping.
Keywords: simulation, deadlock, synchronization, cyclic dependency, system level, Metropolis

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DAC05, pages 266-269

Fault and Energy-Aware Communication Mapping with Guaranteed Latency for Applications Implemented on NoC

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ABSTRACT

As feature sizes shrink, transient failures of on-chip network links become a critical problem. At the same time, many applications require guarantees on both message arrival probability and response time. We address the problem of transient link failures by means of temporally and spatially redundant transmission of messages, such that designer-imposed message arrival probabilities are guaranteed. Response time minimisation is achieved by a heuristic that statically assigns multiple copies of each message to network links, intelligently combining temporal and spatial redundancy. Concerns regarding energy consumption are addressed in two ways. Firstly, we reduce the total amount of transmitted messages, and, secondly, we minimise the application response time such that the resulted time slack can be exploited for energy savings through voltage reduction. The advantages of the proposed approach are guaranteed message arrival probability and guaranteed worst case application response time.

General Terms: Algorithms, Performance

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DAC05, pages 270-273

High Performance Computing on Fault-Prone Nanotechnologies: Novel Microarchitecture Techniques Exploiting Reliability-Delay Trade-offs

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ABSTRACT
Device and interconnect fabrics at the nanoscale will have a density of defects and susceptibility to transient faults far exceeding those of current silicon technologies. In this paper we introduce a new performance optimization dimension at the microarchitecture level which can mitigate overheads introduced by fault tolerance. This is achieved by directly exposing reliability versus delay design trade-offs while incorporating novel forms of speculation which use faster but less reliable versions of a microarchitecture's performance critical components. Based on a parameterized microarchitecture, we exhibit the benefits of optimizing these tradeoffs.
Keywords: Nanotechnologies, Fault Tolerant Microarchitectures, Performance Optimization, Reliability-Delay Trade-offs

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How to Determine the Necessity for Emerging Solutions

Chair: *Nic Mokhoff* - EE Times, Manhasset, NY
Speakers: *Kamalesh N. Ruparel* - Cisco Systems, Inc., San Jose, CA
Hao Nham - eSilicon Corp., Bedminister, NJ
Francesco Pessolano - Philips Semiconductors, Eindhoven, Netherlands
Kee Sup Kim - Intel Corp., Sacramento, CA

Abstract
Different applications for today's chips require different type of optimizations and thus the need to adopt emerging products and solutions to meet such requirements. Optimizing for low power, for high yield, for reduced soft error or minimal bring up time necessitate adequate trade-off analysis and technical/business decision making by management. The lead managers in this session will discuss today's emerging solutions and their economic impact.

DAC05, pages 275-280

Closing the Power Gap between ASIC and Custom: An ASIC Perspective

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ABSTRACT

We investigate differences in power between application-specific integrated circuits (ASICs) and custom integrated circuits, with examples from 0.6um to 0.13um CMOS. A variety of factors cause synthesizable designs to consume ×3 to ×7 more power. We discuss the shortcomings of typical synthesis flows, and changes to tools and standard cell libraries needed to reduce power. Using these methods, we believe that the power gap between ASICs and custom circuits can be closed to within ×2.

Keywords: ASIC, comparison, custom, energy, power, standard cell

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Explaining the Gap Between ASIC and Custom Power: A Custom Perspective

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ABSTRACT

Power dissipation is now both a key constraint and an application driver in VLSI systems. For a specific application, the energy efficiency of different implementations can differ by multiple orders of magnitude. This work surveys a range of techniques available to improve energy efficiency and highlights their cumulative benefit. Understanding, adopting and adapting selected techniques from full-custom solutions can help bridge the efficiency gap for the ASIC designs. Architecture and microarchitecture choices yield multiple-order of magnitude improvements in power dissipation by matching the structure of the design to the structure of the application and by providing multiple operating and power-down modes. The combination of methodology and full-custom circuit techniques and libraries provide benefits primarily due to reduced parasitic loading enabling the improved performance to be translated into the potential for factor-of-3 to factor-of-10 improvements in power.

Keywords: ASIC, Custom Circuits, EDA, Energy Efficiency, Low Power, Normalized Metrics, Technology Scaling

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DAC05, pages 285-288

Keeping Hot Chips Cool

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ABSTRACT

With 90nm CMOS in production and 65nm testing in progress, power has been pushed to the forefront of design metrics. This paper will outline practical techniques that are used to reduce both leakage as well as active power in a standard-cell library based high-performance design flow. We will discuss the design and cost issues for using different power saving techniques such as: power gating to reduce leakage, multiple and hybrid threshold libraries for leakage reduction and multiple supply voltage based design. In addition techniques to reduce clock tree power will be presented as power consumed in clocks accounts for a significant portion of total chip power. Practical aspects of implementing these techniques will also be discussed.

Keywords: Low power, High-Performance, VLSI Design

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DAC05, pages 289-290

Interconnects Are Moving From MHz->GHz Should you be afraid? Or… "My Giga Hertz, Does Yours?"

Chair: *Rick Merritt* - EE Times, San Mateo, CA
Panelists: *John F. D'Ambrosia* - Tyco Electronics Corp., Harrisburg, PA
Adam Healey - Agere Systems, Inc., Allentown, PA
Boris Litinsky - RF Micro Devices, Inc., San Jose, CA
John Stonick - Synopsys, Inc., Hillsboro, OR
Joe Abler - IBM Corp., Research Triangle Park, NC

PANEL ABSTRACT

Chip interfaces, including standards like PCI Express, are increasingly relying on high-speed serial technology. This move from MHz to GHz brings with it a myriad of chip design challenges that many designers have never faced before. This diverse panel of experts in chip and IP mixed-signal design will describe not only why you SHOULD be afraid (very afraid), but also what's being done to make this transition practical, including new design techniques and standards.

DAC05, pages 291-296

Design Methodology for Wireless Nodes with Printed Antennas

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ABSTRACT

The need for mass-produced inexpensive wireless devices operating under strict energy constraints poses new challenges in the system design methodology. This paper presents a methodology for designing wireless nodes in which a low cost, reliable antenna is realized by printed circuit traces. We show how to combine the analysis from 2.5D and 3D EM simulators with the PCB design tools to create predictable nodes with printed antennas that meet stringent power and data transmission range goals. The presented approach is applied to the design of a IEEE802.15.4 wireless node deployed in several indoor environments.

Keywords: RF CAD, Printed Antenna, Antenna Design Methodology, Printed Circuit Board

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DAC05, pages 297-302

MP Core: Algorithm and Design Techniques for Efficient Channel Estimation in Wireless Applications

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ABSTRACT

Channel estimation and multiuser detection are enabling technologies for future generations of wireless applications. However, sophisticated algorithms are required for accurate channel estimation and multiuser detection, and real-time implementation of these algorithms is difficult. This paper presents architectural design methods for wireless channel estimation which can be leveraged to enable real-time multiuser detection. We redesign the matching pursuit (MP) channel estimation algorithm to reduce the complexity while maintaining the estimation accuracy. Furthermore, we develop a parameterized intellectual property (IP) core, which provides a hardware implementation of the MP algorithm. Experimental results demonstrate the effectiveness and efficiency of the new algorithm and IP core for channel estimation. The implementation of our MP core on a modern, high performance reconfigurable system is about 216 times faster than running the algorithm on a state of the art microprocessor. The MP core possesses the speed required for performing true multiuser detection, enabling future generations of wireless communication applications.

Keywords: Channel estimation, matching pursuit algorithm, design space exploration

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From *Myth* to Methodology: Cross-Layer Design for Energy-Efficient Wireless Communication

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ABSTRACT

During the last decade, wireless communication has seen a trend towards application diversification leading to a significant growth in users. With the availability of – however energy-limited – nomadic devices and real-time multimedia applications, user demand is shifting from simply asking for higher data rates to more complex requirements in terms of Quality of Service (QoS) and energy-efficiency. In this new context energy management is becoming a key success factor. Optimized energy-efficiency requires an energy management that continuously trades off QoS and energy adapting to varying user expectations and environment dynamics. But, QoS can only be evaluated on top of the whole protocol stack while energy consumption largely appears at the lower layers. To minimize overhead during the transitions between layers, we need to address the problem from a cross-layer perspective. We present a methodology that, based on systematic exploration, effective problem partitioning and minimal cross-layer interface, allows energy management in a cross-layer way, while maintaining efficient layered semantics. Different case studies in the context of wireless LAN (WLAN) for multimedia and data traffic transport are discussed, to show how cross-layer energy management can easily be included in systems running state-of-the-art protocols.

Keywords: Cross-layer, Energy Management, Power-aware design

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An Efficient Algorithm for Statistical Minimization of Total Power under Timing Yield Constraints

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ABSTRACT

Power minimization under variability is formulated as a rigorous statistical robust optimization program with a guarantee of power and timing yields. Both power and timing metrics are treated probabilistically. Power reduction is performed by simultaneous sizing and dual threshold voltage assignment. An extremely fast run-time is achieved by casting the problem as a second-order conic problem and solving it using efficient interior-point optimization methods. When compared to the deterministic optimization, the new algorithm, on average, reduces static power by 31% and total power by 17% without the loss of parametric yield. The run time on a variety of public and industrial benchmarks is 30X faster than other known statistical power minimization algorithms.

Keywords: Leakage, manufacturability, statistical optimization

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Robust Gate Sizing by Geometric Programming

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ABSTRACT

We present an efficient optimization scheme for gate sizing in the presence of process variations. Using a posynomial delay model, the delay constraints are modified to incorporate uncertainty in the transistor widths and effective channel lengths due to the process variations. An *uncertainty ellipsoid* method is used to model the random parameter variations. Spatial correlations of intra-die width and channel length variations are incorporated in the optimization procedure. The resulting optimization problem is relaxed to be a Geometric Program and is efficiently solved using convex optimization tools. The effectiveness of our robust gate sizing scheme is demonstrated by applying the optimization on the ISCAS '85 benchmark circuits and testing the optimized circuits by performing Monte Carlo simulations to model the process variations. By varying the size of the uncertainty ellipsoids, a trade-off between area and robustness is explored. Experimental results show that the timing yield of the robustly optimized circuits improves manifold over the traditional deterministically sized circuits. As compared to the worst-case design, the robust gate sizing solution having the same area, has fewer timing violations.

Keywords: Geometric Program, posynomial, uncertainty ellipsoid

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Circuit Optimization using Statistical Static Timing Analysis

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Abstract

In this paper, we propose a new sensitivity based, statistical gate sizing method. Since circuit optimization effects the entire shape of the circuit delay distribution, it is difficult to capture the quality of a distribution with a single metric. Hence, we first introduce a new objective function that provides an effective measure for the quality of a delay distribution for both ASIC and high performance designs. We then propose an efficient and exact sensitivity based pruning algorithm based on a newly proposed theory of perturbation bounds. A heuristic approach for sensitivity computation which relies on efficient computation of statistical slack is then introduced. Finally, we show how the pruning and statistical slack based approaches can be combined to obtain nearly identical results compared with the brute-force approach but with an average run-time improvement of up to 89x. We also compare the optimization results against that of a deterministic optimizer and show an improvement up to 16% in the 99-percentile circuit delay and up to 31% in the standard deviation for the same circuit area.

General Terms: Algorithms, performance, reliability, optimization

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An Exact Jumper Insertion Algorithm for Antenna Effect Avoidance/Fixing

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ABSTRACT
As the process technology enters the nanometer era, reliability has become a major concern in the design and manufacturing of VLSI circuits. In this paper we focus on one reliability issue—jumper insertion in routing trees for avoiding/fixing antenna effect violations at the routing/post-layout stages. We formulate the jumper insertion for antenna avoidance/fixing as a tree-cutting problem. We show that the tree-cutting problem exhibits the properties of optimal substructures and greedy choices. With these properties, we present an $O(V \lg V)$-time exact jumper insertion algorithm that uses the optimum number of jumpers to avoid/fix the antenna violations in a routing tree with V vertices. Experimental results show the superior effectiveness and efficiency of our algorithm.

Keywords: Antenna Effect, Jumper Insertion

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Fine-grained Application Source Code Profiling for ASIP Design

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ABSTRACT
Current Application Specific Instruction set Processor (ASIP) design methodologies are mostly based on iterative architecture exploration that uses Architecture Description Languages (ADLs) and retargetable software development tools. However, for improved design efficiency, additional pre-architecture exploration tools are required to help narrow-down the huge design space and making coarsegrained Instruction Set Architecture (ISA) decisions before detailed ADL modeling. Extensive application code profiling is the key in such early design stages. Based on a novel code instrumentation technology, we present a *microprofiling* approach that fills the current gap between sourcelevel and instruction-level profilers and combines their advantages w.r.t. speed and accuracy. We show how the microprofiler is embedded into an advanced ASIP design flow and justify its use in a case study to design an MP3 decoder ASIP.
Keywords: Customizable Processors, ASIPs, Profiling, Codesign

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Physically-Aware HW-SW Partitioning for Reconfigurable Architectures with Partial Dynamic Reconfiguration

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ABSTRACT

Many reconfigurable architectures offer partial dynamic configurability, but current system-level tools cannot guarantee feasible implementations when exploiting this feature. We present a physically aware hardware-software (HW-SW) scheme for minimizing application execution time under HW resource constraints, where the HW is a reconfigurable architecture with partial dynamic reconfiguration capability. Such architectures impose strict placement constraints that lead to implementation infeasibility of even optimal scheduling formulations that ignore the nature of these constraints. We propose an exact and a heuristic formulation that simultaneously partition, schedule, and do linear placement of tasks on such architectures. With our exact formulation, we prove the critical nature of placement constraints. We demonstrate that our heuristic generates high-quality schedules by comparing the results with the exact formulation for small tests and a popular, but placementuanaware scheduling heuristic for larger tests. With a case study, we demonstrate extension of our approach to handle heterogenous architectures with specialized resources distributed between general purpose programmable logic columns. The execution time of our heuristic is very reasonable- task graphs with hundreds of nodes are processed in a couple of minutes.

Keywords: HW-SWpartitioning, partial dynamic reconfiguration, linear placement

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Performance Simulation Modeling for Fast Evaluation of Pipelined Scalar Processor by Evaluation Reuse

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ABSTRACT

This paper proposes a rapid and accurate evaluation scheme for cycle counts of a pipelined processor using evaluation reuse technique. Since exploration of an optimal processor is a time-consuming task due to large design space, fast evaluation methodology for an architecture is crucial. We introduce the performance simulation model which can evaluate the performance without considering the functional correctness. This model has an FSM-like form and can afford to take all hazard types of pipelined architectures into consideration. The proposed approach is based on the property that an application program, especially multimedia application, has many iterative loops in general. This property invokes many iterative operations in the simulation. Evaluation reuse scheme can alleviate redundantly iterative operations of conventional simulators in the loop. A performance simulator for the pipeline architecture has been developed through which greater speedup has been made compared with other approaches in the evaluation of cycle counts.

Keywords: Retargetable simulation, compiled simulation, evaluation reuse, instruction set architecture, trace-driven simulation

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Trace-Driven HW/SW Cosimulation Using Virtual Synchronization Technique

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ABSTRACT

Poor performance of HW/SW cosimulation is mainly caused by synchronization requirement between component simulators. Virtual synchronization technique was proposed to remove the need of synchronization in cycle accurate cosimulation. But the previous execution-driven simulation based on virtual synchronization has limitations in the application area. In this paper, we propose a novel trace-driven HW/SW cosimulation using virtual synchronization technique. Through OS modeling and channel modeling, the proposed cosimulation technique could be applied more widely while improving the simulation performance further. Experiments with a DIVX player example prove the viability of the proposed technique.

Keywords: Trace-driven cosimulation, virtual synchronization

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DAC05, pages 349-350

The Titanic: What Went Wrong!

Organizer: *Sani R. Nassif* – IBM Research, Austin, TX

Abstract
We often hear about success stories in EDA. We are all justifiably proud of the impact we collectively make on the overall integrated circuit design and manufacturing machine. It is fair to say, however, the one learns far more from failure than one does from success. In this special session we found several brave practitioners who are willing to talk about problems in businessas-usual EDA. These problems include technology related issues; reliability related issues, power issues and even methodology issues – In short, covering a wide swatch of the EDA domain.

Metal Variation-Induced Hold Time Failures
Author: Paul S. Zuchowski - IBM, Burlington, VT

Design for Reliability: acknowledging aging effects
Authors: Claude Moughanni, Mohamed Moosa, Gary Anderson - Freescale, Austin, TX

Bridging the Power Reduction & Estimation Gap in the Cell Processor Design Methodology
Author: Stephen D Posluszny - IBM, Austin, TX

A Series of Unfortunate Events
Author: Ward Vercruysse - AMD, Austin, TX

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Wireless Platforms: GOPS for Cents and MilliWatts

Chair: Jan Rabaey - UC Berkeley, Berkeley, CA
Panelists: Allan Cox - 3Plus1 Technology, Inc., Saratoga, CA
Frank Lane - Flarion Technolgies, Inc., Bedminster, NJ
Rudi Lauwereins – IMEC, Belgium
Ulrich Ramacher - Infineon Technologies AG, Muenchen, Germany
David Witt - Texas Instruments, Dallas, TX

PANEL SUMMARY

In recent years, data communication has overtaken voice as the main force behind the growth in wireless. With this has come a proliferation of standards ranging from wide area networks at one end of the spectrum to personal area networks on the other end. The opportunities offered by this truly ubiquitous connectivity are tremendous, and are leading to revolutionary chances in the way computer, communication, and consumer systems operate and interact.

Providing the necessary flexibility to seamlessly interact with the multitude of emerging network models, as well as the muscle to support the demanding multimedia functionality in a mobile environment, presents some huge challenges to the developer of the wireless implementation platforms. The power budget of the mobile terminal is typically fixed by size considerations and operation time. Cost considerations further constrain the solution space.

In response to these challenges, many solutions have been floated and experimented with ranging from multi-processor architectures, advanced DSPs, reconfigurable solutions and hardwired accelerators. While these innovations break new ground in the world of embedded architectures, many questions emerge such as efficiency, flexibility and programming model. This panel will presents a “bake-off” between a number of solutions that have emerged over the recent years.
Keywords: Wireless architectures, data communications, implementation platforms

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Design Methodology for IC Manufacturability Based on Regular Logic-Bricks

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ABSTRACT

Implementing logic blocks in an integrated circuit in terms of repeating or regular geometry patterns [6,7] can provide significant advantages in terms of manufacturability and design cost [2]. Various forms of gate and logic arrays have been recently proposed that can offer such pattern regularity to reduce design risk and costs [2,4,9,11,12]. In this paper, we propose a full-mask-set design methodology which provides the same physical design coherence as a configurable array, but with area and other design benefits comparable to standard cell ASICs. This methodology is based on a set of simple logic primitives that are mapped to a set of *logic bricks* that are defined by a restrictive set of RET(Resolution Enhancement Technique)-friendly geometry patterns. We propose a design methodology to explore trade-offs between the number of bricks and associated level of configurability versus the required silicon area. Results are shown to compare a design implemented with a small number of regular bricks to an implementation based on a full standard cell library in a 90nm CMOS technology.

Keywords: Integrated Circuits, Regularity, Manufacturability, RET

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Advanced Timing Analysis Based on Post-OPC Extraction of Critical Dimensions

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ABSTRACT

While performance specifications are verified before sign-off for a modern nanometer scale design, extensive application of optical proximity correction substantially alters the layout introducing systematic variations to the simulated and verified performance. As a result, actual on-silicon chip performance is quite different from sign-off expectations. This paper presents a new methodology to provide better estimates of on-silicon performance. The technique relies on the extraction of residual OPC errors from placed and routed full chip layouts to derive actual (i.e., calibrated to silicon) CD values that are then used in timing analysis and speed path characterization. This approach is applied to a state-of-the-art microprocessor and contrasted with traditional design flow practices where ideal (i.e., drawn) Lgate values are employed, leading to a subsequent lack of predictive power. We present a platform for diagnosing and improving OPC quality on gates with specific functionality such as critical gates or matching transistors. Furthermore, with more accurate timing analysis we highlight the necessity of a post-OPC verification embedded design flow, by showing substantial differences in the Si-based timing simulations in terms of significant reordering of speed path criticality and a 36.4% increase in worst-case slack. Extensions of this methodology to multi-layer extraction and timing characterization are also proposed.

Keywords: OPC, layout, process CD, design flow

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Self-Compensating Design for Focus Variation

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ABSTRACT
Process variations have become a bottleneck for predictable and high-yielding IC design and fabrication. Linewidth variation (ΔL) due to defocus in a chip is largely systematic after the layout is completed, i.e., dense lines "smile" through focus while isolated (iso) lines "frown". In this paper, we propose a design flow that allows explicit compensation of focus variation, either within a cell (self-compensated cells) or across cells in a critical path (self-compensated design). Assuming that iso and dense variants are available for each library cell, we achieve designs that are more robust to focus variation. Design with a self-compensated cell library incurs ~11-12% area penalty while compensating for focus variation. Across-cell optimization with a mix of dense and iso cell variants incurs ~6-8% area overhead compared to the original cell library, while meeting timing constraints across a large range of focus variation (from 0 to 0.4um). A combination of original and iso cells provides an even better self-compensating design option, with only 1% area overhead. Circuit delay distributions are tighter with self-compensated cells and self-compensated design than with a conventional design methodology.
Keywords: Variation, Layout, Focus, ACLV, Manufacturability, Compensation

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DAC05, pages 369-372

RADAR: RET-Aware Detailed Routing Using Fast Lithography Simulations

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ABSTRACT

This paper attempts to reconcile the growing interdependency between nanometer lithography and physical design. We first introduce the concept of lithography hotspots and the edge placement error (EPE) map to measure the overall printability and manufacturing effort. We then adapt fast lithography simulation models to generate EPE map. Guided by EPE map, we develop effective RET-aware detailed routing (RADAR) techniques that can handle full-chip capacity to enhance the overall printability while maintaining other design closure. RADAR is implemented in an industry strength detailed router, and tested using some 65nm designs. Our experimental results show that we can achieve up to 40% EPE reduction with reasonable CPU time.

Keywords: DFM, RET, OPC, detailed routing, lithography

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BDD Representation for Incompletely Specified Multiple-Output Logic Functions and Its Applications to Functional Decomposition

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ABSTRACT

A multiple-output function can be represented by a binary decision diagram for characteristic function (BDD for CF). This paper presents a new method to represent multiple-output incompletely specified functions using BDD for CF. An algorithm to reduce the widths of BDD for CFs is presented. This method is useful for decomposition of incompletely specified multiple-output functions. Experimental results for radix converters, adders and a multiplier show that this method is useful for the synthesis of LUT cascades. This data structure is also useful to three-valued logic simulation.

Keywords: Incompletely Specified Function, BDD, Characteristic function, Cascade, Code converter

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DAC05, pages 379-384

A New Canonical Form for Fast Boolean Matching in Logic Synthesis and Verification

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Abstract

An efficient and compact canonical form is proposed for the Boolean matching problem under permutation and complementation of variables. In addition an efficient algorithm for computing the proposed canonical form is provided. The efficiency of the algorithm allows it to be applicable to large complex Boolean functions with no limitation on the number of input variables as apposed to previous approaches, which are not capable of handling functions with more than seven inputs. Generalized signatures are used to define and compute the canonical form while symmetry of variables is used to minimize the computational complexity of the algorithm. Experimental results demonstrate the efficiency and applicability of the proposed canonical form.

General Terms: Algorithms, Design, Verification

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DAC05, pages 385-390

Effective Bounding Techniques For Solving Unate and Binate Covering Problems

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ABSTRACT

Covering problems arise in many areas of electronic design automation such as logic minimization and technology mapping. An exact solution can critically impact both size and performance of the devices being designed. This paper introduces *eclipse*, a branch-and-bound solver that can solve many covering problems orders of magnitude faster than existing solvers. When used in place of the default covering engine of a well-known logic minimizer, *eclipse* makes it possible to find, in less than six minutes, true minima for three benchmark problems that have eluded exact solutions for more than a decade.

Keywords: covering, branch and bound, satisfiability, unate, binate

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Operator-based Model-Order Reduction of Linear Periodically Time-Varying Systems

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ABSTRACT

Linear periodically time-varying (LPTV) abstractions are useful for a variety of communication and computer subsystems. In this paper, we present a novel operator-based model-order reduction (MOR) algorithmfor reducing large LPTVsystems to smaller ones, a capability useful for system-level performance analysis. Our procedure is based on generalizing existing matrix-based Krylov-subspace algorithms to arbitrary function-space operators. Practical benefits of our approach include significantly enhanced algorithm and code modularity, compared to previous LPTV-MOR approaches based on a-priori discretization. We demonstrate the use of the proposed technique on several circuit examples.

Keywords: LPTV systems, model-order reduction, operator, modularity

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DAC05, pages 397-402

Simulation of the Effects of Timing Jitter in Track-and-Hold and Sample-and-Hold Circuits

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ABSTRACT
In this paper, we analyze the effect of jitter in track and hold circuits. The output spectrum is obtained in terms of the system function of the track and hold. It is a fairly general model in which the effect of input as well as clock jitter can be included. The clock can have an arbitrary duty cycle, so that the circuit could also approximate a sample and hold. Using this model, it is possible to simulate the effects of jitter in a track and hold using a standard circuit simulator. Three cases are analyzed - long term jitter, correlated jitter with exponential autocorrelation and white noise jitter. These results are verified using Monte Carlo simulations.
Keywords: Jitter, Sampling circuits

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Scalable Trajectory Methods for On-Demand Analog Macromodel Extraction

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ABSTRACT

Trajectory methods sample the state trajectory of a circuit as it simulates in the time domain, and build macromodels by reducing and interpolating among the linearizations created at a suitably spaced subset of the time points visited during training simulations. Unfortunately, moving from simple to industrial circuits requires more extensive training, which creates models too large to interpolate efficiently. To make trajectory methods practical, we describe a scalable interpolation architecture, and the first implementation of a complete trajectory "infrastructure" inside a full SPICE engine. The approach supports arbitrarily large training runs, automatically prunes redundant trajectory samples, supports limited hierarchy, enables incremental macromodel updates, and gives 3-10X speedups for larger circuits.

Keywords: Circuit, trajectory method, analog, macromodel, SPICE

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DAC05, pages 409-412

Cognitive Radio Techniques for Wide Area Networks

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ABSTRACT

The cellular wireless market has begun the transition to data centric services including high speed internet access, video, high quality audio, and gaming. Communications technology can meet the need for very high data link speeds, and can also improve network throughput, but dramatically more spectrum will be needed to provide ubiquitous wireless data service. Cognitive radio is a new technology that allows spectrum to be dynamically shared between users. It offers the potential to dramatically change the way spectrum is used in systems and to substantially increase the amount of spectrum available for wireless communications. This paper introduces cognitive radio and explains the promise, possible operating modes, and benefits it may offer.

Keywords: Cognitive radios, unlicensed spectrum, unlicensed wide area network

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DAC05, pages 413-415

MIMO Technology for Advanced Wireless Local Area Networks

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ABSTRACT

This paper first gives a brief introduction to Multiple Input Multiple Output (MIMO) wireless communication systems. Various architectures of MIMO systems and corresponding features are discussed, including those proposed for the IEEE 802.11n standard. The impact on chip area and required data processing rates is then presented.

Keywords: MIMO, 802.11n, Wireless, Networking

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RF MEMS in Wireless Architectures

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ABSTRACT

Micromechanical (or "μmechanical") communication circuits fabricated via IC-compatible MEMS technologies and capable of low-loss filtering, mixing, switching, and frequency generation, are described with the intent to miniaturize wireless transceivers. Possible MEMS-based receiver front-end architectures are then presented that use these micromechanical circuits in large quantities to enhance robustness and substantially reduce power consumption. Among the more aggressive architectures proposed are one based on a μmechanical RF channel-selector and one featuring an all-MEMS RF front-end.

Keywords: RF MEMS, quality factor, micromechanical circuit, RF front end, resonator, switch, inductor, capacitor

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DAC05, pages 421-426

Multiplexer Restructuring for FPGA Implementation Cost Reduction

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ABSTRACT

This paper presents a novel synthesis algorithm that reduces the area needed for implementing multiplexers on an FPGA by an average of 18%. This is achieved by reducing the number of Lookup Tables (LUTs) needed to implement multiplexers. The algorithm relies on reimplementing 2:1 multiplexer trees using efficient 4:1 multiplexers. The key to the algorithm's performance lies in exploiting the observation that most multiplexers occur in busses. New optimizations are employed which pay a small cost in logic that is shared across the bus to achieve a reduction in the logic required for every bit of the bus.

Keywords: FPGA, Multiplexers, Restructuring, Recoding, Busses, Logic Optimization, Synthesis

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FPGA Technology Mapping: A Study of Optimality

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ABSTRACT
This paper attempts to quantify the optimality of FPGA technology mapping algorithms. We develop an algorithm, based on Boolean satisfiability (SAT), that is able to map a small subcircuit into the smallest possible number of lookup tables (LUTs) needed to realize its functionality. We iteratively apply this technique to small portions of circuits that have already been technology mapped by the best available mapping algorithms for FPGAs. In many cases, the optimal mapping of the subcircuit uses fewer LUTs than is obtained by the technology mapping algorithm. We show that for some circuits the total area improvement can be up to 67%.

Keywords: Boolean Satisfiability, Resynthesis, Optimization, Cone, FPGA, Lookup Table

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DAC05, pages 433-438

Incremental Retiming for FPGA Physical Synthesis

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ABSTRACT

In this paper, we present a new linear-time retiming algorithm that produces near-optimal results. Our implementation is specifically targeted at Altera's Stratix [1] FPGA-based designs, although the techniques described are general enough for any implementation medium. The algorithm is able to handle the architectural constraints of the target device, multiple timing constraints assigned by the user and implicit legality constraints. It ensures that register moves do not create asynchonous problems such as creating a glitch on a clock/reset signal.

Keywords: Retiming, Physical Synthesis, FPGA

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Architecture-Adaptive Range Limit Windowing for Simulated Annealing FPGA Placement

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ABSTRACT

Previous research has shown both theoretically and practically that simulated annealing can greatly benefit from the incorporation of an adaptive range limiting window to control the acceptance ratio of swaps during placement. However, the implementation of such a system is not necessarily obvious. Existing range limiting techniques have several fundamental shortcomings when dealing with both standard island-style FPGAs and more exotic architectures. In this paper we discuss the nature of these problems and present a new algorithm that attempts to deal with these issues.

Keywords: Reconfigurable logic, placement, simulated annealing, windowing, range limiting, architecture-adaptive

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Word Level Predicate Abstraction and Refinement for Verifying RTL Verilog

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ABSTRACT

Model checking techniques applied to large industrial circuits suffer from the state space explosion problem. A major technique to address this problem is abstraction. The most commonly used abstraction technique for hardware verification is localization reduction, which removes latches that are not relevant to the property. However, localization reduction fails to reduce the size of the model if the property actually depends on most of the latches. This paper proposes to use predicate abstraction for verifying RTL Verilog, a technique successfully used for software verification. The main challenge when using predicate abstraction is the discovery of suitable predicates. We propose to use weakest preconditions of Verilog statements in order to obtain new predicates during abstraction refinement. This technique has not been applied to circuits before. On benchmarks taken from an industrial microprocessor, we successfully verified safety properties with more than 32,000 latches in the cone of influence. We compare the performance of our technique with a modern model checker that implements localization reduction.

Keywords: Predicate Abstraction, Verilog, SAT

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Structural Search for RTL with Predicate Learning

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ABSTRACT

We present an efficient search strategy for satisfiability checking on circuits represented at the register-transfer-level (RTL). We use the RTL circuit structure by extending concepts from classic automatic test-pattern generation (ATPG) algorithms and interval-arithmetic to guide the search process. We extend the idea of Boolean recursive learning on predicate logic in the RTL using Boolean and interval constraint propagation in the control and data-path of the circuit. This is used as a pre-processing step to derive relations between predicate logic signals that are used to augment the search. We demonstrate experimentally that these methods provide significant improvement over current techniques on sample benchmarks.

Keywords: Interval Arithmetic, Learning, Predicate Abstraction, Satisfiability

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Normalization at the Arithmetic Bit Level

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ABSTRACT

We propose a normalization technique for verifying arithmetic circuits in a bounded model checking environment. Our technique operates on the *arithmetic bit level (ABL) description* of the arithmetic circuit parts and the property. The ABL description can easily be provided by the front-end of an RTL property checker. The proposed normalization greatly simplifies the SAT instances to be solved for arithmetic circuit verification. Our approach has been applied successfully to verify the integer pipeline of an industrial microprocessor with advanced DSP capabilities.

Keywords: Property checking, arithmetic bit level normalization, SAT

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Exploiting Suspected Redundancy without Proving It

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ABSTRACT

We present several improvements to general-purpose sequential redundancy removal. **(1)** We propose using a robust variety of synergistic transformation and verification algorithms to process the individual proof obligations. This enables greater speed and scalability, and identifies a significantly greater degree of redundancy, than prior approaches. **(2)** We generalize upon traditional redundancy removal and utilize the speculatively-reduced model to enhance bounded search, without needing to complete any proofs.

Keywords: sequential redundancy removal, sequential equivalence checking, correctness-preserving transformations

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Multi-threaded Reachability

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ABSTRACT
Partitioned BDD-based algorithms have been proposed in the literature to solve the memory explosion problem in BDD-based verification. Such algorithms can be at times ineffective as they suffer from the problem of scheduling the relative order in which the partitions are processed. In this paper we present a novel multi-threaded reachability algorithm that avoids this scheduling problem while increasing the latent parallelism in partitioned state space traversal. We show that in most cases our method is significantly faster than both the standard reachability algorithm as well as the existing partitioned approaches. The gains are further magnified when our threaded implementation is evaluated in the context of a parallel framework.
Keywords: Reachability Analysis, Parallel, Multi-threaded

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Automatic Generation of Customized Discrete Fourier Transform IPs

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ABSTRACT

This paper presents a parameterized soft core generator for the discrete Fourier transform (DFT). Reusable IPs of digital signal processing (DSP) kernels are important time-saving resources in DSP hardware development. Unfortunately, reusable IPs, however optimized, can introduce inefficiencies because they cannot fit the exact requirements of every application context. Given the well-understood and regular computation in DSP kernels, an automatic tool can generate high-quality ready-to-use IPs customized to user-specified cost/performance tradeoffs (beyond basic parameters such as input size and data format). The paper shows that the generated DFT cores can match closely the performance and cost of DFT cores from the Xilinx LogiCore library. Furthermore, the generator can yield DFT cores over a range of different performance/cost tradeoff points that are not available from the library.

Keywords: Discrete Fourier transform, IP, design generator, FPGA

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Race-Condition-Aware Clock Skew Scheduling

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ABSTRACT

The race conditions often limit the smallest feasible clock period that the optimal clock skew scheduling can achieve. Therefore, the combination of clock skew scheduling and delay insertion (for resolving the race conditions) may lead to further clock period reduction. However, the interactions between clock skew scheduling and delay insertion have not been well studied. In this paper, we provide a fresh viewpoint to look at this problem. A novel approach, called race-condition-aware (RCA) clock skew scheduling, is proposed to determine the clock skew schedule by taking the race conditions into account. Our objective is not only to optimize the clock period, but also to heuristically minimize the required inserted delay. Compared with previous work, our approach has significant improvement in the time complexity.

Keywords: High performance, Sequential circuits, Timing optimization

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A Novel Synthesis Approach for Active Leakage Power Reduction Using Dynamic Supply Gating

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Abstract:
Due to exponential increase in subthreshold leakage with technology scaling and temperature increase, leakage power is becoming a major fraction of total power in the active mode. We present a novel low-cost design methodology with associated synthesis flow for reducing both switching and active leakage power using dynamic supply gating. A logic synthesis approach based on Shannon expansion is proposed that dynamically applies supply gating to idle parts of general logic circuits even when they are performing useful computation. Experimental results on a set of MCNC benchmark circuits in a predictive 70nm process exhibits improvements of 15% to 88% in total active power compared to the results obtained by a conventional optimization flow.

General Terms: Algorithms, Design, Performance

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DAC05, pages 485-490

Designing Logic Circuits for Probabilistic Computation in the Presence of Noise

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ABSTRACT

As Si CMOS devices are scaled down into the nanoscale regime, current computer architecture approaches are reaching their practical limits. Future nano-architectures will confront devices and interconnections with a large number of inherent defects, which motivates the search for new architectural paradigms. In this paper, we examine probabilistic-based design methodologies for nanoscale computer architectures based onMarkov random fields (MRF). The MRF approach can express arbitrary logic circuits and the logic operation is achieved by maximizing the probability of correct state configurations in the logic network depending on the interaction of neighboring circuit nodes. The computation proceeds via probabilistic propagation of states through the circuit. Crucially, the MRF logic can be implemented in modified CMOS-based circuitry that trades off circuit area and operation speed for the crucial fault tolerance and noise immunity. This paper builds on the recent demonstration that significant immunity to faulty individual devices or dynamically occurring signal errors can be achieved by the propagation of state probabilities over an MRF network. In particular, we are interested in CMOS-based circuits that work reliably at very low supply voltages (V_{DD} = 0.1–0.2 V), where standard CMOS would fail due to thermal and crosstalk noise, and transistor threshold variation. In this paper, we present results for simulated probabilistic test circuits for elementary logic components and well as small circuits taken from the MCNC91 benchmark suite and we show greatly improved noise immunity operating at very low V_{DD}. The MRF framework extends to all levels of a design, where formally optimum probabilistic computation can be implemented as a natural element of the processing structure.

Keywords: noise immunity, reliability, subthreshold operation, probabilistic computing, Markov random fields, nanodevices

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DAC05, pages 491-496

A Lattice-Based Framework for the Classification and Design of Asynchronous Pipelines

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ABSTRACT

This paper presents a unifying framework for the modeling of asynchronous pipeline circuits. A pipeline protocol is captured in a graph-based model which defines the partial ordering of both its control and data events. The relationship between an entire space of different protocols is then captured in a semi-lattice, which has well-defined top and bottom elements, corresponding to the most concurrent and least concurrent protocol variants, respectively. This framework also provides a set of correct-by-construction transformation rules which allows for the systematic exploration of the entire design space by their successive application. To the best of our knowledge, this is the first formal framework for asynchronous pipelines which can capture protocols from a variety of logic style families, including both dynamic and static. It is also the first to provide a formal foundation for the design-space exploration of asynchronous pipelines.

Keywords: pipeline, framework, asynchronous, digital design, protocols

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DAC05, pages 497-502

Power Optimal Dual-V_{dd} Buffered Tree Considering Buffer Stations and Blockages

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ABSTRACT

This paper presents the first in-depth study on applying dual V_{dd} buffers to buffer insertion and multi-sink buffered tree construction for power minimization under delay constraint. To tackle the problem of dramatic complexity increment due to simultaneous delay and power consideration and increased buffer choices, we develop a sampling-based sub-solutions (i.e. options) propagation method and a balanced search tree-based data structure for option pruning. We obtain 17x speedup with little loss of optimality compared to the exact option propagation. Moreover, compared to buffer insertion with single V_{dd} buffers, dual-V_{dd} buffers reduce power by 23% at the minimum delay specification. In addition, compared to the delay-optimal tree using single V_{dd} buffers, our power-optimal buffered tree reduces power by 7% and 18% at the minimum delay specification when single V_{dd} and dual V_{dd} buffers are used respectively.

Keywords: Low power, buffer insertion, detail routing

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DAC05, pages 503-508

Net Weighting to Reduce Repeater Counts during Placement

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ABSTRACT

We demonstrate how to use placement to ameliorate the predicted repeater explosion problem caused by poor interconnect scaling. We achieve repeater count reduction by dynamically modifying net weights in a context-sensitive manner during global placement and coarse legalization. Our scheme, which models layer assignment as well as valid inter-repeater distance ranges, can decrease the repeater counts significantly with minimal impact on wirelength.

Keywords: Placement, Net weighting, Force-directed placement, Repeater, Buffering, Scaling, Interconnect

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Path Based Buffer Insertion

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ABSTRACT

Along with the progress of VLSI technology, buffer insertion plays an increasingly critical role on affecting circuit design and performance. Traditional buffer insertion algorithms are mostly net based and therefore often result in sub-optimal delay or unnecessary buffer expense due to the lack of global view. In this paper, we propose a novel path based buffer insertion scheme which can overcome the weakness of the net based approaches. We also discuss some potential difficulties of the path based buffer insertion approach and propose solutions to them. A fast estimation on buffered delay is employed to improve the solution quality. Gate sizing is also considered at the same time. Experimental results show that our method can efficiently reduce buffer/gate cost significantly (by 71% on average) when compared to traditional net based approaches. To the best of our knowledge, this is the first work on path based buffer insertion and simultaneous gate sizing.

Keywords: Buffer Insertion, Interconnect Synthesis, PowerMinimization, Global Routing, Layout, Physical Design

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DAC05, pages 515-520

Diffusion-Based Placement Migration

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ABSTRACT
Placement migration is the movement of cells within an existing placement to address a variety of post-placement design closure issues, such as timing, routing congestion, signal integrity, and heat distribution. To fix a design problem, one would like to perturb the design as little as possible while preserving the integrity of the original placement. This work presents a new diffusion-based placement method based on a discrete approximation to a closed-form solution of the continuous diffusion equation. It has the advantage of smooth spreading, which helps preserve neighborhood characteristics of the original placement. Applying this technique to placement legalization demonstrates significant improvements in wire length and timing compared to other commonly used techniques.
Keywords: Placement Migration, Diffusion, Legalization

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DAC05, pages 521-522

Is Methodology the Highway Out of Verification Hell?

Chair: *Gabe Moretti* - EDA Consultant & Editor, Venice, FL
Panelists: *Harry Foster* - Jasper Design Automation, Mountain View, CA
Janick Bergeron – Synopsys, Ottawa, Canada
Masayuki Nakamura - Sony Corporation, Shinagawa, Japan
Shrenik Mehta - Sun Microsystems, Osaki Shinagawa-Ku, Japan
Laurent Ducousso - ST Microelectronics, Grenoble, France

PANEL SUMMARY

Few would disagree that verification takes the lion's share of today's project resources. If we examine the available research, we quickly discover that verification is a significant pain point that consumes massive amounts of time and resources across a multitude of market segments. Per Gary Smith at Gartner Dataquest, verification consumes 30% to 70% of total schedule, depending on design size. According to Collett International Research, Inc., a majority of ASICs and integrated circuits (ICs) require at least one respin with 71% of respins are due to functional bugs "verification should have caught".

With such statistics, it is easy to understand why many contend that the verification challenge is growing at a double exponential rate (that is, exponential with respect to Moore's law). Given verification's importance and its significant impact on fundamental design quality and time-to-market demands, what is our industry doing in response? This panel explores where the methodology highway is taking us - is the destination heaven or just another level of Dante's inferno?

Respected authors and experts in verification methodology will share their insights and opinions of the two methodologies used today: verify-after-the-fact (traditional) and verify-as-you-design (emerging). For decades, simulation has necessitated a verifyafter-the-fact methodology and yet we can see from the industry research that a high percentage of silicon requires respins. With the latest advances in simulation testbenches and languages, can the verify-after-the-fact approach scale? Or, is it time for a move to a higher level of abstraction that enables a verify-as-you-design methodology?

Industry leading chip and systems companies will discuss the methodologies they employ today to address the enormous challenge of functional verification. Questions to be addressed by our esteemed panelists include: How can we bring in schedules? What can we do to increase design quality? What cultural and organizational changes have to take place to bring quality back to the forefront of design? Where is the measurable proof of quality? What are the questions that managers should be asking themselves? What are the engines being used? What formal techniques deliver the greatest success? How important is HW/SW verification? What are the processes or methodologies being used to overcome tool or technology limitations? What is the value of assertions? How does a geographically dispersed engineering team impact design quality? What are the metrics being used to measure progress and success? And how do you know when you are done?

Today we currently don't design quality in – we TEST it in (using simulation). But, what would happen if quality was designed in from the beginning? How much could we improve the overall quality level and reduce verification time, and what would this take to do it? Finally, can migration to a new methodology be the highway out of verification hell?

Keywords: Verification, methodology, assertions, formal verification

DAC05, pages 523-528

Full-Chip Analysis of Leakage Power Under Process Variations, Including Spatial Correlations

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ABSTRACT

In this paper, we present a method for analyzing the leakage current, and hence the leakage power, of a circuit under process parameter variations that can include spatial correlations due to intra-chip variation. A lognormal distribution is used to approximate the leakage current of each gate and the total chip leakage is determined by summing up the lognormals. In this work, Both subthreshold leakage and gate tunneling leakage are considered. The proposed method is shown to be effective in predicting the CDF/PDF of the total chip leakage. The average errors for mean and sigma values are –1.3% and –4.1%.

General Terms: Algorithm, Design, Performance, Reliability

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Variations-Aware Low-Power Design with Voltage Scaling

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ABSTRACT

We present a new methodology which takes into consideration the effect of Within-Die (WID) process variations on a low-voltage parallel system. We show that in the presence of process variations one should use a higher supply voltage than would otherwise be predicted to minimize the power consumption of a parallel systems. Previous analyses, which ignored WID process variations, provide a lower non-optimal supply voltage which can underestimate the energy/operation by 8.2X. We also present a novel technique to limit the effect of temperature variations in a parallel system. As temperatures increases, the scheme reduces the power increase by 43% allowing the system to remain at it's optimal supply voltage across different temperatures.

Keywords: Process Variations, Parallel Systems, Low-Voltage

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DAC05, pages 535-540

Accurate and Efficient Gate-Level Parametric Yield Estimation Considering Correlated Variations in Leakage Power and Performance

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Abstract

Increasing levels of process variation in current technologies have a major impact on power and performance, and result in parametric yield loss. In this work we develop an efficient gate-level approach to accurately estimate the parametric yield defined by leakage power and delay constraints, by finding the joint probability distribution function (jpdf) for delay and leakage power. We consider inter-die variations as well as intra-die variations with correlated and random components. The correlation between power and performance arise due to their dependence on common process parameters and is shown to have a significant impact on yield in high-frequency bins. We also propose a method to estimate parametric yield given the power/delay jpdf that is much faster than numerical integration with good accuracy. The proposed approach is implemented and compared with Monte Carlo simulations and shows high accuracy, with the yield estimates achieving an average error of 2%.

Keywords: Yield, Variability, Leakage, Correlation

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Leakage Minimization of Nano-Scale Circuits in the Presence of Systematic and Random Variations

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ABSTRACT

This paper presents a novel gate sizing methodology to minimize the leakage power in the presence of process variations. The leakage and delay are modeled as posynomials functions to formulate a geometric programming problem. The existing statistical leakage model of [18] is extended to include the variations in gate sizes as well as systematic variations. We propose techniques to efficiently evaluate constraints on the α-percentile of the path delays without enumerating the paths in the circuit. The complexity of evaluating the objective function is O(|N|2) and that of evaluating the delay constraints is O(|N| + |E|) for a circuit with |N| gates and |E| wires. The optimization problem is then solved using a convex optimization algorithm that gives an exact solution.

Keywords: Leakage, Statistical, Optimization, Geometric Programming

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A 135Mbps DVB-S2 Compliant Codec based on 64800-bit LDPC and BCH Codes (ISSCC Paper 24.3)

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ABSTRACT
A DVB-S2 compliant codec is implemented in both 130nm-8M and 90nm-7M low-leakage CMOS technologies. The system includes encoders and decoders for both Low-Density Parity Check (LDPC) codes and serially concatenated BCH codes. All requirements of the DVB-S2 standard are supported including code rates between 1/4 and 9/10, block sizes of either 16,200 bits or 64,800 bits, and four digital modulation options. The 130nm core design occupies 49.6mm2 and operates at 200MHz, while the 90nm core design occupies 15.8mm2 and operates at 300MHz.
Keywords: DVB-S2, LDPC, FEC (forward error correction)

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A Design Platform for 90-nm Leakage Reduction Techniques

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ABSTRACT
Methodology, EDA Flow, scripts, and documentation plays a tremendous role in the deployment and standardization of advanced design techniques. In this paper we focus not only on leakage reduction techniques but also on their deployment as a worldwide infrastructure as the added-value resides not only in the techniques themselves but also in the way they are implemented to build an efficient, re-usable, robust, low cost and portable platform. Techniques have been silicon proven on the 90-nm TI CMOS technology and is commonly used to design SoC with complexities over 100 Million transistors
Keywords: SoC Design, Leakage Power Management, Wireless Application processor

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A 24 GHz Phased-Array Transmitter in 0.18 μm CMOS

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ABSTRACT

A fully-integrated 4-element phased array transmitter at 24 GHz with on-chip PAs is demonstrated in 0.18μm CMOS. It has a beam-forming resolution of 10°, a peak-to-null ratio of 23 dB, and 28 dB isolation between paths. Each PA can deliver up to +14 dBm into 50 Ω in saturation. The die size is 6.8mm x 2.1mm. The transmitter bandwidth is more than 400MHz and supports up to 1Gbit/s QPSK, facilitating a Gigabit wireless LAN solution.

Keywords: Wireless, Transmitters, Phased-Array, 24GHz, CMOS, IC

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Cache Coherence Support for Non-Shared Bus Architecture on Heterogeneous MPSoCs

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ABSTRACT

We propose two novel integration techniques -- *bypass* and *bookkeeping* -- in the memory controller to address the cache coherence compatibility issue of a non-shared bus heterogeneous MPSoC. The bypass approach is an inexpensive and efficient solution for computation-bound applications while the bookkeeping approach eliminating unnecessary forwarding traffic offers an alternative for bandwidth-limited applications. Our RTOS kernel simulations show up to 6.65x speedup over the conventional software solution.

Keywords: Cache coherence, Inter-processor communication, Heterogeneous MPSoC, Real-time and embedded systems

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DAC05, pages 559-564

A Low Latency Router Supporting Adaptivity for On-Chip Interconnects

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ABSTRACT

The increased deployment of System-on-Chip designs has drawn attention to the limitations of on-chip interconnects. As a potential solution to these limitations, Networks-on-Chip (NoC) have been proposed. The NoC routing algorithm significantly influences the performance and energy consumption of the chip. We propose a router architecture which utilizes adaptive routing while maintaining low latency. The two-stage pipelined architecture uses look ahead routing, speculative allocation, and optimal output path selection concurrently. The routing algorithm benefits from congestion-aware flow control, making better routing decisions. We simulate and evaluate the proposed architecture in terms of network latency and energy consumption. Our results indicate that the architecture is effective in balancing the performance and energy of NoC designs.

Keywords: Networks-On-Chip, Adaptive Routing, Interconnection Networks

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Floorplan-Aware Automated Synthesis of Bus-based Communication Architectures

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ABSTRACT
As System-on-Chip (SoC) designs become more complex, it is becoming harder to design communication architectures to handle the ever increasing volumes of inter-component communication. Manual traversal of the vast communication design space to synthesize a communication architecture that meets performance requirements becomes infeasible. In this paper, we address this problem by proposing an automated approach for synthesizing cost-effective, bus-based communication architectures that satisfy the performance constraints in a design. Our synthesis flow also incorporates a high-level floorplanning and wire delay estimation engine to evaluate the feasibility of the synthesized bus architecture and detect timing violations early in the design flow. We present case studies of network communication SoC subsystems for which we synthesized bus architectures, detected timing violations and generated core placements in a matter of hours instead of several days it took for a manual effort.
Keywords: Communication Synthesis, Systems-on-Chip

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FLEXBUS: A High-Performance System-on-Chip Communication Architecture with a Dynamically Configurable Topology

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ABSTRACT

In this paper, we describe FLEXBUS, a flexible, high-performance on-chip communication architecture featuring a dynamically configurable topology. FLEXBUS is designed to detect run-time variations in communication traffic characteristics, and efficiently adapt the *topology* of the communication architecture, both at the system-level, through *dynamic bridge by-pass*, as well as at the component-level, using *component re-mapping*. We describe the FLEXBUS architecture in detail and present techniques for its run-time configuration based on the characteristics of the on-chip communication traffic. The techniques underlying FLEXBUS can be used in the context of a variety of on-chip communication architectures. In particular, we demonstrate its application to AMBA AHB, a popular commercial on-chip bus. Detailed experiments conducted on the FLEXBUS architecture using a commercial design flow, and its application to an IEEE 802.11 MAC processor design, demonstrate that it can provide significant performance gains as compared to conventional architectures (up to 31.5% in our experiments), with negligible hardware overhead.

Keywords: Communication architectures, On-chip bus

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Trafffic Shaping for an FPGA based SDRAM Controller with Complex QoS Requirements

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ABSTRACT

Today high-end video and multimedia processing applications require huge amounts of memory. For cost reasons, the usage of conventional dynamic RAM (SDRAM) is preferred. However, SDRAM access optimization is a complex task, especially if multi-stream access with different QoS requirements is involved. In [8], a multi-stream DDR-SDRAM controller IP covering combinations of low latency requirements for processor cache access, hard realtime constraints for periodic video signals and hard real-time bursty accesses for video coprocessors was described. To handle these contradictory QoS requirements at high system performance, a combination of a 2-stage scheduling algorithm and static priorities were used. This paper describes an additional flow control which enhances the overall performance. Experiments with an FPGA based high-end video platform demonstrate the superiority of this architecture.

Keywords: SDRAM, memory access, QoS, trafffic shaping, priorities, flow control, FPGA

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Microarchitecture-Aware Floorplanning Using a Statistical Design of Experiments Approach

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ABSTRACT

Since across-chip interconnect delays can exceed a clock cycle in nanometer technologies, it has become essential in high performance designs to add flip-flops on wires with multi-cycle delays. Although such a wire pipelining strategy allows higher operating frequencies, it can reduce the delivered performance of a microarchitecture, since the extra flip-flops inserted may increase the operation latencies and stall cycles. Moreover, the addition of latencies on some wires can have a large impact on the overall performance while other wires are relatively insensitive to additional latencies. This varying sensitivity suggests the need for a throughput-aware strategy for pipelining the interconnects that interacts closely with the physical design step, which determines the lengths of these multicycle wires. We use a statistical design of experiments strategy based on a multifactorial design, which intelligently uses a limited number of simulations to rank the importance of the wires. When applied at the floorplanning level, our results show improvements both in the overall system performance and in the total wire length when compared with an existing technique.

Keywords: Wire pipelining, Microarchitecture, Floorplanning

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Timing-Driven Placement by Grid-Warping

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Abstract

Grid-warping is a recent placement strategy based on a novel physical analogy: rather than move the gates to optimize their location, it elastically deforms a model of the 2-D chip surface on which the gates have been coarsely placed via a standard quadratic solve. In this paper, we introduce a timing-driven grid-warping formulation that incorporates slack-sensitivity-based net weighting. Given inevitable concerns about wirelength and runtime degradation in any timing-driven scheme, we also incorporate a more efficient net model and an integrated local improvement ("rewarping") step. An implementation of these ideas, WARP2, can improve worst-case negative slack by 37% on average, with very modest increases in wirelength and runtime.

Keywords: Algorithms, Placement

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Faster and Better Global Placement by a New Transportation Algorithm

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ABSTRACT
We present BonnPlace, a new VLSI placement algorithm that combines the advantages of analytical and partitioning-based placers. Based on (non-disjoint) placements minimizing the total quadratic netlength, we partition the chip area into regions and assign the circuits to them (meeting capacity constraints) such that the placement is changed as little as possible. The core routine of our placer is a new algorithm for the Transportation Problem that allows to compute efficiently the circuit assignments to the regions. We test our algorithm on a set of industrial designs with up to 3.6 millions of movable objects and two sets of artificial benchmarks showing that it produces excellent results. In terms of wirelength, we can improve the results of leading-edge placement tools by about 5 %.
Keywords: VLSI-Placement, Global Placement, Transportation Problem

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Multilevel Full-Chip Routing for the X-Based Architecture

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ABSTRACT
As technology advances into the nanometer territory, the interconnect delay has become a first-order effect on chip performance. To handle this effect, the X-architecture has been proposed for high-performance integrated circuits. The X-architecture presents a new way of orienting a chip's microscopic interconnect wires with the pervasive use of diagonal routes. It can reduce the wirelength and via count, and thus improve performance and routability. Furthermore, the continuous increase of the problem size of IC routing is also a great challenge to existing routing algorithms. In this paper, we present the first multilevel framework for full-chip routing using the X-architecture. To take full advantage of the X-architecture, we explore the optimal routing for three-terminal nets on the X-architecture and develop a general X-Steiner tree algorithm based on the delaunay triangulation approach for the X-architecture. The multilevel routing framework adopts a two-stage technique of coarsening followed by uncoarsening, with a trapezoid-shaped track assignment embedded between the two stages to assign long, straight diagonal segments for wirelength reduction. Compared with the state-of-the-art multilevel routing for the Manhattan architecture, experimental results show that our approach reduced wirelength by 18.7% and average delay by 8.8% with similar routing completion rates and via counts.
Keywords: Physical design, routing, multilevel optimization, Xarchitecture

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DAC05, pages 603-606

Matlab Extensions for the Development, Testing and Verification of Real-Time DSP Software

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ABSTRACT

The purpose of this paper is to present the required tools for the development, testing and verification of DSP software in Matlab. The paper motivates a DSP Simulator concept that can be combined with the MATLAB executable interface to develop, evaluate and test DSP software within a single environment. Programming guidelines and optimization results are also provided to demonstrate the effectiveness of the intrinsics software development approach.

Keywords: C Intrinsics, Matlab, DSP Software, Optimization, Verification

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DAC05, pages 607-610

Matlab as a Development Environment for FPGA Design

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ABSTRACT

In this paper we discuss an efficient design flow from Matlab® to FPGA. Employing Matlab for algorithm research and as system level language allows efficient transition from algorithm development to implementation. We show that integrating Matlab with HDL design tools such as HDL designer® and Precision-C®, an efficient design flow, suitable for rapid prototyping, can be obtained. The design flow accelerates process of algorithm development and simplifies test-bench formulation and verification process. The overall development time thus can be significantly reduced. We elaborate on the advantages and disadvantages of the design flow. It will be shown that Matlab based design flow generates functional specifications that are useful for RTL development.

Keywords: System Design Flows, Rapid Prototyping

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Should Our Power Approach Be Current?

Chair: *Tim Fox* - Deutsche Bank Equity Research
Panelists: *David Heacock* - Texas Instruments, Inc., Dallas, TX
Ed Huijbregts - Magma Design Automation, Inc., Santa Clara, CA
Vess Johnson - Nascentric, Inc., Austin, TX
Avner Kornfeld - Intel Corp., Santa Clara, CA
Andrew Yang - Apache Design Solutions, Inc., Mountain View, CA
Paul Zuchowski - IBM Corp., Armonk, NY

Abstract
In the past, power consumption was of little concern to the IC designer. Time-to-market drove the design deadlines, and power consumption was a secondary, if not tertiary, concern. If there were power issues, they could typically be accounted for by tweaking the fabrication process, redesigning after the initial design ship, or even just waiting for the next process change from the fab.

Today power has become one of the sign-off qualifiers prior to fabrication, and the metric for success has changed from performance and area to power consumption in nanometer SoC designs, especially in the huge market for handheld/wireless consumer electronics. Although "power" is often the stated concern, current is the real issue. This fundamental paradigm shift requires changes to both the design flow and the tools used for electrical sign-off.
Keywords: Low-power design, power analysis, leakage current, energy consumption, static power, dynamic power

DAC05, pages 612-617

DTM: Dynamic Tone Mapping for Backlight Scaling

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Abstract

This paper proposes an approach for pixel transformation of the displayed image to increase the potential energy saving of the backlight scaling method. The proposed approach takes advantage of human visual system characteristics and tries to minimize distortion between the perceived brightness values of the individual pixels in the original image and those of the backlight-scaled image. This is in contrast to previous backlight scaling approaches which simply match the luminance values of the individual pixels in the original and backlight-scaled images. Moreover, the proposed dynamic backlight scaling approach, which is based on tone mapping, is amenable to highly efficient hardware realization because it does not need information about the histogram of the displayed image. Experimental results show that the dynamic tone mapping for backlight scaling method results in about 35% power saving with an effective distortion rate of 5% and 55% power saving for a 20% distortion rate.

Keywords: LCDs, Backlight-scaling, Power Management

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DAC05, pages 618-623

Application/Architecture Power CoOptimization for Embedded Systems Powered by Renewable Sources

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ABSTRACT

Embedded systems are being built with renewable power sources such as solar cells to replenish the energy of batteries. The renewable power sources have a wide range of efficiency levels that depend on environment parameters and the current drawn from the circuit. Unlike low-power designs whose goal is to minimize energy consumption, systems with renewable power sources should maximize the efficiency of the sources by load matching. To match the wide dynamic range of solar output, it is necessary to exploit multiple power "knobs" simultaneously. This paper combines computation vs. communication trade-offs, algorithm selection, scheduling and dynamic voltage scaling to maximize the dynamic range of the load over time. Experimental results show one to two orders of magnitude performance improvement for a wireless handheld system running image compression applications.

Keywords: power management, renewable power source, power utilization, load matching, architectural optimization

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DAC05, pages 624-627

User-perceived Latency Driven Voltage Scaling for Interactive Applications

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ABSTRACT

Power has become a critical concern for battery-driven computing systems, on which many applications that are run are interactive. System-level voltage scaling techniques, such as dynamic voltage scaling (DVS) and adaptive body biasing (ABB), have been shown to reduce energy consumption effectively. Previous works on DVS and ABB exploit low CPU utilization of the processor to drive voltage scaling. This has become inadequate for modern interactive applications involving high CPU usage. In this work, we target computer responsiveness during voltage scaling to exploit more opportunities for energy reduction. Instead of CPU utilization, we use the user-perceived latency, the delay between user input and computer response, to drive voltage scaling. Considering the tradeoff between energy consumption and computer responsiveness during voltage scaling not only reduces energy consumption effectively, but also ensures good computer responsiveness for interactive applications. Experimental results show that for the 70nm technology, during the execution of seven commonly-used interactive applications, the energy consumption of the processor using userperceived latency driven DVS is reduced by an average of 37.3%, and the user-perceived latency by an average of 18.3%, compared to CPU utilization driven DVS. If both DVS and ABB are performed simultaneously based on the user-perceived latency, then the energy consumption is reduced by another 38.9% compared to when DVS is performed alone, while maintaining a similar computer responsiveness level. We have implemented user-perceived latency driven voltage scaling under Linux with X Window system. However, the methodology is extensible to other operating systems as well.

Keywords: Adaptive body biasing, computer responsiveness, dynamic voltage scaling, power consumption

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DAC05, pages 628-631

System-Level Energy-Efficient Dynamic Task Scheduling

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ABSTRACT

Dynamic voltage scaling (DVS) is a well-known low power design technique that reduces the processor energy by slowing down the DVS processor and stretching the task execution time. But in a DVS system consisting of a DVS processor and multiple devices, slowing down the processor increases the device energy consumption and thereby the system-level energy consumption. In this paper, we present dynamic task scheduling algorithms for periodic tasks that minimize the system-level energy (CPU energy + device standby energy). The algorithms use a combination of (i) *optimal speed* setting, which is the speed that minimizes the system energy for a specific task, and (ii) *limited preemption* which reduces the numbers of possible preemptions. For the case when the CPU power and device power are comparable, these algorithms achieve up to 43% energy savings compared to [1], but only up to 12% over the non-DVS scheduling. If the device power is large compared to the CPU power, we show that DVS should not be employed.

Keywords: Dynamic task scheduling, energy minimization, optimal scaling point, DVS system, real-time

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DAC05, pages 632-637

OPERA: Optimization with Ellipsoidal uncertainty for Robust Analog IC design

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ABSTRACT
As the design- anufacturing interface becomes increasingly complicated with IC technology scaling, the corresponding process variability poses great challenges for nanoscale analog/RF design. Design optimization based on the enumeration of process corners has been widely used, but can suffer from inefficiency and overdesign. In this paper we propose to formu ate the analog and RF design with variability problem as a special type of robust optimization problem, namely robust geometric programming. The statistical variations in both the process parameters and design variables are captured by a pre-specified confidence ellipsoid. Using such optimization with ellipsoidal uncertainty approach, robust design can be obtained with guaranteed yield bound and lower design cost, and most importantly, the problem size grows linearly with number of uncertain parameters. Numerical examples demonstrate the efficiency and reveal the trade-off between the design cost versus the yield requirement. We will also demonstrate significant improvement in the design cost using this approach compared with corner-enumeration optimization.
Keywords: Statistical optimization

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DAC05, pages 638-643

A Unified Optimization Framework for Equalization Filter Synthesis

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ABSTRACT

We present a novel method for jointly optimizing FIR filters for pre-equalization, decision feedback equalization, and near-end crosstalk cancellation. The unified optimization problem is a linear program, and we describe sparse matrix techniques for its efficient solution. We illustrate our approach with uni- and bi-directional buses using differential signaling in both intra-board and cross-backplane scenarios.

Keywords: crosstalk, equalizing filters, linear programming, optimal synthesis

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Template-Driven Parasitic-Aware Optimization of Analog Integrated Circuit Layouts

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ABSTRACT

Layout parasitics have great impact on analog circuit performance. This paper presents an algorithm for explicit parasitic control during layout retargeting of analog integrated circuits. In order to ensure desired circuit performance, bounds on layout parasitics' magnitudes are determined first. Then, graph techniques are coupled with mathematical programming to constrain layout geometry based on these parasitic bounds. The algorithm has been demonstrated to ensure desired circuit performance during technology migration and performance specification changes.

Keywords: Analog Layout Automation, Parasitics, Sensitivity, Optimization

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DAC05, pages 648-651

Multi-level Approach for Integrated Spiral Inductor Optimization

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ABSTRACT

The efficient optimization of integrated spiral inductors remains a fundamental barrier to the realization of effiective analog and mixed-signal design automation. In this paper, we develop a scalable multi-level optimization methodology for spiral inductors that integrates the exibility of constrained global optimization using Mesh-Adaptive Direct Search (MADS) algorithms with the rapid convergence of local nonlinear convex optimization techniques. Experimental results indicate that our methodology locates optimal spiral inductor geometries with significantly fewer function evaluations than current techniques.

Keywords: Spiral Inductor, Inductor Optimization, Analog Synthesis

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DAC05, pages 652-657

Statistical Static Timing Analysis: How simple can we get?

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Abstract

With an increasing trend in the variation of the primary parameters affecting circuit performance, the need for statistical static timing analysis (SSTA) has been firmly established in the last few years. While it is generally accepted that a timing analysis tool should handle parameter variations, the benefits of advanced SSTA algorithms are still questioned by the designer community because of their significant impact on complexity of STA flows. In this paper, we present convincing evidence that a path-based SSTA approach implemented as a post-processing step captures the effect of parameter variations on circuit performance fairly accurately. On a microprocessor block implemented in 90nm technology, the error in estimating the standard deviation of the timing margin at the inputs of sequential elements is at most 0.066 FO4 delays, which translates in to only 0.31% of worst case path delay.

Keywords: Statistical Static Timing Analysis (SSTA), Process Variations

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DAC05, pages 658-663

Mapping Statistical Process Variations Toward Circuit Performance Variability: An Analytical Modeling Approach

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ABSTRACT

A physical yet compact gate delay model is developed integrating short-channel effects and the Alpha-power law based timing model. This analytical approach accurately predicts both nominal delay and delay variability over a wide range of bias conditions, including sub-threshold. Excellent model scalability enables efficient mapping between process variations and delay variability at the circuit level. Based on this model, relative importance of physical effects on delay variability has been identified. While effective channel length variation is the leading source for variability at current 90nm node, performance variability is actually more sensitive to threshold variation at the sub-threshold region. Furthermore, this model is applied to investigate the limitation of low power design techniques in the presence of process variations, particularly dual V_{th} and L biasing. Due to excessive variability under low V_{DD}, these techniques become ineffective.

Keywords: Process Variations, Delay, Variability

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Power Grid Simulation Via Efficient Sampling-Based Sensitivity Analysis and Hierarchical Symbolic Relaxation

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ABSTRACT

On-chip supply networks are playing an increasingly important role for modern nanometer-scale designs. However, the ever growing sizes of power grids make the analysis problem extremely difficult thereby introducing severe challenges in design and optimization. The inherent analysis complexity calls for innovations in simulation techniques that must provide appropriate accuracy, efficiency as well as the tradeoff thereof to aid design verification and optimization. In this paper, we first present a sampling-based sensitivity analysis by employing the notation of *importance sampling* in a Monte Carlo based circuit simulation framework. This technique allows the extraction of multiparameter sensitivities for the node voltages of interest in the same Monte Carlo runs that are used for computing the nominal voltage values. For more efficient nonstructured whole-grid solution approaches, we further introduce a new *direct* solution method by embedding symbolic relaxation steps in a hierarchical fashion. As a direct method, the proposed hierarchical symbolic relaxation is suitable to both dc and transient analyses. Circuit examples are included to demonstrate the efficacy of the proposed techniques.

Keywords: Power grids, sensitivity and hierarchical analysis

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DAC05, pages 670-671

Formal Verification – Is It Real Enough?

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Keywords: Formal Verification, Functional Verification

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Can We Really Do Without the Support of Formal Methods in the Verification of Large Designs?

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General Terms: verification, reliability

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Streamline Verification Process with Formal Property Verification to Meet Highly Compressed Design Cycle

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ABSTRACT

In this paper, I describe a methodology and tool flow for using formal verification effectively to reduce the verification burden in large custom ASIC designs.

Keywords: Formal verification

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DAC05, pages 678-683

TCAM Enabled On-Chip Logic Minimization

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ABSTRACT

This paper presents an efficient hardware architecture of an on-chip logic minimization coprocessor. The proposed architecture employs TCAM cells to provide fastest and memory efficient implementation suitable for emerging on-chip minimization applications. The paper presents a detailed design of the on-chip minimizer and shows that it requires very little hardware resources to achieve acceptable quality of minimization. An incremental insertion and bulk deletion is achieved in 0.25 μs and 3.8 ms respectively and a compaction of 100000 entries in 25 ms using just 300 TCAM entries.

Keywords: TCAM, Logic Minimization,On-Chip

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DAC05, pages 684-689

Hardware Speech Recognition for User Interfaces in Low Cost, Low Power Devices

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ABSTRACT

We propose a system architecture for real-time hardware speech recognition on low-cost, power-constrained devices. The system is intended to support real-time speech-based user interfaces as part of an effort to bring Information and Communication Technologies (ICTs) to underdeveloped regions of the world. Our system architecture exploits a shared infrastructure model. The computationally intensive task of speech model training and retraining is performed offine by shared servers, while the actual recognition of speech is conducted on low-cost hand-held devices using custom hardware. The recognizer is extremely exible and can support multiple languages or dialects with speaker-independent recognition.Dynamic loading of speech models is used for changing language grammar and retraining, while reprogramming is used to support evolution of recognition algorithms. The focus on small sets of words (at one time) reduces the complexity, cost and power consumption. We design the speech decoder, the central component of the recognizer, and we validate it via a prototype FPGA implementation. We then use ASIC synthesis to estimate power and size for the design. Our evaluations demonstrate an order of magnitude improvement in power compared with optimized recognition software running on a low-power embedded general-purpose processor of the same technology and of similar capabilities. The synthesis also estimates the area of the design to be about 2.5mm2, showing potential for lower cost. In designing and testing our recognizer we use datasets in both English and Tamil languages.

Keywords: Speech recognition, low power, ASIC, tamil, TIER

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DAC05, pages 690-695

Improving Java Virtual Machine Reliability for Memory-Constrained Embedded Systems

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ABSTRACT

Dual-execution/checkpointing based transient error tolerance techniques have been widely used in the high-end mission critical systems. These techniques, however, are not very attractive for cost-sensitive embedded systems because they require extra resources (e.g., large memory, special hardware, etc), and thus increase overall cost of the system. In this paper, we propose a transient error tolerant Java Virtual Machine (JVM) implementation for embedded systems. Our JVM uses dual-execution and checkpointing to detect and recover from transient errors. However, our technique does not require any special hardware support (except for the memory page protection mechanism, which is commonly available in modern embedded processors), and the memory space overhead it incurs is not excessive. Therefore, it is suitable for memory-constrained embedded systems. We implemented our approach and performed experiments with seven embedded Java applications.

Keywords: Java Virtual Machine, dual execution, transient error

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DAC05, pages 696-699

Frequency-Based Code Placement for Embedded Multiprocessors

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ABSTRACT

Multiprocessor embedded systems often have processor-local caches and a shared memory. If the system's code is available at design time we can maximize cache hits by rearranging code in memory so that frequently executed tasks reside in reserved areas of the caches and are not overwritten by less frequent tasks.

Keywords: Embedded Systems, Multiprocessors, Caching, Memory, Code Placement, Frequent Code

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DAC05, pages 700-705

Power Emulation: A New Paradigm for Power Estimation

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ABSTRACT

In this work, we propose a new paradigm called **power emulation**, which exploits hardware acceleration to drastically speedup power estimation. Power emulation is based on the observation that most power estimation tools typically perform the following sequence of operations: simulating the circuit to obtain value traces or statistics for the inputs of its constituent components, evaluating power models for each circuit component based on the input values seen during simulation, and aggregating the power consumption of individual components to compute the circuit's power consumption. We further recognize that the steps involved in power estimation (power model evaluation, aggregation) can themselves be thought of as synthesizable functions and implemented as hardware circuits. Thus, any given design can be enhanced by adding to it .power estimation hardware., and the resulting power model enhanced circuit can be mapped onto a hardware prototyping platform. While drastic speedups in power estimation (orders of magnitude) are possible using this approach, a significant challenge arises due to the increase in circuit size as a result of adding power estimation hardware. We propose a systematic methodology to reduce the size of the power model enhanced circuit through a suite of techniques, including power model reuse across different circuit components, regulating the granularity of components for power modeling, exploiting inter-component power correlations, resource sharing for power model computations, and the use of block memories for efficient storage within power models. We demonstrate the benefits of the proposed power emulation paradigm by applying it to register-transfer level (RTL) power estimation for industrial designs, resulting in speedups from around 10X to over 500X compared to state-of-the-art commercial power estimation tools.

Keywords: Power Estimation, Emulation, Design, Design Methodologies, Macromodels, FPGA, Hardware Acceleration, Register-Transfer Level, Simulation

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Implementing Low-Power Configurable Processors — Practical Options and Tradeoffs

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Abstract

Configurable processors enable dramatic gains in energy efficiency, relative to traditional fixed instruction-set processors. This energy advantage comes from three improvements. First, configuration of the instruction set permits a much closer fit of the processor to the target applications, reducing the number of execution cycles required. Second, configuring the processor removes unneeded features, reducing power and area overhead. Third, automatic processor generation tools enable logic optimization, signal switching reductions, and seamless mapping into low-voltage circuits and processes, for very low-power operation. The first improvement has been well-studied. Analysis of the second and third improvements requires detailed circuit and layout experiments, which is the primary focus of this paper.

Starting from a range of existing available power saving options, this work explores the tradeoff and analyzes the results: the design priority tradeoff, the process technology impact, and implementing low-power configurable processor using commercial scaled-VDD cell libraries compatible with mainstream SOC practices. These real processor designs can achieve power dissipation approaching 20μW/MHz at 0.8V and close to 10μW/MHz at 0.6V, using production 0.13um libraries. Finally, this work quantifies the dramatic process, voltage and temperature dependence in post-layout leakage power for small processor designs.

Keywords: Configurable embedded processor, SOC (system on chip), PVT (process, voltage, temperature), Low-power, Leakage Power, Dynamic Power, Dynamic power efficiency, Scaled VDD

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DAC05, pages 712-715

Low Power Network Processor Design Using Clock Gating

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ABSTRACT

Network processors (NPs) have emerged as successful platforms to providing both high performance and flexibility in building powerful routers. Typical NPs incorporate multiprocessing and multi-threading to achieve maximum parallel processing capabilities. We observed that under low incoming traffic rates, most processing elements (PEs) in NPs are nearly idle and yet still consume dynamic power. This paper develops a low power technique to reduce the activities of PEs according to the varying traffic volume. We propose to monitor the average number of idle threads in a time window, and gate off the clock network of unused PEs when a subset of PEs is enough to handle the network traffic. We show that our technique brings significant reduction in power consumption (up to 30%) of NPs with no packet loss and little impact to the overall throughput.

Keywords: Network Processors, Low Power

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DAC05, pages 716-719

A Variation-tolerant Subthreshold Design Approach

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ABSTRACT

Due to their extreme low power consumption, sub-threshold design approaches are appealing for a widening class of applications which demand low power consumption and can tolerate larger circuit delays. However, sub-threshold circuits are extremely sensitive to variations in supply, temperature and processing factors. In this paper, we present a sub-threshold design methodology which dynamically self-adjusts for inter and intra-die process, supply voltage and temperature (PVT) variations. This adjustment is achieved by performing bulk voltage adjustments in a closed-loop fashion, using a charge pump and a phase-detector.

Keywords: Sub-threshold, Body-biasing, Self-adjusting, Variation-tolerant

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DAC05, pages 720-725

Leakage Efficient Chip-Level Dual-Vdd Assignment with Time Slack Allocation for FPGA Power Reduction

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ABSTRACT

To reduce power, Vdd programmability has been proposed recently to select Vdd-level for interconnects and to powergate unused interconnects. However, Vdd-level converters used in the Vdd-programmable method consume a large amount of leakage. In this paper, we develop chip-level dual-Vdd assignment algorithms to guarantee that no low-Vdd interconnect switch drives high-Vdd interconnect switches. This removes the need of Vdd-level converters and reduces interconnect leakage and interconnect device area by 91.78% and 25.48%, respectively. The assignment algorithms include power sensitivity based heuristics with implicit time slack allocation and a linear programming (LP) based method with explicit time slack allocation. Both first allocate time slack to interconnects with higher transition density and assign low-Vdd to them for more power reduction. Compared to the aforementioned Vdd-programmable method using Vdd-level converters, the LP based algorithm reduces interconnect power by 65.13% without performance loss for the MCNC benchmark circuits. Compared to the LP based algorithm, the sensitivity based heuristics can obtain slightly smaller power reduction but run 4*X* faster.

Keywords: FPGA, low power, time slack, programmable-Vdd

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DAC05, pages726-731

Logic Block Clustering of Large Designs for Channel-Width Constrained FPGAs

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ABSTRACT

In this paper we present a system level technique for mapping large, multiple-IP-block designs to channel-width constrained FPGAs. Most FPGA clustering tools [2, 3, 11] aim to reduce the amount of inter-cluster connections, hence reducing channel width needs. However, if this exceeds the FPGA's channel width (a *hard constraint*), then the circuit still cannot be routed. Previous work [11, 12] depopulates logic clusters (CLBs) to reduce channel width. By depopulating non-uniformly, *i.e.* depopulate more in hard-to-route regions, we show a graceful trade-off between channel width and CLB count. This makes it possible to target specific channel-width constraints during clustering with minimal CLB inflation. Results show channel width decreases of up to 20% with a 5% increase in area. Further decreases of nearly 50% are possible at 3.3 times the original area. Despite the area increase, this technique creates routable solutions from otherwise-unroutable circuits.

Keywords: Field-Programmable Gate Arrays (FPGA), Clustering, Packing, Channel Width Constraints

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DAC05, pages 732-737

Dynamic Reconfiguration with Binary Translation: Breaking the ILP Barrier with Software Compatibility

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ABSTRACT

In this paper we present the impact of dynamically translating any sequence of instructions into combinational logic. The proposed approach combines a reconfigurable architecture with a binary translation mechanism, being totally transparent for the software designer. Besides ensuring software compatibility, the technique allows porting the same code for different machines tracking technological evolutions. The target processor is a Java machine able to execute Java bytecodes. Experimental results show that even code without any available parallelism can benefit from the proposed approach. Algorithms used in the embedded systems domain were accelerated 4.6 times in the mean, while spending 10.89 times less energy in the average. We present results regarding the impact of area and power, and compare the proposed approach with other Java machines, including a VLIW one.

Keywords: Java, Reconfigurable Processors, Binary Translation, Power Consumption

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DAC05, pages 738-743

Beyond Safety: Customized SAT-based Model Checking

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ABSTRACT

Model checking of safety properties has taken a significant lead over non-safety properties in recent years. To bridge the gap, we propose dedicated SAT-based model checking algorithms for properties beyond safety. Previous bounded model checking (BMC) approaches have relied on either converting such properties to safety checking, or finding proofs by deriving termination criteria using loop-free path analysis. Instead, our approach uses a customized SAT-based formulation for bounded model checking of non-safety properties, and determines the completeness bounds for liveness using unbounded SAT-based analysis. Our main contributions are: 1) Customized property translations for LTL formulas for BMC, with novel features that utilize partitioning, learning, and incremental formulation. Customized translations not only improve the BMC performance significantly in comparison to standard monolithic LTL translations, but also allow efficient derivation and use of completeness bounds. Though we discuss the translation schemas for liveness, they can be easily extended to handle other LTL properties as well. 2) Customized formulations for determining completeness bounds for liveness using SAT-based unbounded model checking (UMC) rather than using loop-free path analysis. These formulations comprise greatest fixed-point and least fixed-point computations to efficiently handle nested properties using SAT-based quantification approaches. We show the effectiveness of our overall approach for checking liveness on public benchmarks and several industry designs.

Keywords: Formal verification, bounded model checking, unbounded model checking, LTL, liveness, SAT, circuit cofactoring

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DAC05, pages 744-749

Efficient SAT Solving: Beyond Supercubes

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ABSTRACT

SAT (Boolean satisfiability) has become the primary Boolean reasoning engine for many EDA applications, so the efficiency of SAT solving is of great practical importance. Recently, Goldberg et al. introduced supercubing, a different approach to search-space pruning, based on a theory that unifies many existing methods. Their implementation reduced the number of decisions, but no speedup was obtained. In this paper, we generalize beyond supercubes, creating a theory we call B-cubing, and show how to implement B-cubing in a practical solver. On extensive benchmark runs, using both real problems and synthetic benchmarks, the new technique is competitive on average with the newest version of ZChaff, is much faster in some cases, and is more robust. Categories and Subject Descriptors

Keywords: SAT, formal verification, learning, search space pruning

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DAC05, pages 750-753

Prime Clauses for Fast Enumeration of Satisfying Assignments to Boolean Circuits

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Abstract

Finding all satisfying assignments of a propositional formula has many applications in the design of hardware and software. An approach to this problem augments a clause-recording propositional satisfiability solver with the ability to add *blocking clauses*, which prevent the solver from visiting the same solution more than once. One generates a blocking clause from a satisfying assignment by taking its complement. In this paper, we present an improved algorithm for finding all satisfying assignments for a generic Boolean circuit. An optimization based on lifting—which generates minimal satisfying assignments—yields prime blocking clauses. Thanks to the primality of the blocking clauses, the derived conflict clauses usually prune both satisfiable and unsatisfiable points at once. The efficiency of our new algorithm is demonstrated by our preliminary results on SAT-based unbounded model checking.

Keywords: SAT, CNF, AllSAT, minimal satisfying assignment

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Dynamic Abstraction Using SAT-based BMC

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ABSTRACT
We propose a new dynamic method of abstraction, which can be applied during successive steps of the model checking algorithm to further reduce the model produced by traditional static abstraction methods. This is facilitated by information gathered from an analysis of the proof of unsatisfiability of SAT-based bounded model checking problems formulated on the original design. The dynamic abstraction effectively allows the model checker to work with smaller abstract models. Experiments on several industrial benchmarks demonstrate that dynamic abstraction can significantly improve both the performance and the capacity of typical abstraction refinement flows.
Keywords: Abstraction Refinement, Model Checking, SAT

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DAC05, pages 758-759

BEOL Variability and Impact on RC Extraction

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Abstract
Historically, Back End of Line (BEOL) or interconnect resistance and capacitance have been viewed as parasitic components. They have now become key parameters with significant impact on circuit performance and signal integrity. This paper examines the types of BEOL variations and their impact on RC extraction. The importance of modeling systematic effects in RC extraction is discussed. The need for minimizing the computational error in RC extraction before incorporating random process variations is emphasized.
Keywords: Process variation, Interconnect, Extraction

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An Effective DFM Strategy Requires Accurate Process and IP Pre-Characterization

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Keywords: DFM, yield, test chips, yield models

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DAC05, pages762-763

Variation-Tolerant Circuits: Circuit Solutions and Techniques

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ABSTRACT

Die-to-die and within-die variations impact the frequency and power of fabricated dies, affecting functionality, performance, and revenue. Variation-tolerant circuits and post-silicon tuning techniques are important for minimizing the impacts of these variations. This paper describes several circuit techniques that can be employed to ensure efficient circuit operation in the presence of ever-increasing variations.

Keywords: Parameter variation, high-performance design, body bias

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DAC05, pages 764-765

On the Need for Statistical Timing Analysis

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ABSTRACT

Traditional corner analysis fails to guarantee a target yield for a given performance metric. However, recently proposed solutions, in the form of statistical timing analysis, which work by propagating delay distributions, do not conform to modern design methodology. Instead, new statistical techniques are needed to modify corner analysis in ways that overcome its weaknesses without violating usage models of timing tools in modern flows.

Keywords: Variability, Statistical timing analysis

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CAD Tools for Variation Tolerance

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ABSTRACT

Process variability greatly affects power and timing of nanometer scale CMOS circuits, leading to parametric yield loss due to both timing and power constraint violations. This parametric yield loss will continue to worsen in future technologies as a result of increasing process variations [1] and the increased importance of leakage power. Hence, statistical techniques are required to maximize parametric yield under given power and frequency constraints. Recently, much progress has been reported in the area of statistical modeling of leakage power [6] and circuit timing [2-5]. These techniques are useful in analyzing the impact of process variations on performance and power in nanometer CMOS designs. In this extended abstract, we outline the need for statistical optimization methods.

Keywords: Yield, Variability, Design Flows

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DAC05, pages 767-768

Are There Economic Benefits in DFM ?

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ABSTRACT
A fabless company perspective is presented on the roles of the foundries, design entities and EDA providers in the DFM arena, and the requirements for measurement of the economic benefits of DFM
Keywords: DFM, Design for Manufacturability, Foundries, Fabless

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A Generic Micro-Architectural Test Plan Approach for Microprocessor Verification

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ABSTRACT
Modern microprocessors share several common types of microarchitectural building blocks. The rising complexity of the microarchitecture increases the risk of bugs and the difficulty of achieving comprehensive verification. We propose a methodology to exploit the commonality in the different microprocessors to create a design-independent micro-architectural test plan. Our method allows the testing of the huge micro-architectural test space by using systematic partitioning, which offers a high level of comprehensiveness of the tested behaviors. We show how this method was used to find bugs during verification of an actual high-end microprocessor. Our results show the advantages of this approach over the more traditional test methods that use design specific test plans or that use tools with little micro-architectural knowledge for covering micro-architectural aspects of the design.
Keywords: Micro-architecture, Coverage, Generic Test Plan, Dynamic Verification, Test Generation

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IODINE: A Tool to Automatically Infer Dynamic Invariants for Hardware Designs

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ABSTRACT

We describe IODINE, a tool to automatically extract likely design properties using dynamic analysis. A practical bottleneck in the formal verification of hardware designs is the need to manually specify design-specific properties. IODINE presents a way to automatically extract properties such as state machine protocols, request-acknowledge pairs, and mutual exclusion between signals from design simulations. We show that dynamic invariant detection for hardware designs can infer relevant and accurate properties.

Keywords: Dynamic Invariants, Dynamic Analysis, Formal Specification

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VLIW – A Case Study of Parallelism Verification

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ABSTRACT
Parallelism in processor architecture and design imposes a verification challenge as the exponential growth in the number of execution combinations becomes unwieldy. In this paper we report on the verification of a Very Large Instruction Word processor. The verification team used a sophisticated test program generator that modeled the parallel aspects as sequential constraints, and augmented the tool with manually written test templates. The system created large numbers of legal stimuli, however the quality of the tests was proved insufficient by several post silicon bugs. We analyze this experience and suggest an alternative, parallel generation technique. We show through experiments the feasibility of the new technique and its superior quality along several dimensions. We claim that the results apply to other parallel architectures and verification environments.
Keywords: Functional verification, Processor verification, Test generation, VLIW, Parallelism

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StressTest: An Automatic Approach to Test Generation Via Activity Monitors

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ABSTRACT

The challenge of verifying a modern microprocessor design is an overwhelming one: Increasingly complex micro-architectures combined with heavy time-to-market pressure have forced microprocessor vendors to employ immense verification teams in the hope of finding the most critical bugs in a timely manner. Unfortunately, too often size doesn't seem to matter for verification teams, as design schedules continue to slip and microprocessors find their way to the marketplace with design errors. In this paper, we describe a simulation-based random test generation tool, called StressTest, that provides assistance in locating hard-to-find corner-case design bugs and performance problems. StressTest is based on a Markov-model-driven random instruction generator with activity monitors. The model is generated from the user-specified template programs and is used to generate the instructions sent to the design under test (DUT). In addition, the user specifies key activity points within the design that should be stressed and monitored throughout the simulation. The StressTest engine then uses closed-loop feedback techniques to transform the Markov model into one that effectively stresses the points of interest. In parallel, StressTest monitors the correctness of the DUT response to the supplied stimuli, and if the design behaves unexpectedly, a bug and a trace that leads to it are reported. Using two micro-architectures as example testbeds, we demonstrate that StressTest finds more bugs with less effort than open-loop random instruction test generation techniques.

Keywords: Architectural simulation, High-performance simulation, Directed-random simulation

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Smart Diagnostics for Configurable Processor Verification

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ABSTRACT

This paper describes a novel technique called Embedded Test-bench Control (ETC), extensively used in the verification of Tensilica's latest configurable processor. Conventional simulation-based verification methodologies that employ assembly programs for testing cannot easily link the diagnostic program to the test-bench for interactive control, consequently resulting in weaker coverage. ETC links the diagnostic program execution and the test-bench functions, thereby increasing the flexibility and power of the diagnostics to create more complex corner cases in fewer simulation cycles and with smaller code size. This method also enables dynamic self-checking and dynamic coverage analysis by either passing or failing the diagnostic based on the coverage goal, or terminating runaway random diagnostics much earlier. The presented simulation results show that ETC augments verification in two major areas: the creation of more maintainable, efficient, and smart diagnostics, and the reduction of the regression time. Some of the techniques presented in this paper can apply to non-processor verification methodologies as well.

Keywords: Functional Verification, Configurable Processors, Embedded Test-bench Control, Diagnostics, Coverage

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Power-Aware Placement

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ABSTRACT

Lowering power is one of the greatest challenges facing the IC industry today. We present a power-aware placement method that simultaneously performs (1) *activity-based register clustering* that reduces clock power by placing registers in the same leaf cluster of the clock trees in a smaller area and (2) *activity-based net weighting* that reduces net switching power by assigning a combination of activity and timing weights to the nets with higher switching rates or more critical timing. The method applies to designs with multiple clocks and gated clocks. We implemented the method and obtained experimental results on 8 real-world designs after placement, routing, extraction and analysis. The power-aware placement method achieved on average 25.3% and 11.4% reduction in net switching power and total power respectively, with 2.0% timing, 1.2% cell area and 11.5% runtime impact. This method has been incorporated into a commercial physical design tool.

Keywords: Net Switching Power, Clock Tree, Dynamic Power

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How Accurately Can We Model Timing In A Placement Engine?

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ABSTRACT

This paper presents a novel placement algorithm for timing optimization based on a new and powerful concept, which we term differential timing analysis. Recognizing that accurate optimization requires timing information from a signoff static timing analyzer, we propose an incremental placement algorithm that uses timing information from a signoff static timing engine. We propose a set of differential timing analysis equations that accurately capture the effect of placement perturbations on changes in timing from the signoff timer. We have formulated an incremental placement optimization problem based on differential timing analysis as a single linear programming (LP) problem which is solved to generate the new timing-optimized placement.

Our experiments show that the worst negative slack (WNS) improves by an average of 30% and the total negative slack (TNS) improves by 33% on average for a set of circuits from a 3.0 GHz microprocessor that were already synthesized and placed by a leading industrial physical synthesis tool. We also show that multiple iterations of our engine give further TNS improvements – an average improvement of 51%, which implies that our placer will significantly speed up timing convergence.

Keywords: Timing-driven placement, static timing analysis, linear programming, differential timing analysis

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Efficient and Accurate Gate Sizing with Piecewise Convex Delay Models

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ABSTRACT

We present an efficient and accurate gate sizing tool that employs a novel piecewise convex delay model, handling both rise and fall delays, for static CMOS gates. The delay model is used in a new version of a gate-sizing tool called Forge, which not only exhibits optimality, but also efficiently produces the area versus delay trade-off curve for a block in one step. Forge includes a realistic delay propagation scheme that combines arrival times and slew-rates. Forge is 6.4X faster than a commercial transistor sizing tool, while achieving better delay targets and uses 28% less transistor area for specific delay targets, on average.

Keywords: Delay modeling, gate sizing, Lagrangian relaxation, piecewise convex, optimization

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Freeze: Engineering a Fast Repeater Insertion Solver for Power Minimization Using the Ellipsoid Method

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ABSTRACT

This paper presents a novel repeater insertion algorithm for the power minimization of realistic interconnect trees under given timing budgets. Our algorithm judiciously combines a local optimizer based on the dynamic programming technique and a global search engine using the *ellipsoid method*. As a result, our approach is capable of producing high-quality solutions at a very fast speed. Furthermore, our scheme is robust and does not need any manual tuning of the iteration-control parameters. We have developed a repeater insertion tool, called FREEZE, using the proposed algorithm and applied it to various interconnect trees with different timing targets. Experimental results demonstrate the high effectiveness of our approach. In comparison with the state-of-the-art low-power repeater insertion schemes, FREEZE requires 5.8 times fewer iterations on the average, achieving up to 27 times speedup with even better power savings. When compared with a dynamic programming based scheme, which guarantees the optimal solution, our tool delivers up to 50 times speedup with 0.9% power increase on the average.

Keywords: Interconnect, Repeater Insertion, Low Power

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Minimising Buffer Requirements of Synchronous Dataflow Graphs with Model Checking

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ABSTRACT

Signal processing and multimedia applications are often implemented on resource constrained embedded systems. It is therefore important to find implementations that use as little resources as possible. These applications are frequently specified as synchronous dataow graphs. Communication between actors of these graphs requires storage capacity. In this paper, we present an exact method to determine the minimum storage capacity required to execute the graph using model-checking techniques. This can be done for different measures of storage capacity. The problem is known to be NP-complete and because of this, existing buffer minimisation techniques are heuristics and hence not exact. Modern model-checking tools are quite efficient and they have been successfully applied to scheduling-related problems. We study the feasibility of this approach with examples.

Keywords: Synchronous Dataow, buffering, model-checking, optimization

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Unified High-Level Synthesis and Module Placement for Defect-Tolerant Microfluidic Biochips

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ABSTRACT
Microfluidic biochips promise to revolutionize biosensing and clinical diagnostics. As more bioassays are executed concurrently on a biochip, system integration and design complexity are expected to increase dramatically. This problem is also identified by the 2003 ITRS document as a major system-level design challenge beyond 2009. We focus here on the automated design of droplet-based microfluidic biochips. We present a synthesis methodology that unifies operation scheduling, resource binding, and module placement for such "digital" biochips. The proposed technique, which is based on parallel recombinative simulated annealing, can also be used after fabrication to bypass defective cells in the microfluidic array. A real-life protein assay is used to evaluate the synthesis methodology.
Keywords: Synthesis, placement, defect tolerance, microfluidics, biochip

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Towards Scalable Flow and Context Sensitive Pointer Analysis

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ABSTRACT

Pointer analysis, a classic problem in software program analysis, has emerged as an important problem to solve in design automation, at a time when complex designs, specified in the form of C code, need to be synthesized or verified. However, precise pointer analysis algorithms that are both context and flow sensitive (FSCS), have not been shown to scale. In this paper, we report a new solution for FSCS analysis, which can evaluate the program states of all program points under billions of different calling paths. Our solution extends the recently proposed symbolic pointer analysis (SPA) technology, which exploits the efficiency of Binary Decision Diagrams (BDDs). With our new strategy of problem solving, called superposed symbolic computation, and its application on our generic pointer analysis framework, we are able to report the first result on all SPEC2000 benchmarks that completes context sensitive, flow insensitive analysis in seconds, and context sensitive, flow sensitive analysis in minutes.

Keywords: Pointer analysis, binary decision diagrams, High-level synthesis

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MiniBit: Bit-Width Optimization via Affine Arithmetic

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ABSTRACT

MiniBit, our automated approach for optimizing bit-widths of fixed-point designs is based on static analysis via affine arithmetic. We describe methods to minimize both the integer and fraction parts of fixed-point signals with the aim of minimizing circuit area. Our range analysis technique identifies the number of integer bits required. For precision analysis, we employ a semi-analytical approach with analytical error models in conjunction with adaptive simulated annealing to find the optimum number of fraction bits. Improvements for a given design reduce area and latency by up to 20% and 12% respectively, over optimum uniform fraction bit-widths on a Xilinx Virtex-4 FPGA.

Keywords: Affine Arithmetic, Bit-Width, Fixed-Point, FPGA, Simulated Annealing

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A Non-Parametric Approach for Dynamic Range Estimation of Nonlinear Systems

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ABSTRACT

It has been widely recognized that the dynamic range information of an application can be exploited to reduce the datapath bitwidth of either processors or ASICs, and therefore the overall circuit area, delay, and power consumption. Recent advances in analytical dynamic range estimation methods indicate that by systematically decomposing the system inputs into orthonormal random variables using a mathematical procedure called polynomial chaos expansion (PCE), output statistics of interest can be obtained for both linear and nonlinear systems. Despite its power for capturing both spatial and temporal correlation, the application of this method has been limited only to near-Gaussian inputs. In this paper, we propose the first algorithm with the capacity of handling both near-Gaussian and non-Gaussian input signals. Our method is based on the use of independent component analysis (ICA). Our experiments show that the new algorithm can reduce the original relative errors of 2nd order moments from 25% − 65% to 1% − 2%.

Keywords: Dynamic range estimation, Non-Gaussian, Nonlinear, Independent component analysis, Non-parametric

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Path Delay Test Compaction with Process Variation Tolerance

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ABSTRACT
In this paper we propose a test compaction method for path delay faults in a logic circuit. The method generates a compact set of two-pattern tests for faults on long paths selected with a criterion. While the proposed method generates each two-pattern test for more than one fault in the target fault list as well as ordinary test compaction methods, secondary target faults are selected from the fault list such that many other faults, which may not be included in the fault list, are detected by the test pattern. Even if faults on long paths in a manufactured circuit are not included in the fault list due to a process variation or noise, the compact test set would detect the longer untargeted faults, i.e., the test set has a noise or variation tolerant nature. Experimental results show that the proposed method can generate a compact test set and it detects longer untargeted path delay faults efficiently.
Keywords: delay testing, test compaction, path delay fault, process variation

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A DFT Approach for Diagnosis and Process Variation-Aware Structural Test of Thermometer Coded Current Steering DACs

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Abstract

A design for test (DFT) hardware is proposed to increase the controllability of a thermometer coded current steering digital to analog converter. A procedure is introduced to reduce the diagnosis and structural test time from quadratic to linear using the proposed DFT hardware. To evaluate the applicability of the proposed technique, principal component analysis is used to create virtual process variations to simulate in lieu of semiconductor fabrication data. An architecture specific soft fault model is suggested for the diagnosis problem. Random errors according to the fault model are introduced in the virtual test environment on top of the process variations and it is shown that diagnosis of a fault is possible with high accuracy with the proposed method. The same technique employing principal component analysis is furthermore used to provide process variation-aware reference test comparison values for a structural test of the DAC. The structural test provides a mechanism to test for even unmodeled manufacturing faults. The process variation-aware test values help detect defects even under process variations. The proposed DFT hardware and method are low cost and quite suitable for a built-in self diagnosis and test implementation.

Keywords: DFT, BIST, CS-DAC, current steering, test, process variation-aware test, diagnosis

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Resistive-Open Defect Injection in SRAM Core-Cell: Analysis and Comparison between 0.13 µm and 90 nm Technologies

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ABSTRACT
Resistive-open defects appear more and more frequently in VDSM technologies. In this paper we present a study concerning resistive-open defects in the core-cell of SRAM memories. The first target of this work is a comparison of the effect produced by resistive-open defects in the 0.13 µm and 90 nm core-cell. We show that the 90 nm core-cell is more robust than the 0.13 µm core-cell in presence of resistive-open defects. On the other hand we show that dynamic faults are most likely to occur in the 90 nm than in 0.13 µm core-cell. Finally we propose a unique March test solution that ensures the complete coverage of all the extracted fault models for both technologies.
Keywords SRAM Memories, Core-cell, Dynamic Faults, March Test

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Asynchronous Circuits Transient Faults Sensitivity Evaluation

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ABSTRACT

This paper presents a transient faults sensitivity evaluation for Quasi Delay Insensitive (QDI) asynchronous circuits. Because of their specific architecture, asynchronous circuits have a very different behavior than synchronous circuits in the presence of faults. We address the effects of transient faults in QDI circuits and describe the causes that lead the faults to be memorized into one or more soft errors. Therefore, a refined fault sensitivity criterion is defined for this class of circuits. This methodology enables us to point out the weak parts of a circuit. An analysis tool is implemented to support this evaluation. This tool provides a quantitative study of the fault sensitivity, and enables us to compare the robustness of different architectures of a circuit along the steps of its design flow. The objective of this work is to evaluate the circuits robustness against natural faults (single fault model) and intentional fault injection (multiple faults model).

Keywords: Asynchronous circuits, Quasi Delay Insensitive, transient fault, fault model, simulation

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Deterministic Approaches to Analog Performance Space Exploration (PSE)

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ABSTRACT

Performance space exploration (PSE) determines the range of feasible performance values of a circuit block for a given topology and technology. In this paper, we present two deterministic approaches for PSE. One approximates the feasible performance space based on linearized circuit models and is suitable for investigating a large number of performances. The other one computes discretizations of the Pareto front of competing performances. In addition, a motivation and application of PSE using a hierarchical design example is presented.

Keywords: Performance Space Exploration, Analog Integrated Circuits, Pareto Optimization, Fourier Motzkin Elimination

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Mixed Signal Design Space Exploration through Analog Platforms

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ABSTRACT

We propose a hierarchical mixed signal design methodology based on the principles of Platform-Based Design (PBD). The methodology is a meet-in-the-middle approach where design components are modeled bottom-up at various abstraction levels and performance constraints are mapped top-down to select among the available components the ones that best meet the constraints. The design methodology can seamlessly operate on both analog and digital designs, thus dealing with mixed signal designs in a consistent way. We demonstrate the effectiveness of the approach optimizing an 80 MS/s 14 bit pipelined Analog-to-Digital Converter (ADC) including digital calibration, yielding 64% power reduction compared to the original hand optimized design.

General Terms: Algorithms

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Performance Space Modeling for Hierarchical Synthesis of Analog Integrated Circuits

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ABSTRACT

Automated analog sizing is becoming an unavoidable solution for increasing analog design productivity. The complexity of typical analog SoC subsystems however calls for efficient methods that can handle design hierarchy, in terms of both performance estimation and hierarchical design optimization method. This paper discusses and compares recent developments in this area, with special emphasis on automated modeling and on multi–objective bottom–up hierarchical design.

Keywords: Hierarchical Synthesis

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DAC05, pages 887-888

Structured/Platform ASIC Apprentices Which Platform Will Survive Your Board Room?

Panel Moderator: *Ron Wilson* - Electronic Engineering Times
Panelists: *Chris Hamlin* - LSI Logic Corp., Milpitas, CA
Ken McElvain - Synplicity Inc., Sunnyvale, CA
Steve Leibson - Tensilica Inc., Santa Clara, CA
Ivo Bolson - Xilinx Inc., San Jose, CA
Rich Tobias - Toshiba America Inc., New York, NY
Raul Camposano - Synopsys Inc., Mountain View, CA

Abstract
Moore's law delivers higher performance and lower cost for FPGAs and ASICs alike, but at the 90nm process node and below, design schedules using the traditional cell-based ASIC design methodology hit a wall of uncertainty. At 90nm and below an emerging alternative ASIC design platform is either Platform ASIC or FPGAs. Which way will the cell-based ASIC designer turn for their next design?

Over time, FPGAs and structured/platform ASICs are together poised to replace today's cell-based ASIC market, but which is the real answer to future digital design? Can companies really use these platforms to achieve the system cost reduction and functionality that they need to stay competitive? Which applications will migrate to these platforms the fastest? Is it possible to just tweak the existing cell-based methodology to more efficiently reach the benefits of 90nm process nodes and below? This lively panel will discuss whether it is FPGAs, structured/platform ASICs, or something else that stand to gain the most ground from the projected $25B ASIC market, and why.
Keywords: Digital Design and Programmable ASIC Platforms

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Quasi-Static Assignment of Voltages and Optional Cycles for Maximizing Rewards in Real-Time Systems with Energy Constraints

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ABSTRACT

There exist real-time systems for which it is possible to trade off precision for timeliness. In these cases, a function assigns reward to the application depending on the amount of computation allotted to it. At the same time, many such applications run on battery-powered devices with stringent energy constraints. This paper addresses the problem of maximizing rewards subject to time and energy constraints. We propose a quasi-static approach where the problem is solved in two steps: first, at design-time, a number of solutions are computed and stored (off-line phase); second, one of the precomputed solutions is selected at run-time based on actual values of time and energy (on-line phase). Thus our approach is able to exploit, with low on-line overhead, the dynamic slack caused by tasks executing less number of cycles than in the worst case. We conduct numerous experiments in order to show the advantages of our approach.

Keywords: Quasi-Static, Dynamic Voltage Scaling

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DC-DC Converter-Aware Power Management for Battery-Operated Embedded Systems

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ABSTRACT

Most digital systems are equipped with DC-DC converters to supply various levels of voltages from batteries to logic devices. DC-DC converters maintain legal voltage ranges regardless of the load current variation as well as battery voltage drop. Although the efficiency of DC-DC converters is changed by the output voltage level and the load current, most existing power management techniques simply ignore the efficiency variation of DC-DC converters. However, without a careful consideration of the efficiency variation of DC-DC converters, finding a true optimal power management will be impossible. In this work, we solve the problem of energy minimization with the consideration of the characteristics of power consumption of DC-DC converter. Specifically, the contributions of our work are: (1) We analyze the effects of the efficiency variation of DC-DC converters on a single task execution in DVS (dynamic voltage scaling) scheme, and propose a technique, called DC DVS, of DC-DC converter-aware energy-minimal DVS; (2) DC DVS is then extended to combine the effects of DC-DC converters with the procedures of general DVS techniques with multiple tasks; (3) Conversely, we propose a technique, called DC CONF, of generating a DC-DC converter that is best suited, in terms of total energy efficiency, to the intended application, and (4) finally, we complete our integrated framework DC-lp, which is based on DC DVS and DC CONF, that attempts to solve the DC-DC converter configuration selection problem and the DVS problem simultaneously. To show the effectiveness of the proposed techniques, a set of experimental results is provided. In summary, it is shown that DC-lp is able to save 16.0%»22.1% of energy on the average, which otherwise was dissipated in the previous power management schemes with no consideration of DC-DC converter efficiency variation.

Keywords: Low power, DC-DC converter, Voltage scaling

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Energy Optimal Speed Control of Devices with Discrete Speed Sets

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ABSTRACT

We obtain analytically, the energy optimal speed profile of a generic multi-speed device with a discrete set of speeds, to execute a given task within a given time. Current implementations of energy efficient speed control policies (including DVFS) almost exclusively use the minimum feasible speed pair, which has been shown before to be suboptimal. Unlike previous works, ours does not require an explicit functional relationship between the device's power and speed (e.g. the CMOS power model), but only assumes that the power-speed relationship is a W-convex (a discrete equivalent of a convex) function. This assumption allowed us to show that the optimal speed profile uses at most two speeds, and that all the essential characteristics of the power-speed relationship can be encapsulated within a single speed, wu. The latter speed is intrinsic to the device (i.e. task independent) and can be readily computed from its power-speed values (without any curve fit). Further, wu is also the speed at which the the device consumes the least energy per unit work done. The problem formulation reduces to a linear program in the number of supported speeds, which in general, is difficult to solve analytically. However, the optimum solution has a very simple form – it is either wu, or the minimum feasible speed pair for the given task. We verified that a number of commercial DVFS processors, and other devices like disk drives satisfied our model of the W-convex power-speed relationship.

Keywords: voltage scaling, frequency scaling, speed control, low-power, convex functions, energy optimization

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Optimal Procrastinating Voltage Scheduling for Hard Real-Time Systems

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ABSTRACT

This paper presents an optimal procrastinating voltage scheduling (OP-DVS) for hard real-time systems using stochastic workload information. Algorithms are presented for both single-task and multi-task workloads. Offline calculations provide real-time guarantees for worst-case execution, and online scheduling reclaims slack time and schedules tasks accordingly. The OPDVS algorithm is provably optimal in terms of energy minimization with no deadline misses. Simulation results show up to 30% energy savings for single-task workloads and 74% for multi-task workloads compared to using a constant worst-case execution voltage. The complexity of the algorithm for multi-task workloads is linear to the number of tasks involved.

Keywords: Power Management, Dynamic Voltage Scaling, Real-time Scheduling, Optimization Algorithm

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Flexible ASIC: Shared Masking for Multiple Media Processors

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ABSTRACT

ASIC provides more than an order of magnitude advantage in terms of density, speed, and power requirement per gate. However, economic (cost of masks) and technological (deep micron manufacturability) trends favor FPGA as an implementation platform. In order to combine the advantages of both platforms and alleviate their disadvantages, recently a number of approaches, such as structured ASIC/regular fabrics, have been proposed. Our goal is to introduce an approach that has the same objective, but is orthogonal to those already proposed. The idea is to implement several ASIC designs in such a way that they share the datapath, memory structure, and several bottom layers of interconnect, while each design has only a few unique metal layers. We identified and addressed two main problems in our quest to develop a CAD flow for realization of such designs. They are: (i) the creation of the datapath, and (ii) the identification of common and unique interconnects for each design. Both problems are solved optimally using ILP formulations. We assembled a design flow platform using two new programs and the Trimaran and Shade tools. We quantitatively analyzed the advantages and disadvantages of the approach using the Mediabench benchmark suite.

Keywords: ASIC, interconnect, optimization

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Device And Architecture Co-Optimization for FPGA Power Reduction

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ABSTRACT

Device optimization considering supply voltage Vdd and threshold voltage Vt tuning does not increase chip area but has a great impact on power and performance in the nanometer technology. This paper studies the simultaneous evaluation of device and architecture optimization for FPGA. We first develop an efficient yet accurate timing and power evaluation method, called trace-based model. By collecting trace information from cycle-accurate simulation of placed and routed FPGA benchmark circuits and re-using the trace for different Vdd and Vt, we enable the device and architecture co-optimization for hundreds of combinations. Compared to the baseline FPGA which has the architecture same as the commercial FPGA used by Xilinx, and has Vdd suggested by ITRS but Vt optimized by our device optimization, architecture and device co-optimization can reduce energy-delay product by 20.5% without any chip area increase compared to the conventional FPGA architecture. Furthermore, considering power-gating of unused logic blocks and interconnect switches, our co-optimization method reduces energy-delay product by 54.7% and chip area by 8.3%. To the best of our knowledge, this is the first in-depth study on architecture and device co-optimization for FPGAs.

Keywords: FPGA, low power, powergating, Ptrace, Psim

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DAC05, pages 921-926

Exploring Technology Alternatives for Nano-Scale FPGA Interconnects

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ABSTRACT

Field Programmable Gate Arrays (FPGAs) are becoming increasingly popular. With their regular structures, they are particularly amenable to scaling to smaller technologies. On the other hand, there have been significant advances in nano-electronics fabrication over the past few years. In this paper we explore FPGA devices of the next decade using nano-wires and molecular switches for programmable interconnect, and compare them to traditional SRAM-based FPGAs that use pass transistors as switches (scaled to 22nm). We show that by using nano-wires and molecular switches, it is possible to reduce the area of the FPGA by 70% and improve performance.

Keywords: FPGA, nanotechnology, nanoelectronics, interconnect

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Piece-wise Approximations of *RLCK* Circuit Responses using Moment Matching

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ABSTRACT

Capturing *RLCK* circuit responses accurately with existing model order reduction (MOR) techniques is very expensive. Direct metrics for fast analysis of *RC* circuits exist but there is no such technique for *RLCK* circuits. This paper introduces a new family of MOR techniques based on piece-wise functions to capture *RLCK* circuit responses accurately using only four or five moments. The time-domain response is approximated using a piece-wise function whose pieces are simple polynomials. The proposed method is fast and guaranteed stable and it avoids the calculation of poles and residues associated with existing model order reduction techniques. Results for many different industrial netlists indicate that delay and transition time can be captured within 5% error using only four moments. To the authors' knowledge, there is no existing method that can extract as much information about *RLCK* circuits with only four or five moments.

Keywords: Interconnect timing analysis, moments, *RC*, *RLC, RLCK* circuits

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A Quasi-Convex Optimization Approach to Parameterized Model Order Reduction

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ABSTRACT

In this paper an optimization based model order reduction (MOR) framework is proposed. The method involves setting up a quasiconvex program that explicitly minimizes a relaxation of the optimal H_∞ norm MOR problem. The method generates guaranteed stable and passive reduced models and it is very flexible in imposing additional constraints. The proposed optimization approach is also extended to parameterized model reduction problem (PMOR). The proposed method is compared to existing moment matching and optimization based MOR methods in several examples. A PMOR model for a large RF inductor is also constructed.

Keywords: parameterized model order reduction, quasi-convex optimization, ellipsoid algorithm, RF inductor

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Structure Preserving Reduction of Frequency-dependent Interconnect

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ABSTRACT

A rational Arnoldi method for passivity-preserving model-order reduction (MOR) with implicit multi-point moment matching for systems with frequency-dependent interconnects is described. The structure $\mathbf{H}(s) = s\mathbf{E} - \mathbf{A} - \mathbf{K}\sqrt{f}$, which arises from frequencydependent effects in high speed interconnects, is preserved by the proposed MOR technique. Moment matching using congruence transforms and based on two types of moments that are derivatives of the transfer function w.r.t s and $\sqrt{f}$ is described. Simulation results show that the proposed approach can significantly reduce the complexity of systems with frequency-dependent elements, while retaining high accuracy in comparison to the original system in both the time and frequency domains.

Keywords: Model-order reduction, skin effect, interconnect

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Segregation by Primary Phase Factors: A Full-wave Algorithm for Model Order Reduction

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ABSTRACT
Existing Full-wave Model Order Reduction (FMOR) approaches are based on Expanded Taylor Series Approximations (ETAS) of the oscillatory full-wave system matrix. The accuracy of such approaches hinges on the worst case interaction distances, producing accurate models over a very narrow band of frequencies. In this paper we present Segregation by Primary Phase Factors (SPPF), a novel algorithm for FMOR enabling wideband interconnect impedance analysis. SPPF extracts exponential terms (primary phase factors) and then approximates the smoother remainder with an ETAS, thus resulting in good accuracies over a very wide band of frequencies. We also present a technique to improve conditioning for the required computation. Example results are given for simple interconnect structures modeled using a discretized mixed potential integral equation formulation.
Keywords: Full-wave Impedance Extraction, Model Order Reduction

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