Reliability and Design in Deep Submicron Technologies

Tuesday, March 25
10:30 am - 12:00 pm

Session Co-Chairs: Farid Najm, University of Toronto
Ajith Amerasekera, Texas Instruments

Deep submicron technology introduces strong linkages between process, design, and reliability. Papers in this session talk about the effect of process defects on chip reliability estimation, measurement of circuit delay variations due to process variability, and future trends in power supply distribution as a result of interconnect scaling.
Reducing Leakage Currents in VLSI Circuits

Tuesday, March 25
10:30 am - 12:00 pm

Session Co-Chairs: Payam Heydari, University of California, Irvine
Khorram Muhammad, Texas Instruments

Leakage currents are expected to account for significant portion of the total power consumption in VLSI circuits. This session presents a number of techniques to manage and reduce subthreshold and gate leakage currents through circuit and logic redesign.
Session 1C

SoC Methodology

Tuesday, March 25
10:30 am - 12:00 pm

Session Co-chairs:    Vamsi Srikantam, Agilent Technologies
                     Tom Chen, Colorado State University

This session addresses topics in verification and IP reuse for SoC design. The first paper proposes a behavioral-level approach to model verification that reduces CPU and memory usage versus traditional BDD-based approaches. The second paper describes a top-down methodology for extending coverage on existing commercial verification tools. The third paper illustrates IP reuse for producing high-resolution images with low-resolution sensors, reducing system cost and time to market. The concluding paper presents an IP library modeling and methodology to effectively manage system cost.
Testing of SoCs

Tuesday, March 25
1:00 pm - 3:05 pm

Session Co-Chairs:  Sreejit Chakravarty, Intel Corporation
                    Jacob Abraham, University of Texas

The papers in this session discuss issues in testing SoCs and novel techniques for BIST-based diagnosis and testing. The first papers present novel optimization algorithms for test scheduling. Fault diagnosis in BIST environment is addressed in the third paper. A novel technique to drastically reduce the dictionary size is proposed. The last paper proposes the use of reconfigurable 2D LFSR to reduce hardware overhead over previous 2D FLSR design and improves fault coverage over conventional LFSR.
Design for Manufacturability and Quality

Tuesday, March 25
1:00 pm - 3:05 pm

Session Co-Chairs: Sharad Saxena, PDF Solutions
Jay Michlin, Consultant

This session addresses current and emerging issues in design of manufacturability and quality. The DFM aspects focus specifically on lithography from both a modeling and characterization angle. The DFQ aspects focus on frameworks and design flows which can help improve the quality of semi-custom designs.
Design Considerations in Advanced Technologies

Tuesday, March 25
1:00 pm - 3:05 pm

Session Co-chairs: Ken Shepard, Columbia University
Vivek De, Intel Corporation

In this special invited session, we consider design challenges in advanced technology. The first paper in the session consider the unique issues of digital integrated circuit design in SOI technology. The second talk considers circuit metrics in the design of digital communication systems. The third talk examines the development of standard benchmarks for interconnect characterization.
Interconnect and Substrate Noise

Tuesday, March 25
3:30 pm - 5:30 pm

Session Co-Chairs: Sarma Vrudhula, University of Arizona
Amit Majumdar, Sun Microsystems

This session investigates various forms of noise in highly scaled CMOS processes. Specifically, techniques to model, characterize, and reduce both functional coupled interconnect noise and delay change due to coupling capacitance are presented. Also, substrate noise in mixed-signal systems is addressed in the final paper.
Session 3B

Impact of New Standards for Design Data Modeling and Manufacturing Interface

Tuesday, March 25
3:30 pm - 5:30 pm

Session Co-Chairs:  Andrew Kahng, University of California, San Diego
                   Tom Chen, Colorado State University

The first paper in this session describes experiences with the OpenAccess v2.0 data model. The second paper discusses from an academic viewpoint (i) the impact of new interoperability standards on academic research practices, (ii) automated benchmarking and flow optimization, and (iii) design technology reuse. The third paper presents the latest word in SEMI (OASIS, UDM) efforts to widen the design-manufacturing data pipeline. The session concludes with a panel discussion of actual impacts and possible futures for these emerging standards.
Session 3C

Package-Design Interface Challenges

Tuesday, March 25
3:30 pm - 5:30 pm

Session Co-chairs: Ali Iranmanesh, Celeritek
Ken Shepard, Columbia University

This session considers issues in the design of high-performance packaging, including electrical and thermal modelling. The last paper considers layout techniques for high-pin-count SOCs.
As rapid progress in the miniaturization of semiconductor devices leads toward chip feature sizes smaller than 100 nm, VLSI designers are inevitably faced with the growing significance of power dissipation. This session contains a number of technical results describing circuit techniques for energy analysis and measurement, power estimation with crosstalk consideration, and efficient on-chip voltage regulation.
This session begins with a paper describing an approach to computer total leakage current in large circuit blocks considering both gate and subthreshold leakage. The next paper provides a thorough analysis of low-swing current-mode logic buffers and compares them to CMOS repeaters in terms of performance and signal integrity. The final paper extends previous reduced order modeling work using transformation techniques and shows improved results over Padé approximations for a number of case studies.
The first paper describes a clocking strategy for dynamic circuits to minimize skew and polarity concerns. The second paper presents a design environment for design exploration and synthesis of analog cells. The third paper describes and illustrates the application of a new delay model for parameterized cell design.
Timing and Noise Issues in Physical Design

Wednesday, March 26
1:00 pm - 3:05 pm

Session Co-Chairs: Tanay Karnik, Intel Corporation
Rajeev Murgai, Fujitsu

For multigigaHertz VLSI design, timing and noise issues are crucial for design convergence. In this session, five papers in timing and noise are presented. First, a clock scheduling algorithm for power supply noise reduction is introduced. Second, a clock construction algorithm to reduce coupling noise is presented. Third, a timing-driven scan-chain ordering method is proposed. Later, a false alarm reduction algorithm is demonstrated. Finally, a comprehensive physical design environment is presented.
Reliability Analysis

Wednesday, March 26
1:00 pm - 3:05 pm

Session Co-Chairs:  Jayasimha Prasad, Micrel Semiconductor
                    Olof Tornblad, Infineon

This session addresses a range of device and interconnect reliability phenomena. An invited talk describes the impact of variability on device modeling in modern processes. The remaining papers deal with enhancing device reliability through process modifications, the simulation of piezoelectrics, the role of tiling on circuit performance, and the analysis of electromigration effects in signal lines.
This session investigates a number of key questions in interconnect parasitics modeling today. How does inductance actually impact circuit performance based on experimental data? How good are common assumptions about the current return path for inductance calculation? What is the impact of wiring density on performance? Finally, what is the role of random logic switching on ground bounce?
Design and Measurement Issues in Testing

Wednesday, March 26
3:30 pm - 5:30 pm

Session Co-Chairs: George Alexiou, University of Patras
Daniela De Venuto, Polytechnic of Bari

This session covers new results dealing with design and measurement for test. The first paper discusses a method for implicitly identifying all possible input patterns which could cause hazards in a combinational circuit. This will be followed by a paper which shows a method for designing efficient checking logic for detecting the effects of faults in a combinational circuit. The third paper determines the difference between the number of structurally and functionally detectable delay faults when statistical variations are taken into account, but using statistical timing models. The next paper describes a technique which automatically adjusts digital window comparators for DFT, taking into account lot-to-lot process variations. The final paper presents an embedded Iddq architecture which interfaces built-in-current sensors to the IEEE 1149.1 standard to reduce overhead.