Evening Panel Discussion*

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IC & Package Co-Design: Challenge or Dream?

Moderator
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EETimes

Organizer
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Description

In recent years, major breakthroughs have occurred in packaging technology, which have led to the industrialization of several kinds of new packages, more powerful, and yet more flexible, in the attempt to cope with the challenges posed by multi-million gates and multi-GHz systems-on-a-chip (SOC). While offering a great deal of opportunities, ball-grid array (BGA) substrates, flip-chip and multi-stacked dies require an unprecedented level of integration between IC and package design and verification.

This integration, however, requires a change in methodology, with the availability of new EDA tools, and a major shift in the profile of the designers and engineers involved which, to a certain extent, have to acquire each other competences.

Although necessary, this cannot be given for granted. While BGA is a reality, flip-chip is still a question mark for the majority of the applications, due to both cost reasons and lack of commercial EDA tools. A package re-use discipline is becoming a must to avoid a package design start for each IC design start, with expensive substrates scraps. How to implement it? Interoperability between Cadence and Synopsys and the rest of the EDA world is a key aspect, as customers don’t want to be further bound to few vendors—nor wants the FTC! How to enforce it?

This panel is not about packages nor about ICs, it’s about whether today’s electronic systems can be successfully designed and assembled in their target package, without taking into consideration each other requirements since the very early beginning. It’s about the requirements, the challenges and the on-going initiatives, if any.

Panelists

Dr. Raul Camposano, CTO, Synopsys
Carlo Cognetti, VP Corporate Package Development, STMicroelectronics
Aurangzeb Khan, VP Design Foundry, Cadence Design Systems
Dr. Lou Scheffer, Architect, Cadence Design Systems
Nitin Deo, VP Business Development, Magma Design Automation

*Sponsored by Advanced Packaging/PennWell
Dr. Raul Camposano, CTO, Synopsys

Packaging has not been a primary focus of EDA, due to the fact that wire bonding has scaled well in the past and automation of package design wasn’t a real necessity. But with skyrocketing I/O counts (thousands of pads increasing at 10% year) which require flip-chip ball grid-arrays, complex substrates (~10 layers), very high speeds (several GHz), stacked dies (more than 2) and very high volumes (billions), the time has come for EDA to increasingly focus on package design. Packaging can impact device performance severely and can contribute over half to the device cost. The main technical problems that need to be addressed are:

- Optimizing the I/O plan for both chip and package simultaneously (signal assignment and placing I/O cells and bump pads), taking into account given constraints;
- Automatic multi layer routing of the substrate;
- Modeling the complete signal transmission and power distribution path including die and package.

While these problems are not new to EDA, including the package requires bi-directional integration with the design data base and the package information, better modeling of inductance, better “pin assignment” algorithms, etc. The resulting tools must provide the capability to evaluate and coordinate packaging during the early stages of chip design, to optimize the die/package interface, and ultimately to lower cost, reduce cycle-time, and enhance overall device performance.

Coordinated, concurrent chip, package, and substrate co-design will replace the current independent practices, otherwise packaging will become a limiting factor in the continued evolution of overall semiconductor technology. EDA will respond to these challenges.”

Carlo Cognetti, VP Corporate Package Development, STMicroelectronics

Global semiconductor companies, such as STMicroelectronics, which design and manufacture a broad range of semiconductor integrated circuits (ICs) used in a wide variety of microelectronics applications, always strive to get the most they can out of their back-end manufacturing plants. To put things in perspective, in year 2000 ST assembled 10+ billions of units, roughly 300 units per second. The huge pressure for always lower costs—of paramount importance to address emerging markets such as China—and the high volumes required to make flip-chip economically worth from a back-end manufacturing stand-point, make wire bonding the preferred choice whenever possible. While wire bonded ICs with I/O density up to 1,000 and performances up to several GHz are within our reach, new tools to identify the exact threshold, which makes flip-chip mandatory, are urgently needed.

Concerning advanced packaging technologies, ball-grid arrays (BGA) substrates, while offering unprecedented possibilities of package and IC co-design, often lead to a new substrate design start—hundreds of designs starts! —for each new IC design start, with little chances of re-use and potential substrates’ scraps, should the IC design don’t go through. Flip-chip BGA (fcBGA) do not make things any better: bumping rules are worse than bonding rules, package-level parasitic extraction and electrical characterization need to take into proper account redistribution layer(s), mutually induced substrate noises between package and IC must be modeled and characterized. Not to mention the design, verification and manufacturing challenges posed by stacked dies, up to four, sometimes mixing wire bonding and flip-chip. Again, new tools are urgently needed as to avoid the big deal of opportunities that are ahead of us to be killed by un-addressed issues.

Collaboration between semiconductor and EDA industry is necessary in order to make key ingredients, such as concurrent package and IC physical design and full package and IC parasitic extraction and electrical characterization, available shortly.
Aurangzeb Khan, VP Design Foundry, Cadence Design Systems
Current system-on-chip ICs for networking and optical telecommunications systems are typically packaged in flip-chip BGA packages with ~2,000+ bumps, ~3,000 - 4,000+ on-chip pads and 3-7+ layer custom substrates. I/O data rates range from ~200 MHz to 3.125 GHz, with 10 GHz signal rates required over the next year. These devices typically dissipate 10 - 25 watts of power at very low voltage levels, hence requiring the flow of many amperes of current in and out of the chip/package/board combination.

In addition to addressing single signal electrical properties, including analog signaling and impedance management, we need to address the effects of simultaneously-switched inputs and outputs, package capacitance, the interaction between signal and image currents, differential signaling performance and cross-chip VDD/VSS differentials, as well as thermal properties across the chip/package/board system, to ensure a smooth and reliable transition to volume production. Modeling the complete signal transmission and power distribution path (including the effect of current flow in die substrate) is critical to achieving technical design requirements.

Today, such needs are inadequately addressed, making this critical aspect of design engineering a weak link in the product delivery chain for advanced systems.

Dr. Lou Scheffer, Architect, Cadence Design Systems
Package/IC design is a complex field, with many differing requirements. Here are some problems that are being addressed more or less successfully, then some problems that need more work.

Electrical analysis: given the package layout and materials, existing tools can build electrical models for the package and simulate them. Improvements are always welcome, particularly in speed of analysis and capacity, but the basic capability exists in commercially available products. Chip design with an existing package: this basically boils down to pin assignment, which has existed for many years. Flip-chip is not as mature but presents few fundamental problems. Design a package where the chip is king: here the package must adapt to the wishes/needs of the chip. Existing packaging tools can handle this, though improvements in electrically driven routing and inter-tool operability are needed.

However, there are package design problems that are addressed poorly, if at all. True co-design: given a blank slate, design a package and chip(s) for lowest total cost, or best cost/performance. This should trade off performance and cost between the elements, and find pin locations satisfactory to all. This is an extremely hard problem, not least because it requires expertise not commonly found in one organization, let alone one person. It’s also not a high volume tool, so expect this to be done by experienced designers for some time. Tool interoperability: Package descriptions are moving to XML, and IC design to integrated databases, but the two need to communicate. This is a problem of engineering time and resources, but is not fundamentally difficult, and users can expect a solution. Chip/package tradeoff analysis: very early in the design process, users and manufacturers would like to get at least some visibility into packaging issues and possible solutions, in the spirit of the chip prototyping tools now available. Such a tool must be fast and easy to use, with reasonable accuracy. All in all, between enhancing existing tools and creating new ones, there is lots of room for progress in IC/package co-design.

Nitin Deo, VP Business Development, Magma Design Automation
A designer’s job is not finished until his/her chip is actually running in the system with a built-in reliability for high volume production. Everyone keeps talking about Time-To-Market, but if you ask the designers, they will tell you that Time-To-Volume is even more important. A high quality package with a high quality chip in it reduces that time to volume.

Many years ago there were innovative packaging technologies such as multi-chip module (MCM). There were many issues with respect to design (chip design), reliability (of the whole package) and then design-for-reliability in those systems. Designers ran into these issues as they were pushing the technology envelope at that time. Its funny how history repeats itself. Today’s nanometer chips, which carry millions of transistors at clock speeds exceeding GHz and I/O count exceeding 2000 pins, embody the entire system—hence some people call it System-In-a-Package. When this system has to reliably go to high volume production, the same issues come into picture. Even the simplest things like partitioning the design have a major impact when the chip has to go into a 2000-pin flip-chip package with area I/Os. Then there are other detailed issues such as clock routing, power management and routing, etc. So, the bottom line is that EDA vendor’s job is not finished until the designer’s job is finished!