An Embedded I_{DDQ} Testing Architecture and Technique

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Abstract

In this paper an embedded I_{DDQ} testing architecture is presented that targets to overcome the excessive hardware overhead requirements in built-in current sensing based testing applications. Moreover, a technique that utilises the IEEE 1149.1 boundary scan standard to control the proposed architecture is provided. The proposed solution is characterised by low silicon area requirements and permits the application of I_{DDQ} testing also in case that the chip is mounted on a printed circuit board.

Index terms: I_{DDQ} Testing, Design for Testability (DFT), Boundary Scan, IEEE 1149.1

1. Introduction

I_{DDQ} testing is an effective testing technique [1], which is based on the observation that defect free CMOS circuits exhibit lower quiescent (or I_{DDQ}) current compared to defective ones, for a wide range of defect types. Thus an excessive quiescent current in a circuit under test (CUT), outside the specified limits, can be treated as an indicator of a defect presence. In I_{DDQ} testing the target is to detect the existence of these excessive currents.

The effectiveness of I_{DDQ} testing in very deep submicron technologies is threatened by the increased transistor sub-threshold leakage current. Various techniques have been proposed [2-5] aiming to reduce the leakage current and make I_{DDQ} testing feasible in future technologies. A promising approach towards this direction is the partition of the power supply of a CUT and the test of each partition separately. A major limitation of this technique in external I_{DDQ} testing schemes is that the number of the required power partitions, in high performance technologies, exceeds the number of the power pins [6]. Recently, in [7] and [8] a design methodology was presented which provides control on the power supply lines of the embedded cores in a circuit, utilizing the JTAG boundary scan, for external I_{DDQ} testing purposes. The target of this technique is to minimize the accumulative current of multiple static current dissipating cores during I_{DDQ} testing. This is achieved by using control signals to selectively switch-off the power supply lines of all the cores in the circuit except the core under test. The disadvantage of this approach is that for large cores under test the problem of high leakage currents during I_{DDQ} testing still exists.

Alternatively, circuit/core partitioning and Built-In Current Sensors (BICSs) can be used for embedded I_{DDQ} testing. BICSs seem to be attractive for high speed I_{DDQ} testing. A series of BICSs' designs have been proposed in the open literature [9-15]. In the BICSs based I_{DDQ} testing approach the power supply network of a circuit is logically partitioned within the chip, using a dedicated current sensor per partition [9, 16]. A drawback of this scheme is that the required silicon area for BICSs implementation can be extremely high [6].

In this paper we propose an embedded I_{DDQ} testing architecture and technique that reduces the number of required BICSs in partition based I_{DDQ} testable designs. Potentially this number can be reduced down to one. According to this approach only one of the circuit partitions (sub-circuits) is connected each time to the BICS for I_{DDQ} testing. Consequently only the leakage of this sub-circuit under test affects the I_{DDQ} current measurement. Limiting properly the size of each sub-circuit we can overcome the problem of high leakage currents when I_{DDQ} testing is performed. The proposed scheme can be extended to cooperate with the IEEE 1149.1 boundary scan (JTAG) standard [17] in order to control the testing process with the minimum cost on pin count. Utilizing this approach, I_{DDQ} testing can be also applied even when the chip is mounted on a board.

The paper is organised as follows. In section 2 the proposed I_{DDQ} testing architecture is presented while in section 3 the corresponding technique to utilize the IEEE 1149.1 standard as the control vehicle for this architecture is given. In section 4 the requirements to perform I_{DDQ} testing in future technologies and the applicability of the proposed scheme are discussed. Finally, in section 5 the conclusions are drawn.

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2. The proposed I_{DDQ} testing architecture

The proposed I_{DDQ} testing scheme is illustrated in Fig. 1. The CUT is partitioning into sub-circuits. A single BICS is used for the current monitoring of these sub-circuits or in general for a group of sub-circuits. The BICS is connected to the sensing node (virtual ground) of each Sub-Circuit Under Test (SCUT) in a group via a common sensing line (SL) and through the pass transistors MT_i ($i \in 1 \ldots n$) that are in the conducting state whenever the corresponding sub-circuit is tested. Only one sub-circuit in a group is under test each time. The rest sub-circuits are connected to the ground (V_{SS}) through the pass transistors MN_i ($i \in 1 \ldots n$).

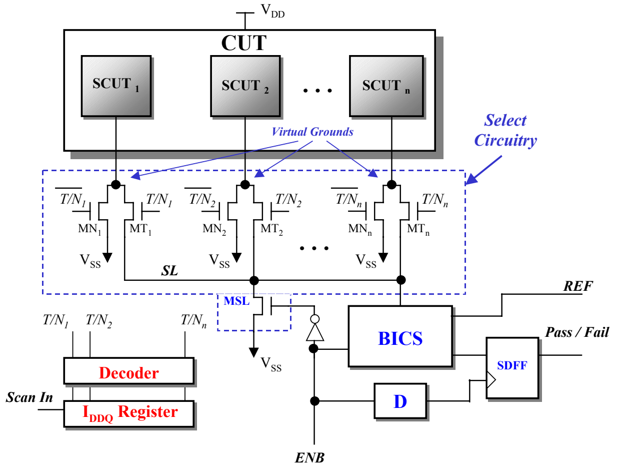

Figure 1: The proposed I_{DDQ} testing scheme

The selection of the sub-circuit under test (SCUT) can be achieved using a register (I_{DDQ} register). Its status provides through a decoder a unique selection signal (T/N_i) ($i \in 1 \ldots n$) for each SCUT, which prohibits the virtual ground of this SCUT to be connected to the ground and connects it to the sensing line SL of the BICS. Obviously, another option is to assign a specific bit of the register to each SCUT and omit the decoder. The all zero state of the I_{DDQ} register corresponds to the normal mode of operation. Whenever the decoder provides a high value on its outputs the CUT turns in the test mode of operation and the corresponding SCUT is selected for current monitoring through the Select Circuitry (see Fig. 1). In parallel the BICS is activated with the enable signal (*ENB*) raised to high. A sample D flip-flop (SDFF) at the output of the BICS is used to capture the response of the sensor. Furthermore, a delay element (D), which is driven by the ENB signal, is used to feed the clock input of the flip-flop in order to sample the BICS pass/fail output after the required sensing time has elapsed. Finally, the complementary signal of *ENB* is used to ground the sensing line SL, through the MSL transistor, whenever the BICS turns to be inactive.

According to this scheme a single BICS or a small number of BICSs are used for I_{DDQ} testing. This approach provides a solution to the hardware overhead drawback when the number of required partitions is large. In future technologies the demand of large numbers of partitions, in order to overcome problems during I_{DDQ} testing related to the excessive static leakage currents of CMOS circuits, will be imperative [6].

Note that in the classical embedded I_{DDQ} testing architecture dedicated BICS are used for each sub-circuit and each test vector is capable to exercise in parallel all the sub-circuits of the circuit. Contrary to this scheme, in the method proposed here the sub-circuits of each group are tested successively one after the other. However, the introduced extra test time penalty, compared to the classical approach, does not imply any major limitations since the number of required test vectors for the I_{DDQ} testing of a circuit is quite small [8, 18]. Moreover, if each BICS is to provide its response on a scan chain, then the cost of this scan chain alone will be too large to be acceptable for the classical approach [6]. Thus also in that case an extra test application time penalty will be paid in order to exploit a shared scan chain among a number of BICS. This penalty is due to the fact that only a subset of the partitions is tested in every test vector application. This extra test time is comparable to that of the proposed in this work technique.

Finally, aiming to avoid problems related to the use of a single reference current by the BICS, an extra pin (*REF*) can be utilised to provide, during testing, the proper reference current according to the actual test vector and the active SCUT.

3. Cooperation with the IEEE 1149.1 std

Considering the proposed in the previous section scheme, a drawback arises by the demand of an additional shift register, a decoder and extra test pins to control the I_{DDQ} testing process. Although the hardware overhead is negligible, the pin count is of great concern being a main limitation of today and future chips. In order to avoid the large cost related to the extra pins, the IEEE 1149.1 boundary scan standard can be utilised. Taking into account that the standard may be already present due to other testing purposes the actual cost is reduced drastically.

In that case the I_{DDQ} register is treated as one of the design specific data shift registers of the standard. The architecture of the proposed I_{DDQ} testing approach is presented in Fig. 2. In this figure the I_{DDQ} Register and the rest registers that belong to the standard like, the Instruction Register (IR) with its Decode Logic, the Bypass Register, the Boundary Scan Register (BSR) and the Device ID Register, are illustrated. Note that the SDFF flip-flop, where the BICS's response is captured, is also considered as another design specific one bit data shift register.

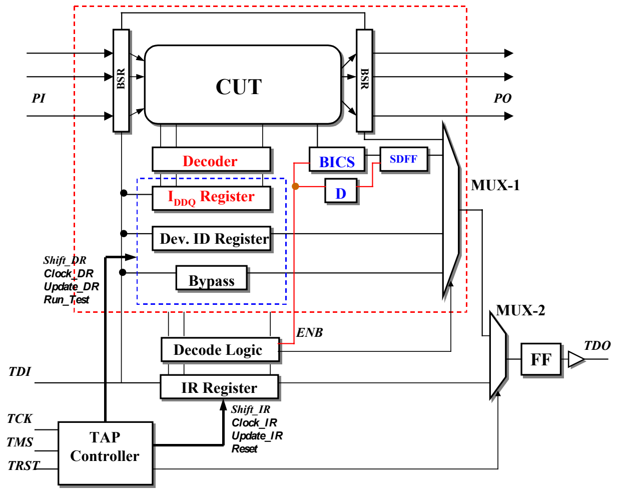

Figure 2: IEEE 1149.1 based architecture to support I_{DDQ} testing

The required user-defined instructions that must be loaded in the IR register in order to apply the proposed I_{DDQ} testing technique are:

- *IDDQ-Register_Load*: This instruction scans in a pattern to the I_{DDQ} Register.
- *Execute*: This instruction activates the *ENB* signal so that an I_{DDQ} testing operation to be performed.
- *Read_Result*: This instruction enables the content of the SDFF (Pass/Fail signal) to be scanned out at the TDO pad of the chip.

Utilising the above instructions, the procedure to perform a complete I_{DDQ} testing operation is as follows:

1. Initially, the selected test vector is applied to the primary inputs of the CUT utilizing the facilities of the IEEE 1149.1 std.
2. A pattern capable to activate the proper SCUT is shifted into the I_{DDQ} Register using the *IDDQ-Register_Load* instruction.
3. An I_{DDQ} testing operation is performed and the result is captured in the SDFF utilising the *Execute* instruction.
4. The contents of the SDFF are shifted through the multiplexers MUX-1 and MUX-2 to the TDO pad utilising the *Read_Result* instruction. In this step information regarding the pass/fail decision of the I_{DDQ} testing process is provided to the external environment of the chip.
5. If more sub-circuits can be tested with the same test vector, the steps 2 to 4 are repeated inserting the proper patterns into the I_{DDQ} Register.
6. The steps 1 to 5 are repeated for each test vector of the selected test set for I_{DDQ} testing.

In Fig. 3 a flow diagram of the above procedure is provided. At the end of a complete I_{DDQ} operation the I_{DDQ} Register is forced to the all zero state and the CUT turns to the normal mode of operation. Obviously, also during every start up of the circuit the proper reset operation on the I_{DDQ} Register must be performed.

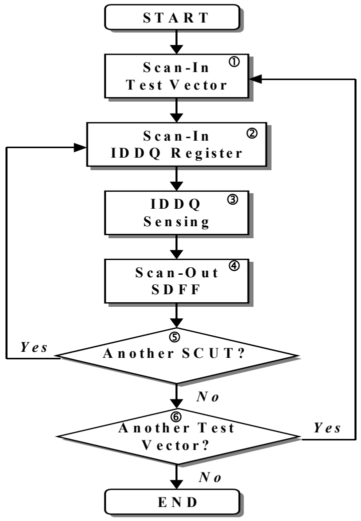

Figure 3: Flow diagram of the I_{DDQ} testing operation

4. Discussion

According to the projections of the 1999 International Technology Roadmap for Semiconductors (ITRS) [19], circuit partition requirements are presented in [6]. Thus, 86K. 337K, 1.35M and 10.5M partitions/chip are reported for the 100nm, 75nm, 50nm and 35nm technology nodes respectively, in the case of high performance, high transistor count MPUs. Note that in the classical embedded I_{DDQ} testing technique the number of required BICSs is equal to the number of the partitions in the circuit.

Considering the above partitions/chip requirements, the number of circuit partitions (CP) per group for various numbers of groups is provided in Table I according to the proposed in this work architecture. Taking into account that a test set of 100 test vectors is efficient for I_{DDQ} testing [8], the required test sessions (TS) for the complete I_{DDQ} testing of the circuit are also presented in Table I. As test session we define the application of a test vector along with the subsequent I_{DDQ} current monitoring phase. Since the corresponding test application time of few thousands test sessions is acceptable for I_{DDQ} testing, we can observe from Table I that it is feasible to achieve even more than one order of magnitude reduction in the required hardware overhead for BICS implementation. Realistic configurations for the proposed here architecture are underlined in the table.

For instance, in the 70nm technology it is feasible to achieve a reduction of more than 30 times in the related hardware overhead with a demand of 3400 test sessions or a reduction of more than 3 times using only a number of

400 test sessions. Note that the necessary number of test sessions per architecture configuration has been calculated based on the hypothesis that the whole test set must be applied to each partition. Actually, only a subset of these test vectors is required and consequently the number of test sessions is expected to be quite smaller. Furthermore, in order to exploit the parallelism of the classical approach a scan chain of 337K stages is necessary while in our scheme 10K or 100K wide scan chains, for the two mentioned alternatives respectively, are enough. For even deeper submicron technologies the scan chain requirements makes the classical technique impractical.

5. Conclusions

In this paper we presented an embedded I_{DDQ} testing architecture and technique aiming to overcome the excessive hardware requirements related to the BICS implementation in the case of partition hungry designs.. Exploiting this architecture a relatively small number of BICSs can be used for the I_{DDQ} testing of large circuits with a high count of partitions. In addition a technique to utilise the well-known IEEE 1149.1 standard in order to control the proposed scheme is illustrated. According to this technique a set of user-defined instructions are introduced and applied through the standard providing the ability to disconnect each sub-circuit under test from a power supply line (V_{DD} or V_{SS}) and connect it on the BICS to perform the testing operation. Thus a programmable sharing of the BICS resources is available while in parallel the hardware overhead requirements are reduced drastically although as a trade-off to the test application time. Furthermore, this reduction offers the ability to implement more accurate current sensing circuits in order to cope with hard to detect defects as well as various constrains in BICS design. Finally, this boundary scan based I_{DDQ} testing approach enables the application of I_{DDQ} testing throughout the useful lifetime of a chip even when it is mounted on a circuit board.

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Table I

Circuit partitions per group (CP) / Required test sessions (TS)

Technology	**100nm**		**70nm**		**50nm**		**35nm**	
Groups or # BICS	**CP**	**TS**	**CP**	**TS**	**CP**	**TS**	**CP**	**TS**
1	86K	8.6M	337K	33.7M	1.35M	135M	10.5M	1.05B
10	8.6K	860K	33.7K	3.37M	135K	13.5M	1.05M	105M
100	860	86K	3.37K	337K	13.5K	1.35M	105K	10.5M
1K	***86***	***8.6K***	337	33.7K	1.35K	135K	10.5K	1.05M
10K	***9***	***900***	***34***	***3.4K***	135	13.5K	1.05K	105K
100K	-	-	***4***	***400***	***14***	***1.35K***	***105***	***10.5K***
1M	-	-	-	-	***2***	***200***	***11***	***1.1K***