Analyzing Internal-Switching Induced Simultaneous Switching Noise

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Abstract

***T**he internal-switching induced simultaneous switching noise (SSN) is studied in the paper. Unlike ground bounce caused by driving off-chip loading, both power-rail and ground-rail wire/pin impedances are important in evaluating internal SSN, and the double negative feedback mechanism should be accounted for. Based on the lumped-model analysis and taking into account the parasitic effects and velocity-saturation effect of MOS transistors, a novel analytical model is developed which includes both switching and non-switching gates. The proposed model is employed to analyze on-chip decoupling capacitance, wire/pin inductance effect and loading effect analytically. Good agreements with SPICE simulations are obtained for submicron technology.*

1. Introduction

Simultaneous switching noise (SSN), also known as ground bounce, *di/dt* noise, is one major noise source in modern digital and mixed-signal circuit design. It's generated at the power/ground distribution connections within a chip due to switching currents passing through the parasitic inductance of the package or wire. This voltage surge is spread to other circuits through power rails and substrate, causing malfunction or performance degradation. Traditionally, SSN is associated with the drivers that drive the output buffer. However, as the circuit density and speed keep increasing, the SSN due to internal gate switching becomes a serious problem in digital design [1].

Some works have been done [1-4] to analyze the SSN effects caused by the internal gate switching. Larsson [2][3] examined the maximum peak voltage of SSN using long-channel MOS models and simplified circuit. Chang et. al [1] investigated SSN effects based on the simulation observations. Gomez et. al [4] derived analytical equations of SSN using short-channel MOS model. However, their method only considered the negative feedback for nMOS, and moreover, they neglected the impact of the power-rail bond wire / pin impedance and hence lost accuracy.

In this paper, the ground bounce due to internal gate switching is analyzed accurately. The power-rail and ground-rail pin impedances are both involved in evaluating the ground bounce. Double negative feedbacks [2] for nMOS and pMOS are considered. The velocity-saturation effects and the parasitic effects of short-channel transistors are included. The proposed method analyzes the influence of both switching and non-switching gates, and it's applied for extended analysis, such as capacitive decoupling, inductance effect and loading effect. Since it has been found that gate delay mainly depends on the first peak of the ground bounce [5]. This first peak voltage is the main concern of this paper.

In the following sections, section 2 investigates the importance of including the power-rail pin impedance in evaluating internal SSN. Section 3 provides the details of modeling ground bounce. The proposed analytical model is employed for circuit analysis and validated by SPICE simulations in Section 4. Finally, the summary is given in Section 5.

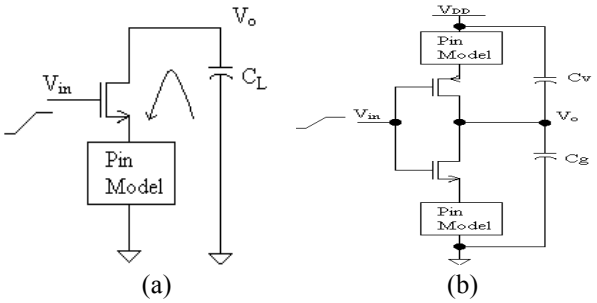

Figure 1. (a) Equivalent switching circuit model for SSN due to driving the output buffer, which is simplified from circuit (b)

2. Lumped Model Analysis

As mentioned before, there are two sources that can generate simultaneous switching noise. When the output buffer is considered, the ac equivalent circuit, shown in Figure 1(a), is often employed for the input transition from 0 → 1 [6][7]. It's simplified from the circuit in Figure 1(b) with the assumption that pMOS transistor is

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in the cut-off region and $C_L = C_g + C_v$. Since capacitances C_v and C_g are off-chip loading and all drain currents of MOS transistors go to the parasitic pin impedances, the equivalent circuit in Figure 1(a) provides good accuracy without considering the impedance of the power-rail pin model. However, if the SSN due to internal gate switching is considered, this method is invalid because the signal bounce in power rail is not negligible [2].

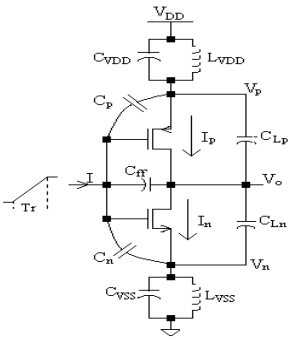


Figure 2. Circuit model to evaluate SSN due to internal gate switching

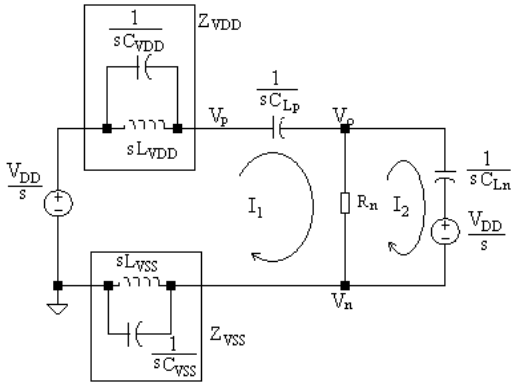


Figure 3. Lumped-model circuit to evaluate SSN due to internal gate switching

Consider the circuit shown in Figure 2 [4], where LC pin models are used for both power rail and ground rail, C_{Ln} (C_{Lp}) includes the load capacitance of fan-outs and wire capacitance. The equivalent gate-to-drain capacitance C_{ff} is the sum of C_{gd} from both nMOS and pMOS transistors. C_n (C_p) is the gate-to-source and gate-to-substrate capacitances for nMOS (pMOS). Due to the input transition from 0 → 1, the nMOS transistor is turned on and pMOS is turned off. The equivalent lumped-model circuit is drawn in Figure 3, where all elements are represented by their complex-frequency domain models [8]. Using the loop current law, the ground and power bounces are expressed as

$$V_n = Z_{VSS} \cdot I_1 \tag{1}$$

$$V_p - \frac{V_{DD}}{s} = -Z_{VDD} \cdot I_1 \tag{2}$$

Z_{VDD} and Z_{VSS} are the impedances of the ground pin model and power pin model, respectively.

Assume symmetric power and ground pin model ($L_{VDD} = L_{VSS}$, $C_{VDD} = C_{VSS}$), and note that the inverse Laplace transformation of (V_{DD}/s) is V_{DD} for t ≥ 0, Equations (1) and (2) imply the symmetric bounce signal on the power rail and ground rail, and the phase difference between them is 180° [9]. It's obvious that when SSN due to internal gate switching is considered, the signal bounce on the power rail is as significant as that on the ground rail, and both the power-rail and ground-rail pin impedances contribute to these voltage surges.

3. Modeling the Ground Bounce

3.1. Ground Bounce of Switching Gates

As mentioned in Section 1, the first peak of the ground bounce is the major concern of this paper. For the input rising ramp depicted as $V_{in} = (V_{DD}/Tr)t = kt$, this peak occurs when nMOS operates in the saturation region while pMOS is in the cut-off region, or when nMOS is in saturation but pMOS is in the linear or saturation region. These operation modes are dependent on the input-signal and loading. For the internal gate transitions, as the input transition time is comparable with the output transition time, the first peak of ground bounce usually occurs when nMOS is in the saturation region while the pMOS current is negligible [10].

As the noise generated on the power and ground rails, the input signal of the internal gates is not ideally full swing. Two negative feedback effects need to be considered. One is from the ground bounce V_n, which reduces the effective voltage of V_{gs} of nMOS (falling output is assumed) [11]. Another is from the power-rail bounce V_p, which is symmetric of V_n and hence reduces the high voltage to $V_p = V_{DD} - V_n$. Applying Kirchoff current law to the nodes in Figure 2, and neglecting the short-circuit current [4], the following differential equations are setup for n simultaneous switching inverters that share the same internal ground rail and power rail

$$C_{Vp}\frac{d^2V_P}{dt^2} + C_d\frac{d^2V_n}{dt^2} - nC_{Lp}\frac{d^2V_o}{dt} - \frac{V_{DD}-V_p}{L_{VDD}} + n\frac{dI_p}{dt} = 0$$

$$C_{Lp}\frac{d^2V_p}{dt^2} + C_{Ln}\frac{d^2V_n}{dt^2} - C_{Vo}\frac{d^2V_o}{dt^2} - \frac{dI_n}{dt} + \frac{dI_p}{dt} = 0$$

$$C_b\frac{d^2V_p}{dt^2} - C_{Vn}\frac{d^2V_n}{dt^2} + nC_{Ln}\frac{d^2V_o}{dt^2} - \frac{V_n}{L_{Vss}} + n\frac{dI_n}{dt} = 0$$

where $C_d = C_b = nC_p$

$C_{Vp} = C_{VDD} + nC_p + nC_{Lp}$

$C_{Vo} = C_{Lp} + C_{ff} + C_{Ln}$

$$C_{Vn} = nC_{Ln} + C_{VSS} - nC_p - nC_{ff}$$

C_{Vp}, C_{Vo} and C_{Vn} are the total effective capacitance connected to the V_p node, V_o node and V_n node, respectively.

Using the approximations derived in Section 2 and note that C_{Lp}, C_{Ln} >> C_{ff}, C_p, the above equations are simplified. The resulting differential equation for V_n is

$$\frac{d^2V_n}{dt^2} + 2p\frac{dV_n}{dt} + \omega_o{}^2 V_n = q \qquad (3)$$

where $p = \frac{nK_c C_{fo}{}^2}{C_{eq}{}^3}$ $q = \frac{nkK_c C_{fo}{}^2}{C_{eq}{}^3}$ and

$$\omega_o{}^2 = \frac{C_\omega{}^2}{C_{eq}{}^3 L_{VSS}} \qquad (4)$$

$$C_{fo}{}^2 \approx (C_{VDD} - nC_p)C_{Lp}$$

$$C_\omega{}^2 \approx (C_{VDD} - nC_p)(C_{Ln} + C_{Lp})$$

$$C_{eq}{}^3 \approx (C_{Ln} + C_{Lp})(n^2 C_p{}^2 + C_{VDD}{}^2) + nC_{Lp}C_{Ln}(2C_{VDD} - nC_p)$$

K_c is from the α power model of nMOS transistor in the saturation region, where it's expressed as $I_n = K_c(V_{gs} - V_{tn})^\alpha$ (assume α ≈ 1for the submicron device) [10].

The solution of Equation (3) depends on two operation regions [4]. If $p^2 < \omega_o{}^2$, the noise is weak and $\omega = \sqrt{\omega_o{}^2 - p^2}$. Otherwise, the noise is strong and $\omega = \sqrt{p^2 - \omega_o{}^2}$. Therefore, unlike prediction made in [5], $\omega \approx \omega_o$ stays only when noise is very samll. For weak noise, two cases are considered according to the different time point that the first peak of ground bounce occurs.

- CASE A: Since the load capacitance of the internal gate is usually small, the first peak of ground bounce occurs before the input signal reaches V_{DD}. The solution to Equation (3) is

  $$V_n = \frac{q}{\omega_o{}^2}[1 - e^{-pt}(\cos(\omega t) + \frac{p}{\omega}\sin(\omega t))] \qquad (5)$$

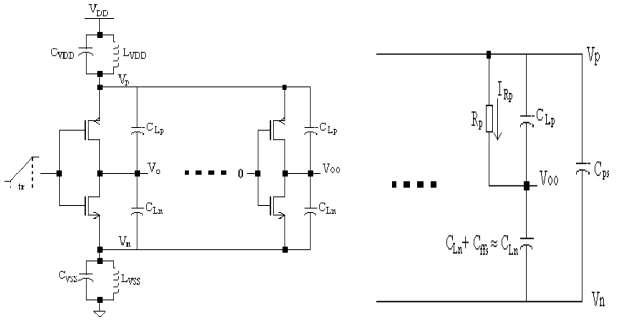
  It's straightforward to find out that the first peak of V_n is:

  $$V_{npeak} = \frac{q}{\omega_o{}^2}(1 + e^{-\frac{p\pi}{\omega}}) \qquad (6)$$

- CASE B: Under certain circumstance, the first peak of ground bounce may occur after the input signal reaches V_{DD}. The solution to Equation (3) is

  $$V_n = e^{-pt}[V_{no}\cos(\omega t) + \frac{V_{no}' + pV_{no}}{\omega}\sin(\omega t)] \qquad (7)$$

where V_{no} and V_{no}' are V_n and the first-derivation of V_n at the time point when input reaches V_{DD} (assuming no delay on the input signal). They are solved from Equation (5) and used as the initial conditions in deriving Equation (7).



(a) (b)

Figure 4(a) Circuit model includes both switching and non-switching gates, and (b) simplified circuit from (a) for non-switching gates.

3.2. Ground Bounce Including Non-switching Gates

When SSN is evaluated, the importance of the non-switching gates need to be addressed [1] [5]. Figure 4(a) depicts one inverter which has stable input during SSN period (input LOW is assumed). In this case, pMOS is usually in the linear region and nMOS is off. The circuit is reduced to Figure 4(b), where parasitic capacitances are also shown. Their notations are similar to those in Figure 2. [5] further simplified circuit in Figure 4(b) to a single capacitance C_{Ln} by assuming that (1) R_p is much less than the impedances of C_{Ln} ($1/\omega C_{Ln}$) and C_{Lp} ($1/\omega C_{Lp}$), which is not always true because the pMOS device is used for internal gates and thus can be very small; and (2) effective decoupling capacitance (C_{eff}) is much larger than the C_{Ln} and C_{Lp} of non-switching gates. As the number of non-switchings increases, their total parasitics increase and this assumption is no longer valid. Considering m non-switching gates along with n switchings, the differential equations in Section 3.1 are changed slightly with an extra item $m\frac{C_{Ln}}{C_{Ln} + C_{Lp}}\frac{dI_{Rp}}{dt}$, and

$$C_{Vp} = C_{VDD} + nC_p + (n+m)C_{Lp} + mC_{ps} - m\frac{C_{Lp}{}^2}{C_{Lp} + C_{Ln}}$$

$$C_{Vn} = (n+m)C_{Ln} + C_{VSS} + m(C_{ps} - \frac{C_{Ln}{}^2}{C_{Lp} + C_{Ln}}) - n(C_p + C_{ff})$$

$$C_d = nC_p - m(C_{ps} + \frac{C_{Lp}C_{Ln}}{C_{Lp} + C_{Ln}})$$

$$C_b = nC_p + m(C_{ps} + \frac{C_{Lp}C_{Ln}}{C_{Lp}+C_{Ln}})$$

The resulting equation for V_n is similar to Equation (3) except that

$$p = \frac{2nK_c{C_{fo}}^2 + TC\omega^2}{2{C_{eq}}^3}$$

where $T\frac{dV_n}{dt} = m\frac{C_{Ln}}{C_{Lp}+C_{Ln}}\frac{dI_{Rp}}{dt}$.

To solve for T, the working frequency of the circuit needs to be found. Assuming the this frequency is ω, the ratio of the voltage drop on (C_{Ln}+ C_{ffs}) to the voltage (V_p - V_n) is [8]

$$\dot{U} = \frac{(1+\omega^2{R_p}^2C_{Lp}(C_{Lp}+C_{Ln})) - j\omega R_pC_{Ln}}{1+\omega^2{R_p}^2(C_{Lp}+C_{Ln})^2} \quad (8)$$

Therefore, the amplitude of the first derivation of I_{Rp} is

$$\frac{dI_{Rp}}{dt} = \frac{1}{R_p}\frac{d(V_p - V_{oo})}{dt} = \frac{2}{R_p}(1-|\dot{U}|)\frac{dV_n}{dt} \quad (9)$$

The working frequency is then found numerically by solving $\omega = \sqrt{{\omega_o}^2 - p^2}$.

For weak noise, for example, $\omega_o \geq 4p$, the working frequency ω is very close to ω_o, and ω_o is then used in Equation (8) to solve for $|\dot{U}|$ in Equation (9). The analytical solution of V_n can be found.

4. Analysis and Discussions

Based on the analytical equations derived in Section 3, the proposed model is compared with the results from Cadence SPICE simulations and the previous work. TSMC 0.18 µm / 1.8 V technology and BSIM3v3 model are employed in SPICE. From Equations (5) and (7), we find out the time point that the first peak of ground bounce occurs depends on the number of switching gates. As the switching gate increases, the noise peak will be delayed. Therefore, both CASE A and CASE B in Section 3.1 need to be considered. Figure 5 depicts one result for switching gates. Good agreement between the proposed method and SPICE simulation is obtained. The parabolic relation between the number of switching gates and noise peak is obvious due to negative feedback effect. In the meantime, the Gomez's method [4] agrees with the SPICE simulation only when the ground bounce is small. As the number of switching gates increases, Gomez's method introduces errors due to neglecting the impact of the internal power rail and the peak shift.

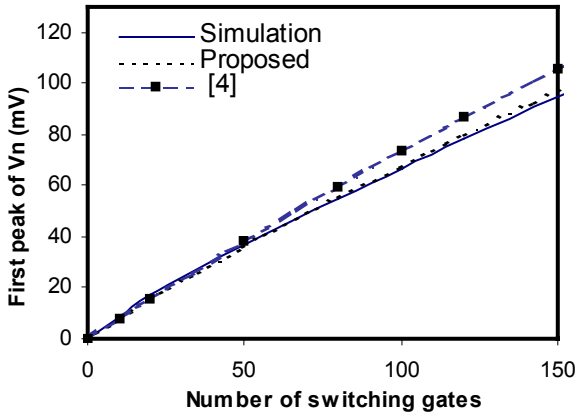


Figure 5. First peak of SSN versus the number of switching gates for different models

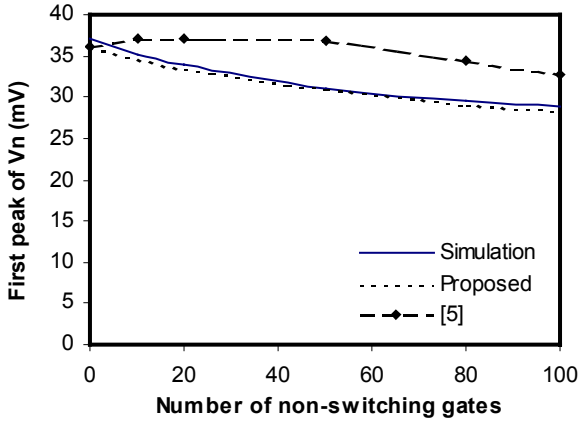


Figure 6. First peak of SSN versus the number of non-switching gates when 50 gates switch

Figure 6 illustrates the effect of non-switching gates. The simulation results are compared with the proposed method and the method in [5], where the non-switching gates are modeled as a capacitor. It's clear that the SSN is reduced as the number of switching gates holds constant (50 switching gates in Figure 6) while the number of non-switching gates increases. This is because the non-switching gates act as the capacitive impedance connected between the virtual *GND* and V_{DD} (see Figure 4(b)). It causes the redistribution of local switching charge, thus reducing currents flowing along the whole distance between switching circuit and supply pins. This is one reason that the asynchronous circuit has less SSN impact than synchronous circuit. In the proposed method, the effective resistance of pMOS (R_p) is obtained from the pMOS I-V curve when drain-to-source voltage (V_{ds}) of pMOS equals to the noise peak generated from the switching gates.

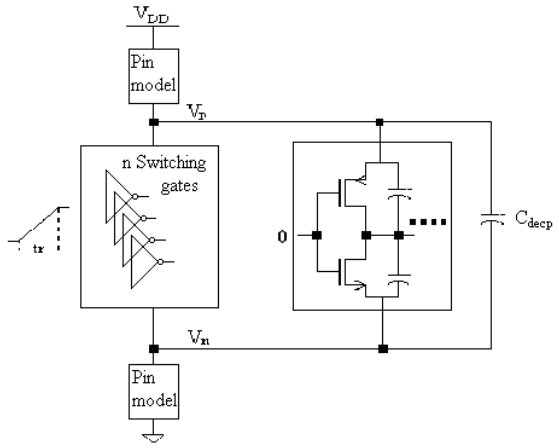


Figure 7. Circuit schematic of switching and non-switching gates along with decoupling capacitance

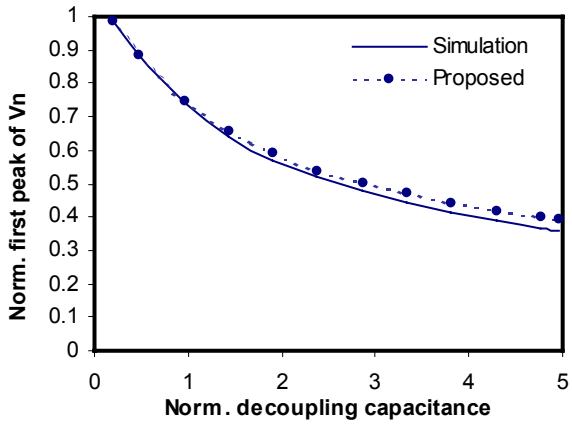


Figure 8. Normalized first peak of SSN versus normalized decoupling capacitance

The analytical results in Section 3 can be employed for extended analysis. Some of the examples are given below.

4.1. On-chip Decoupling Capacitance

On-chip decoupling is the widely accepted approach to reduce SSN. Figure 7 shows the circuit block diagram. Since the effective decoupling capacitance C_{decp}, which includes both substrate parasitic and the designer-added capacitance, is in parallel with C_{ps} s' of non-switching gates (see Figure 4(b)), the non-switching gates enhanced the capacitive impedance effectively. For simplicity, considering only switching gates with decoupling capacitance, the results from Section 3.2 are reemployed with some straightforward changes. The result is shown in Figure 8. The amplitude of the first SSN noise is normalized to the noise without the decoupling capacitance C_{decp}, and C_{decp} is normalized to the switched capacitance C_{sw} of the circuit, which is defined as $C_{sw} = C_{VDD} + C_{Vss} + n(C_{Ln} + C_{Lp})$. It's clear that in order to reduce SSN dramatically, a large capacitance C_{decp} should be used, especially when the number of switching gates (n) is large. [9] suggested C_{decp} should be 5 times larger than C_{sw} if the gate activity ratio is 1. Due to the presence of C_{decp}, the driving nMOS may exit saturation region when the first peak of SSN comes. Therefore, the proposed model overestimates the noise value for large C_{decp} because a bigger nMOS current is assumed.

4.2. Bond Wire/Pin Inductance Effect

As mentioned in section 1, SSN is also called delta-I noise because $V_{noise} = L\, di/dt$. Many researches have been done to reduce the effective pin inductance L and therefore reduce the noise, such as using multiple power and ground pins [12]. It is generally assumed that SSN is reduced linearly with the reduction of inductance L. However, it's not true because inductance L also influences the switching current. Figure 9 compares the results from simulation and the proposed method, along with the linear estimation. Considering switching gates in CASE A (see Section 3), two work regions are employed to evaluate the relationship between the inductance L and SSN.

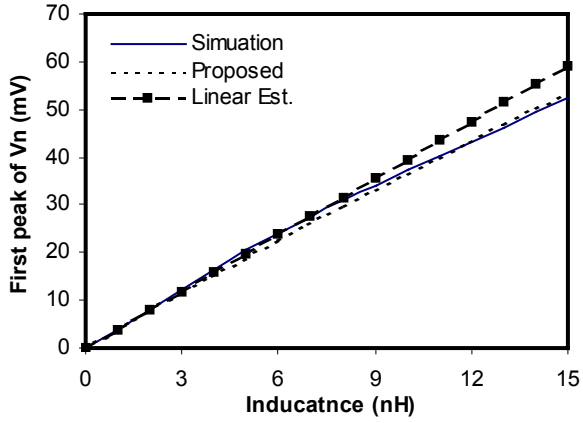


Figure 9. First peak of SSN versus wire/pin inductance

- Region A: If $p << \omega_o$, $\omega \approx \omega_o$ *and* $e^{-\frac{p\pi}{\omega}} \approx 1$. The V_{npeak} is estimated by $V_{npeak} = 2KL_{Vss}$, where $K = q\frac{C_{eq}^{\ 3}}{C_{\omega}^{\ 2}}$.

- Region B: If p is close to ω_0, $e^{-\frac{p\pi}{\omega}}$ approaches zero. The V_{npeak} is approximately depicted as $V_{npeak} = KL_{Vss}$.

For any other values of p and ω_0 between these two regions, the slope of V_{npeak}-L_{Vss} curve varies from K to $2K$. The linear estimation shown in Figure 9 is for Region A. It's accurate when inductance is small. As L increases, ω_0 and ω decrease and the slope $2K$ introduces numerous errors.

4.3. Loading Effect

As mentioned in Section 2, two capacitive loadings need to be considered when internal SSN is analyzed. For output falling transition, the C_{Ln} is discharged (see Figure 3) and most of its current goes to the nMOS in parallel with it. The C_{Lp} is charged by current I_1, and this current also goes through the GND and V_{DD} pin impedances to generate SSN [1]. Therefore, increasing C_{Lp} can increase SSN level because of large charging current, as seen in Figure 10. The value of C_{Ln} also influences SSN. As C_{Ln} increases, the output voltage V_o changes slower and hence reduces the voltage drop on C_{Lp}. Since $I_1 = C_{Lp}\frac{d(V_p - V_o)}{dt}$ and V_p is symmetric of V_n, increasing C_{Ln} will reduce SSN level, as seen in Figure 10. Again, the proposed method agrees with SPICE simulation very well.

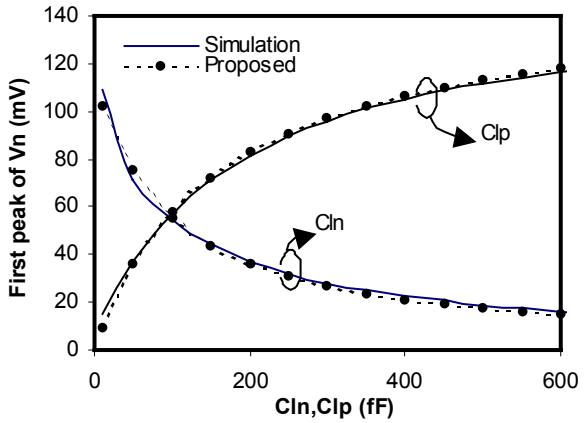


Figure 10. First peak of SSN versus capacitive load C_{Lp} and C_{Ln}

5. Summary

In this paper, the ground bounce due to internal gate switching is analyzed accurately. Unlike the ground bounce caused by driving off-chip loading, both power-rail and ground-rail impedances are important in evaluating the internal ground bounce. The lumped model predicts that the ground bounce and the power bounce are symmetric and out of phase. Using this assumption and taking into account the parasitic effects and velocity-saturation effect of MOS transistors, a novel analytical model is developed for SSN with and without non-switching gates. The proposed model is employed to analyze on-chip decoupling effect, pin inductance effect and loading effect. Some new observations have been made and explained. By comparing with SPICE simulations and previous work, the proposed method is validated for submicron technology.

6. References

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