Impact of Interconnect Pattern Density Information on a 90nm Technology ASIC Design Flow

Payman Zarkesh-Ha, S. Lakshminarayann, Ken Doniger, William Loh, and Peter Wright
LSI Logic Corporation, Device Technology Division, AJ-100, Milpitas, CA 95035, USA
E-mail: {payman, lakshmi, kdoniger, wloh, pjwright}@lsil.com

Abstract

The importance of an interconnect pattern density model in ASIC design flow for a 90nm technology is presented. It is shown that performing the timing analysis at the worst-case corner model for interconnect variation, without the knowledge of interconnect pattern density, often results in overdesign. Our experiments on real ASIC products indicate that knowledge of interconnect pattern density in timing analysis of 90nm ASIC design flow prevents such overdesign. Quantitatively, it is shown that considering only the worst-case corner model in a global net results in a 10% delay overdesign. To meet the target delay for the net, it is sufficient to use a 45% smaller gate, which results in a 32% reduction in gate power dissipation, as well. It is, therefore, imperative to take into account the interconnect pattern density information in ASIC design flow of 90nm and future technologies.

1. Introduction

Process-induced parameter variations are important issues in the design of high-performance chips [1]. Until recently, it was sufficient to consider only die-to-die device and interconnect variations into the design methodology, which leads to a worst-case design. In the deep-submicron era, however, within-die variations become just as important [2]. The impact of within-die device variation has been well studied [3] but within-die interconnect variation has only recently been studied [4]. This is difficult because within-die variation is composed of random and systematic (layout dependent) components [4]. Unfortunately, the analysis of the systematic component cannot occur until the layout is substantially complete. As a result, performing timing analysis without the interconnect pattern density information and considering only the worst-case systematic variations often results in a non-optimal outcome [1,5].

It is, therefore, imperative to gain a thorough understanding of interconnect pattern density for present and projected gigascale integrated systems. Moreover, prediction of interconnect pattern density can also be an essential factor in reducing the design time, simplifying timing analysis, and improving the accuracy of timing verification.

A statistical analysis on the interconnect pattern density of various ASIC products is presented in Section 2. In Section 3, an intra-die interconnect thickness variation model due to pattern density effects is characterized. Utilizing the results from Sections 2 and 3, the impact of knowledge of interconnect pattern density in timing analysis of a 90nm ASIC design flow is explained in Section 4.

2. Statistical interconnect pattern density

Interconnect pattern density plays a significant role in systematic variation analysis. It has been previously shown in [1,4] that a substantial portion of within-die variability is from the interconnect pattern density, and therefore any information of wiring density from the layout is critical in timing analysis and verification.

Although the preliminary design rules limit the pattern density from 20% to 80% [6], a detailed statistical analysis is required to examine the realistic range of pattern density in real ASIC products. As an example, a plot of wiring pattern density of an M1 metal layer in a real ASIC chip with a 100μm window size is shown in Fig. 1.

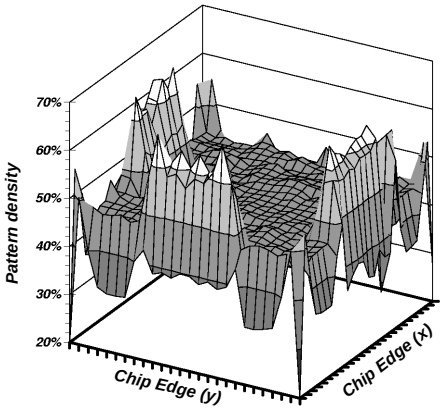

Figure 1. Pattern density of M1 metal layer in a real ASIC chip with 100μm window size

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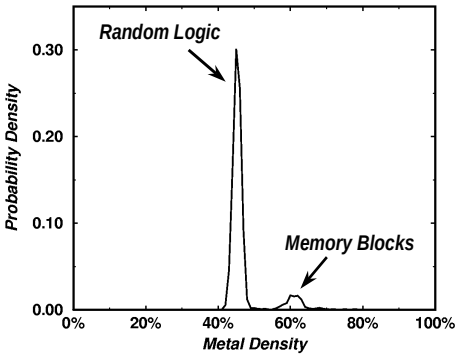

Figure 2. Probability density function of interconnect pattern density of M1 metal layer shown in Figure 1

By definition, the pattern density is the fractional area occupied by the metal interconnects in a region, which in this case is a tile of $100\times100\mu m^2$. The chip area is 13×13 mm^2 and it contains 2.7 million gates. The chip is fabricated in a 0.18μm technology with 5 metal layers. There are three blocks of memory in this chip, which can be easily recognized in the high-density regions of Fig. 1. The rest of the chip, which shows a relatively uniform pattern density, is random logic.

Although the M1 metal layer pattern density of the chip shown in Fig. 1 varies from 20% to 70%, the high-density regions are mostly clustered within the memory blocks and the rest of the chip has a relatively smooth metal density.

To show a clearer image of wiring pattern density, a plot of the probability density function (PDF) of the M1 pattern density of the design in Fig. 1 is illustrated in Fig. 2. Since the wiring density of standard cells is lower than that of memory cells, the first and second peaks in Fig. 2 are associated with the random logic and memory blocks, respectively. Moreover, since M1 is used only for internal standard cell routing, which is hand crafted and efficiently routed, its PDF is a very narrow Gaussian type function centered at about 45%.

The pattern density PDFs of M2 and M3, which are the main routing layers of random logic, also show the same behavior, as illustrated in Fig. 3. However, since the M2 and M3 layers are automatically routed using CAD tools, they show wider PDFs centered at much lower metal densities than that of M1.

On the other hand, the pattern density PDFs of M4 and M5 are rather different than those of M2 and M3. The high variation in M4 and M5 layers is mainly due to the power distribution networks and lower utilization of those layers in the routing process.

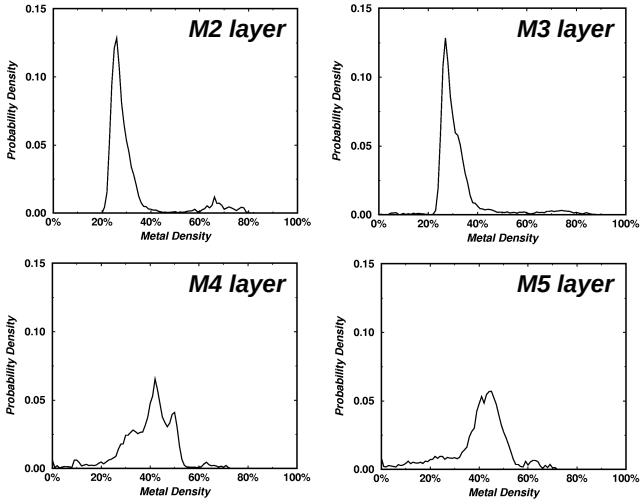

Figure 3. Probability density function of wiring pattern density of M2 to M5 metal layers

Since the pattern density PDF depends mostly on the layout of a design and the layout pattern itself is similar within different generations of technology (it only scales), it is a reasonable assumption that the pattern density PDF of a given metal layer is approximately constant throughout different generations of technology. Therefore, in this paper we use the pattern density PDF of M2 and M3 for the routing layers of random logic in a 90nm generation of technology.

3. Interconnect process CMP model

The damascene approach used to fabricate copper interconnects leads to a significant line resistance variation within the die [7]. This is a result of the inherent layout dependency of material removal rates in the chemical mechanical polishing (CMP) process used to create the lines. The phenomena of copper dishing and dielectric erosion combine to provide a metal sheet resistance that is a function of line width, local pattern density and the width of neighboring features [8]. The resistance of any single line can hence exhibit spatial variation depending on its layout environment. Such a systematic variation presents a serious challenge to the designer in accurately simulating circuit behavior and developing worst-case interconnect models. It hence becomes essential to characterize the metal resistance under various configurations as well as develop a model for its estimation of an arbitrary layout. In this paper we extend our previous work on resistance characterization and design rule formulation [6] to generate an empirical model for the resistance as a function of the line width and pattern density.

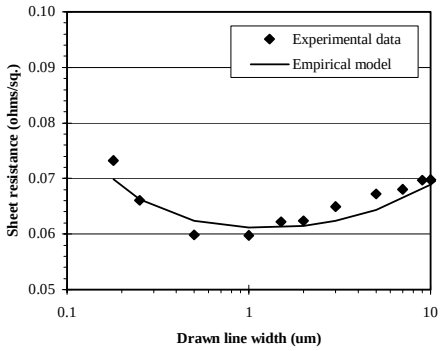

Figure 4. Effect of line width on metal sheet resistance for isolated lines

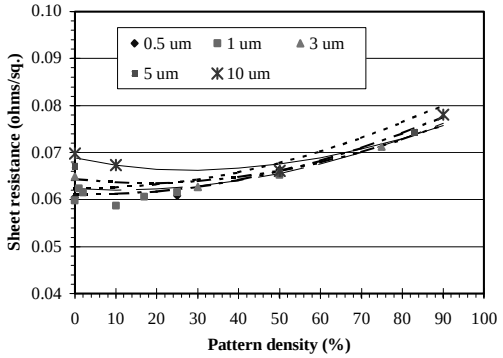

Figure 5. Impact of pattern density on metal resistance (symbols are experimental data and lines show the empirical model)

Figure 4 shows the effect of line width on the interconnect sheet resistance. The sheet resistance is extracted from the measured line resistance using the actual widths from X-SEM. The higher resistance on the wide lines is due to the reduction in copper thickness from dishing. On the narrow sub-micron lines (< 0.5 μm), the steep rise in sheet resistance is explained not by a difference in conductor thickness but rather from an increase in copper resistivity. Such a resistivity increase is believed to occur due to electron scattering from the trench sidewalls as the line dimensions approach the electron mean free path [9].

The impact of metal pattern density on sheet resistance is illustrated in Fig. 5. Pattern density is the fractional area occupied by the metal interconnects in any given region. For instance, a 3 μm line at a 30% density consists of a uniform array of 3 μm wide lines spaced 7 μm apart. The sheet resistance generally increases with pattern density due to greater dielectric erosion (with the exception of wide lines which exhibit a minimum between 20% and 50%). The total variation in sheet resistance for a given range of line widths and pattern densities can be deduced from this graph.

To maintain the sheet resistance within acceptable limits and ensure a predictable resistance under all layout scenarios, design rules and layout guidelines are needed. Rules specified include the maximum line width and a pattern density range [6]. For a random logic layout, the pattern density is calculated at any given die location by computing the metal coverage within a square window of a given dimension. The window size is the distance over which neighboring features affect the polish rate at the location of interest.

An empirical model has been generated to predict the copper line resistance as a function of the line width and pattern density in the range specified by the design rules (Figs. 4 and 5). The higher resistance in the narrow lines is accounted for by introducing a sidewall scatter correction factor in the line width.

4. Impact of interconnect pattern density on chip performance

Utilizing the metal process CMP model presented in Section 3, the interconnect geometry is computed as a function of metal pattern density for a 90nm technology. The interconnect geometry is then fed into our in-house fast capacitance extraction tool, VARCAP, to extract the wiring capacitance as a function of pattern density. The wiring resistance is also computed using the model presented in Section 3, considering the sidewall scatter correction factor in line width. The values of line capacitance and resistance for the main routing layers of our preliminary 90nm technology are illustrated in Fig. 6.

Figure 6 indicates that the line capacitance and resistance behave in opposite ways with metal pattern density. While the line capacitance decreases, the line resistance increases with increasing pattern density. Also, it is shown in Fig. 6 that the line resistance is more sensitive to metal pattern density variation than the line capacitance. For the whole range of pattern density variation, the line capacitance varies about 13%, whereas the line resistance varies more than 26%.

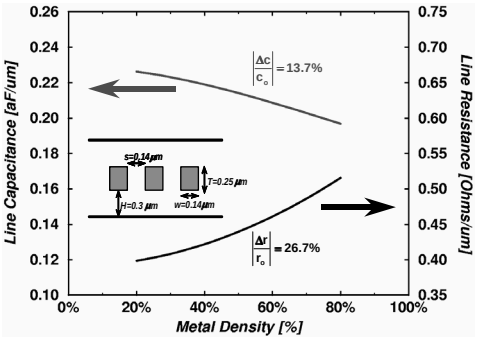

Figure 6. Variation of interconnect capacitance and resistance as a function of pattern density

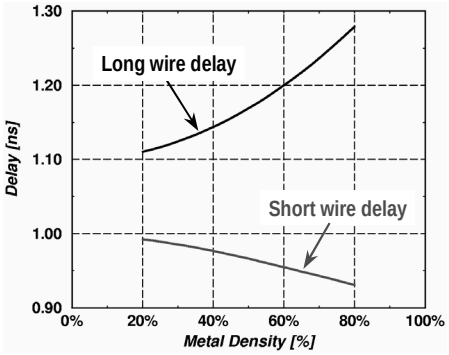

Figure 7. Variation of short and long interconnect delay as a function of pattern density

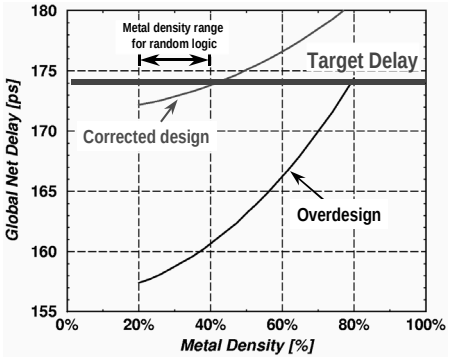

Figure 9. Variation of the synthetic global net reference circuit as a function of pattern density

To examine the impact of pattern density variation on delay, two reference circuits are simulated using HSPICE. One is a chain of 20 stages of small NAND gates, each driving a 200µm net (short wire) routed in M2/M3 layers, and the other is a chain of 8 stages of large NAND gates, each driving a 1000µm net (long wire) routed in M4/M5 layers. The simulation results are shown in Fig. 7.

Figure 7 indicates that the delay of long nets and short nets behave in opposite ways with metal pattern density. While the delay of long nets increases, the delay of short nets decreases with increasing pattern density. This is mainly because the delay of long nets depends largely on line resistance whereas the delay of the short nets depends largely on line capacitance.

Moreover, as shown in Fig. 7, the delay of the long wire circuit is more sensitive to metal pattern density variation than the delay of the short wire circuit. For the whole range of pattern density variation, the short wire delay varies about 6%, whereas the long wire delay varies more than 14%. It is also worthwhile to note that while 20% pattern density is the worst-case delay for the short wire circuit, 80% pattern density is the worst-case delay for the long wire circuit. As a result, the worst-case corner for delay calculations can be different depending on the wire length.

Global interconnects are commonly considered a key potential bottleneck to advancing the performance of future integrated systems [10].

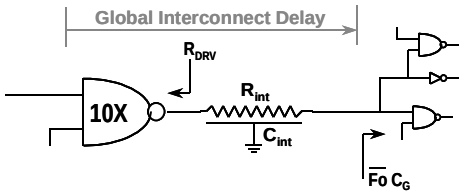

Figure 8. Circuit diagram of a synthetic global net

In order to investigate the impact of wiring pattern density on global interconnects, a synthetic reference circuit of a global net is generated for an ASIC product in a 90nm technology utilizing a stochastic wire length distribution model [11]. The synthetic reference circuit contains a 10× large NAND gate driving a 1500µm line in M4/M5 layers loaded with three other gates as presented in Fig. 8.

The results of HSPICE simulation on the synthetic global net reference circuit are illustrated in Fig. 9. In this simulation the target delay is set to be 174 ps. The overdesign curve in Fig. 9 is the global net delay assuming the complete range of metal density variation from 20% to 80% based on design rule limitations. However, based on the metal density range of 20% to 40% for random logic, as explained in Section 2, the design can be relaxed by resizing the driver gate to meet the target delay. The curve for the corrected design in Fig. 9 is the delay of the relaxed design.

Our simulation results indicate that considering only the worst-case corner model in a global net results in a 10% delay overdesign. To meet the target delay for the net, it is sufficient to use a 45% smaller gate, which results in a 32% reduction in total gate power dissipation, as well.

It is, therefore, imperative to take into account the interconnect pattern density information for ASIC design flow of 90nm and future technologies.

5. Conclusions

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6. Acknowledgements

The Authors would like to express their appreciation for the support and contribution of Richard Schinella, Paul Rissman, Peter Bendix, and Stan Yeh of LSI Logic Corp. In addition, the intellectual contribution to this paper by Prof. James D. Meindl of Georgia Institute of Technology is gratefully acknowledged.

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