Investigation of the capacitance deviation due to metal-fills and the effective interconnect geometry modeling

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Abstract

In this paper, the influence of floating dummy metal-fills on interconnect parasitic is analyzed with the variations of possible factors which can affect the capacitance. Recently proposed chip-level metal-fill modeling, replacing metal-fill layer with effective high-k dielectric, has been reviewed in detail. Using a systematized modeling flow, the property of the effective permittivity in the modeled geometry is examined. Validation with the realistic 3D structures clearly demonstrates the importance and correctness of the geometry modeling.

1. Introduction

Dummy metal-fills have been used to obtain the uniform etching profile and to maintain the global chip-scale planarity with the CMP (Chemical-mechanical polishing) process [1,2]. In any case, this floating metal-fills affect the interconnect capacitance more or less. This results in speed deviation from designer's expectation when it is not considered [3-5]. Recently, efficient yet accurate chip-scale modeling approach of floating metal-fills, via the effective interconnect geometry modeling, has been proposed and applied to the full chip RC extraction [6]. However, detailed features of the technology transformation into effective geometries, including the accuracy of the method, have not been extensively discussed. Furthermore, how various process parameters increase the capacitance due to metal-fills is not clarified yet. This paper investigates the characteristics of the metal-fills from various points of view. This can give insights to minimize the capacitance increase. The modeling accuracy of the effective interconnect geometry is verified with rigorous numerical analysis for the realistic 3D structures. In addition, the characteristics of the effective permittivity in the transformed geometry are examined with the automated modeling flow.

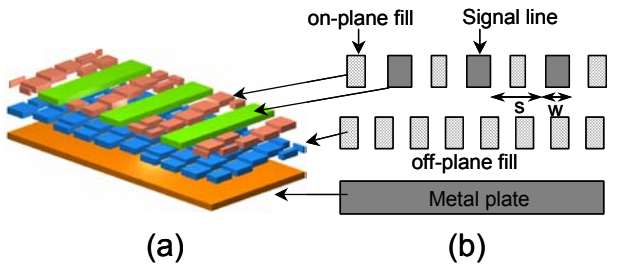

Figure 1. (a) 3D images of on- and off-plane metal-fills. (b) Vertical structure of (a).

2. Deviation of Interconnect capacitances due to floating metal-fills

In this section, increments of the capacitance by metal-fills are analyzed as a function of various parameters using the field solver PASCAL and the metal-fill characterization tool [4]. All possible factors - including signal line width/space, IMD thickness, density of metal-fills, filler size, metal layer thickness, and IMD permittivity – are considered. The structure in Figure 1 that has both on- and off-plane dummy metal-fills is used as a standard structure to evaluate the capacitance deviations.

Signal line width and space: The increments of capacitances have been examined with various line widths and spaces. The line widths and spaces are the major factors governing the effects of metal-fills. In Figure 2, the ca-

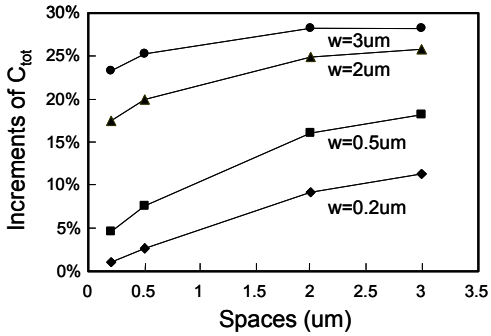

Figure 2. Increments of capacitances due to dummy metal-fills at various widths and spaces. IMD thickness is 0.5um.

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pacitance of the line, of which width and space are near the minimum design rule, is hardly affected by metal-fills because the large portion of the line capacitance is coupling capacitance and there is no chance for the metal-fills to be inserted between the lines. Meanwhile, as the width and space increase, the deviation of capacitance considerably increases and tends to saturate at a certain level as the overlap capacitance becomes dominant. The deviation of coupling capacitance is proportional to line spaces but the deviation of overlap capacitance is determined by its vertical structure and not a function of line width and space.

IMD thickness: The IMD thickness between the signal line and the metal-fill layer is also one of the major factors determining the influence of the dummy metal-fills. As the thickness of IMD decreases, mainly the overlap capacitance increases. The coupling capacitance also increases slightly because the influence of the off-plane floating metal-fills increases.

Metal-fill density: Figure 3 shows the average capacitance variations as a function of metal-fill density. The metal-fill density affects the global planarity as well as capacitance deviation. To determine the optimal metal-fill density, both capacitance increments and global planarity

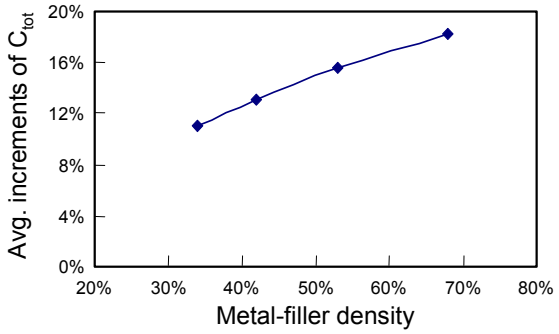

Figure 3. Average increments of C_{tot} versus metal-filler density. The capacitance is averaged for the combinations in Figure 1. (width/space - 0.2, 0.5, 2, 3um)

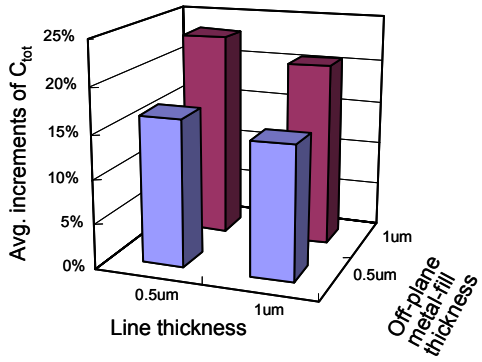

Figure 4. Average increments of capacitance as a function of signal line thickness and dummy layer thickness.

should be considered simultaneously. The dependencies of capacitance deviations on filler sizes are also investigated. In this study, the density of metal-fills is fixed to 53%. Smaller filler size at a constant dummy density can reduce some coupling capacitance but the improvement is too small to reduce the total capacitance. Accordingly, the increments of capacitance are independent of the filler size.

Metal layer thickness: Figure 4 shows the increments of average capacitances as a function of the signal line thickness and metal-fill thickness. The capacitance deviations are strongly influenced by the thickness of off-plane metal-fills rather than the thickness of signal lines. The thin signal lines and the thick metal-fills make the parasitic capacitances worse. For example, if the thin signal lines run below the top-most layer, which has thick metal-fills, the interconnect capacitance deviation would be significant.

Permittivity of IMD: The absolute value of interconnect capacitance is directly proportional to the permittivity surrounding the metal-fills and the signal lines. However, the percentage of the increment due to metal-fills does not change at all. This fact indicates that the low-*k* dielectric material can reduce the absolute value of parasitic capacitance, but this cannot improve the deviation rate of capacitance by metal-fills.

3. Effective interconnect geometry modeling

Recently, a methodology to perform the chip-level RC extraction including the floating metal-fill effect was proposed [6]. Floating metal-fills are replaced with the high-*k* dielectric material and the effective interconnect geometry is modeled as shown in Figure 5 (b). Such effective interconnect geometry is applied to the conventional full-chip RC extractor and the effects of the metal-fills are considered with a negligible increase of computational time. Figure 6 shows the capacitance deviation by dummy metal-fills at the full-chip level. The original and the effectively modeled geometries are applied to 0.18μm design and used as inputs of the full-chip RC extractor,

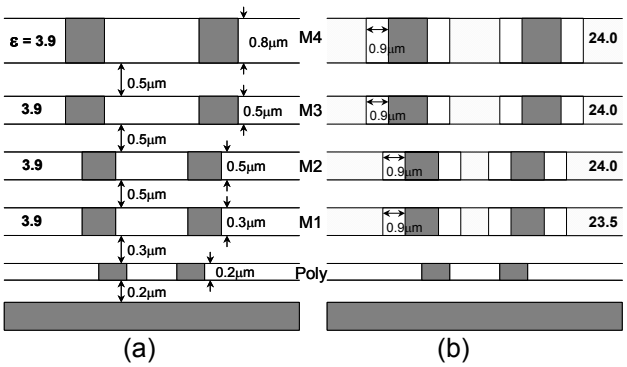

Figure 5. Effective interconnect geometry modeling for 4-metal process technology. (a) Original structure, (b) Modeled structure.

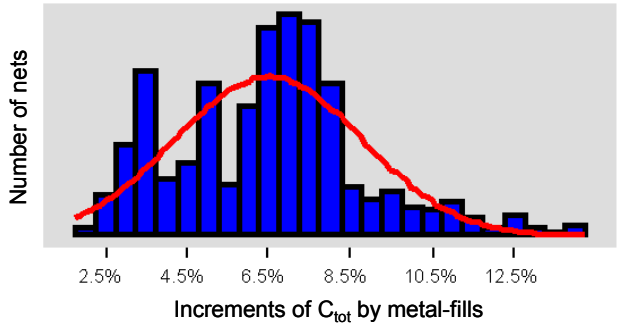

Figure 6. Deviations of the interconnect capacitances between with and without consideration of dummy metal-fills. Original and modeled structures are applied to STAR-RCXT.

STAR-RCXT. The average capacitance deviation by metal-fills is around 6.5% and for some nets the deviations reach to 15%. The subsequent timing delay simulation shows the same trend. The results show that the floating dummy metal-fills should be included in the chip-level RC extraction and timing analysis to avoid timing errors.

In the previous study, however, the validity and accuracy of the proposed method are explicitly proven for only simple 2D line-and-space type structures [6]. Even though it may be enough for assuring the extraction accuracy for global nets, the qualification for realistic 3D structures is important not only for the completeness of the methodology but also for special purpose. Such 3D qualification is important for the cell-level parasitic extraction, especially for the analog cell. In the analog cells, the floating metal-fills are usually eliminated because it is hard to estimate the deviation of capacitances by metal-fills and errors in parasitic extraction may result in design failure for the sensitive analog circuit. Thus, the uniformity of pattern density gets worse due to the absence of metal-fills and the global planarity after the CMP process is compromised. Therefore, inserting dummy metal-fills into the analog cells by virtue of the accurate extraction methodology would be definitely beneficial in global planarity point of view.

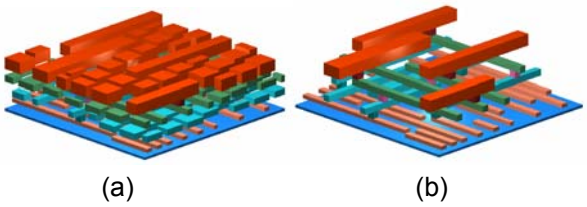

Figure 7. Test structures for 3D qualification of geometry modeling. (a) with the dummy metal. (b) without the dummy metal.

Table 1. (a) Combinations of the interconnect technology and structure for 3 examples. (b) Deviation of C_{tot} from ***Reference*** capacitance values.

(a)	Interconnect technology	Structure
Reference	original - Fig. 5(a)	with dummy – Fig. 7(a)
Neglected	original – Fig. 5(a)	w/o dummy – Fig. 7(b)
Modeled	modeled - Fig. 5(b)	w/o dummy – Fig. 7(b)

(b)	Net1	Net2	Net3	Net4
Neglected	-9.0%	-8.3%	-11.7%	-5.3%
Modeled	-0.6%	0.0%	0.3%	0.4%

Test structures in Figure 7 are used for the 3D qualification of the effective geometry modeling. The interconnect geometries in Figure 5 and the structures in Figure 7 containing 4 metal layers are combined to generate examples of 3 cases, as shown in Table 1(a). Capacitances are exactly calculated using the 3D field solver PASCAL for each case. Deviations from reference values are summarized in Table 1(b). Neglecting the effects of floating metal-fills results in underestimation of capacitances by about 10% for the present 3D structure. Whereas, the modeled interconnect technology combined with the structure without metal-fills gives very accurate

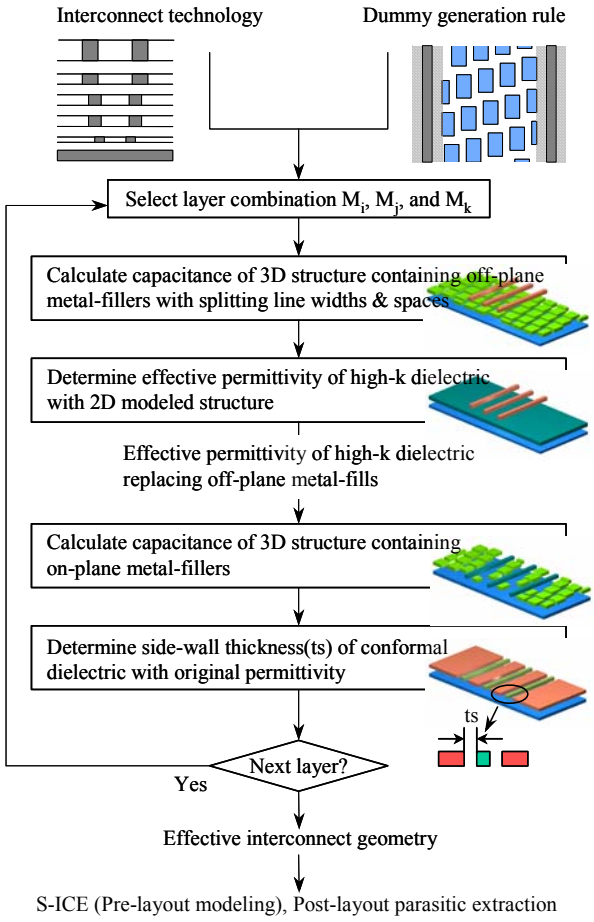

Figure 8. Automation flow of effective geometry modeling to consider the dummy metal-fills.

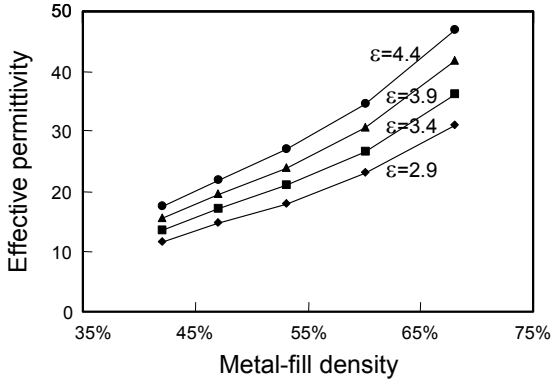

Figure 9. The effective permittivity as a function of the metal filler density. IMD thickness is 0.5um.

ture without metal-fills gives very accurate capacitance values with less than 1% errors. Furthermore, the extraction for modeled structure is about 3 times faster than that for structure with metal-fills, even though the field solver PASCAL employs an efficient algorithm for treating the floating electrodes [4].

To employ the present method to the design flow, nothing is required except the interconnect technology transformation to the effective one at the early process characterization step. However, such effective geometry modeling is tedious and time-consuming for recent interconnect technology containing more than 8 metal layers. The automation flow as shown in Figure 8 is implemented and integrated into our interconnect modeling environment S-ICE (Samsung Interconnect Characterization Environment). The overall modeling flow consists of two major parts. The first step is to obtain the effective permittivity of high-*k* dielectric, which replaces the off-plane metal-fills. After that, the sidewall thickness of the original dielectric that is placed as a conformal layer is determined. During whole flow, the capacitance deviation by the metal-fills is calculated with the 3D structure containing fillers explicitly and the effective permittivity and the sidewall thickness are determined with the 2D modeled structure.

Figure 9 shows the effective permittivity as a function of the metal-filler density and the IMD permittivity of the original structure. Extensive evaluation using the automated flow exhibits that the effective permittivity is mainly dependent on those two parameters and the dependences are roughly linear in meaningful parameter regimes. The thicker metal layer is mapped to the higher permittivity but the correlation is very low.

4. Conclusions

Electrical influences of floating dummy metal-fills on interconnect have been analyzed with the variation of capacitance related parameters. Presented simulation results and analyses can help reduce the effects of dummy metal-fills. The geometry modeling methodology that enables full chip RC extractor to consider metal-fills has been systematized and importance and accuracy of the modeling have been discussed.

5. References

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