A Novel Clocking Strategy for Dynamic Circuits

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Abstract

This paper proposes a new clocking strategy for dynamic circuit. It provides faster performance and smaller area than conventional clocking scheme. The proposed clocking scheme for dynamic circuits provides the solution of the problem caused by logic polarity and clock skew problem simultaneously. To demonstrate the proposed clocking strategy, a 32 bit Carry Look Ahead adder (CLA) is designed and simulated using 0.25um CMOS technology to demonstrate 32.7% faster speed than the conventional clocking scheme and 19.4% transistor counter reduction.

1. Introduction

Domino logic family has prevailed for high performance CMOS applications because of its high speed advantage. The main drawback of standard domino logic is non-inverting output characteristic due to its monotonic nature required for proper functionality. This characteristic hampers the freedom of IC designer whenever they need an inverting logic gate. And the other drawback of standard domino logic is precharge period. If single phase clock is used for standard domino logic, the precharge period is a waste of time. Therefore, two phase clocking was suggested to circumvents this problem. However, in order to hide the latency of precharge, the standard domino logic requires memory elements such as latch or flip-flop between the phase A (CLK) and phase B (CLKB) as shown in Fig.1. If a memory element is not inserted between the phase A and phase B, the final output of the logic gate in phase A does not propagate to the first input of the logic gate in phase B because gates of phase A, especially the last gate of phase A, is precharged right after phase A evaluation period. The drawback of this scheme is waste of evaluation time imposed by the clock skew[3] since the evaluation time is decreased because of clock uncertainty (skew). Therefore, several circuit families have been proposed and evaluated to overcome the lack of inverting logic and clock skew.

For inverting gate, Nora domino logic[5], Dual rail domino logic[1] and Clock-delayed domino logic[2] were suggested. Nora domino logic uses the N-tr and P-tr tree evaluation stage for inverting logic gate, and Dual rail domino logic uses an additional circuit to generate the inverting output signal. Clock-delayed domino logic uses delayed clocks to implement the inverting logic gate. For the clock skew problem, Skew tolerant domino logic[3] was suggested. This technique uses overlapping clock not to waste evaluation time due to clock skew.

The non-inverting problem and clock skew related problem have been addressed as two different issues so far. Consequently, the solutions turned out to be not effective causing area penalty. In this paper, we propose a new clocking strategy to solve the non-inverting logic polarity issue and clock skew problem simultaneously.

The basic idea of the proposed strategy combines the merits of clocking strategy of Clock-delayed logic and Skew tolerant logic. Therefore, we can obtain the inverting logic and reduce timing penalty due to clock skew. In order to compare the performance of the proposed circuit to the conventional dynamic circuits, 32 bit CLA[1] adder is designed and the critical path simulation is performed to compare the delays.

This paper is divided into 5 sections. Section 2 discusses standard domino logic, its clocking strategy, and drawbacks. Clock-delayed domino logic and Skew tolerant domino logic is discussed in Section 3. Section 4 describes a new proposed circuits and a design example of 32 bit CLA adder. The performance and size issues of each domino logics and static logic for CLA adder are presented in Section 5.

2. Domino logic overview

Domino logic is a very attractive design style for high performance IC design because it has a low logic threshold voltage (logic threshold voltage of domino logic is same as

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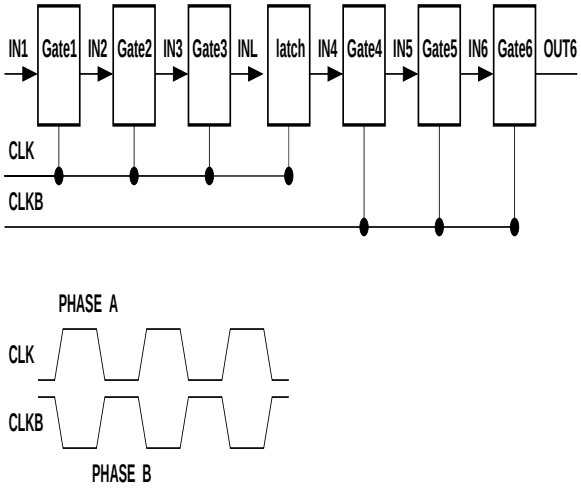

Figure 1. Clock waveform of conventional domino logic

the device threshold voltage.) and small transistor count compared with conventional static CMOS logic. Since it has inherent monotonicity, a conventional domino logic can only generate non-inverting output signal and it uses two phase clocking strategy to hide latency of precharge and to maximize the logic levels within a cycle as shown in Fig.1. In Fig.1, in order to hold the output data of Gate 3, the memory element should be inserted between Gate 3 and Gate 4. If the memory element is not used, the output data of Gate 3 cannot propagate to the input data of Gate 4, because the output of Gate 3 is precharged during the evaluation period of Gate 4.

The operating frequency of this logic is determined by the sum of the delays of gates through critical path, propagation delays of latches and clock skew delays, which are represented in Equation(1). In Equation(1), T_{gd} and T_{pd} are inevitable terms. However, T_{skew} depends on the external conditions such as clock loading, process variation, power supply variation, and clock distribution network, etc.

$$T_{cycletime} = T_{gd} + T_{pd} + T_{skew} \quad (1)$$

, where
$T_{cycletime}$: Total required cycle time of domino logics
T_{gd} : Gate delays of critical path
T_{pd} : Propagation delays of latches
T_{skew} : Clock skew of latches

3. Clock-delayed domino logic and Skew tolerant domino logic

Clock-delayed domino logic was suggested to provide a solution for non-inverting logic problem. The basic idea of Clock-delayed domino logic is shown in Fig.2. This idea is similar to the concept of Wave-domino logic[8], but the difference is in the presence of inverting logic. The evaluation phase of Gate 1 in Fig.2 is postponed until the inputs of Gate 1 arrive. After the output of Gate1 is evaluated, it is going to the input of Gate2, and if the other inputs of Gate2 are ready to evaluate the output signal, then the evaluation clock of Gate 2 will be followed. To do this, clocks for each gate should be provided and delayed separately.

In case of conventional domino logic in Fig.1, the evaluation clock precedes the inputs of a gate since only one evaluation clock is provided. Thus, the inputs of conventional domino logic should be "low-go-high" monotonic going from logic "0" to "logic "1" to avoid the erroneous output evaluation. If an input of a Nand gate goes from high to low during the evaluation period, output of a Nand gate will be invalid due to erroneous discharge. Former logic "High" input of a Nand gate already would have evaluated the dynamic node of a Nand gate to be zero by discharging the output node, and the followed low input becomes meaningless. Since the evaluation clock is delayed until all the inputs of a gate arrive for Clock-delayed domino logic, inputs do not have to be low-to-high monotonic transition and the keeper transistor is not needed any more since the gate does not suffer from charge sharing. As a result, the inverting gate will be freely used for designs with Clock-delayed logic. In addition, high fan-in gate is allowed in Clock-delayed domino logic, because all the inputs arrive during the precharge period as shown in Fig.2. Therefore, the circuit does not suffer from charge sharing. However, the penalty of this scheme is that the clock delay circuits are required in contrast to the standard domino logic and it should be well designed to achieve an optimum delay of the clock. They did not consider the clocking scheme for multiple pipelines in [2], and an additional circuit is required when the clocking method is used for multiple pipelines. Because each delayed clocks for Clock-delayed domino logic are not synchronized with the reference clock, the output may change during the precharge phase of the previous gate.

Skew tolerant domino logic was proposed to overcome the clock skew problem and propagation time of a latch. The basic idea of skew tolerant domino logic is shown in Fig.3. The difference between the conventional domino logic and the Skew tolerant domino logic is that Skew tolerant logic uses an overlapping clocks between phase A and phase B. This overlapped period of clock can soften the edge of clock to maximize the clock skew budget. Even though clock is skewed for some reasons, if overlapped clock period is sufficiently large, clock skew never affects the total delay of critical path because output is immediately evaluated as soon as inputs arrive.

The downside of this scheme is that it needs an additional overlapping clock generator, and the circuit does not

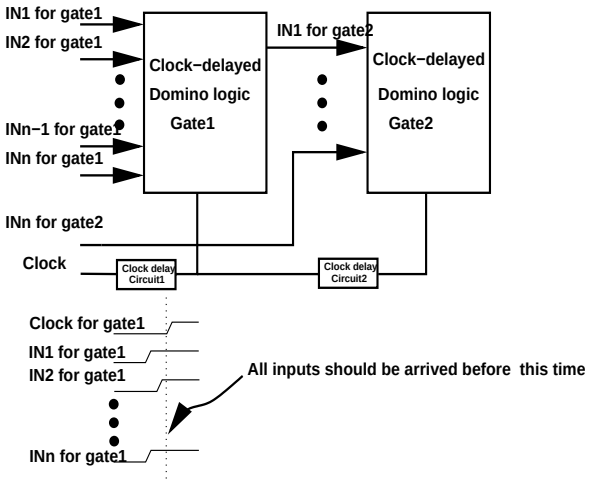

Figure 2. Clock-delayed domino logic

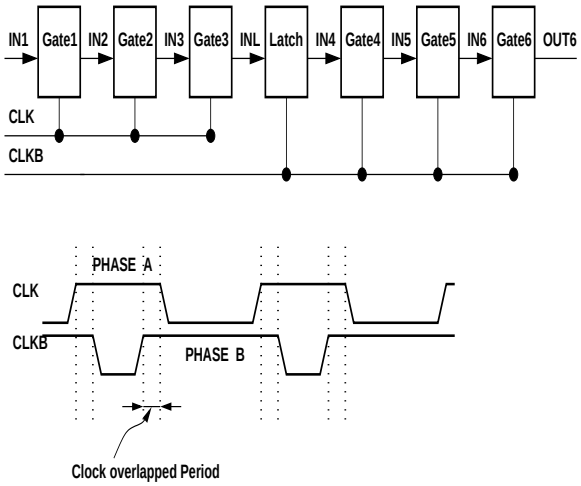

Figure 3. Skew tolerant domino logic

consider the inverting logic gate issue. If a circuit is designed using Skew tolerant domino logic and inverting logic gates are required, it imposes an additional area penalty to generate inverting signals.

4. New clocking strategy for dynamic gate

The proposed new clocking strategy is shown in Fig.4 with the timing diagram of the clocking schemes. If the evaluation clock of each gate is delayed until the last input of the gate arrives, low-to-high monotonic signal is not required. Therefore, an inverter is not required after dynamic logic, which gives us inverting logic gate. As the evaluation clock of the gate is later than all of gate input signals, all inputs of the gate are stable during the evaluation phase. Therefore, the keeper transistor to compensate the charge

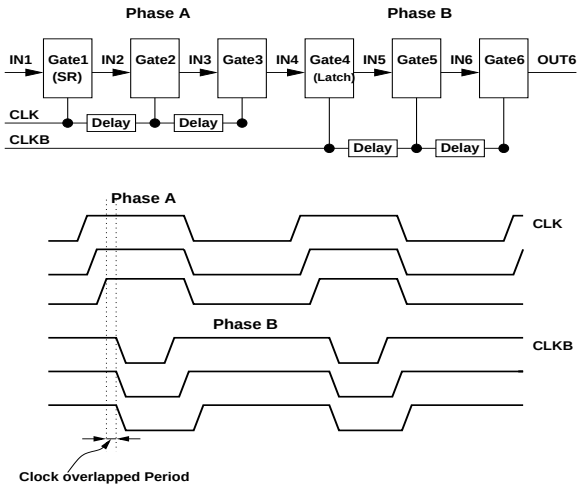

Figure 4. Proposed clocking method

loss and the inverter to drive the keeper transistor are not required at each output. Thus, data hazard caused by high-to-low transition of inputs dose not occur and inverting logic gates is available in this scheme. In addition, this allows designers to use high fan-in gate because there is no charge sharing problems. Thus, high speed and small area implementation of logical function is achievable.

To eliminate the clock skew problem, gated overlapping clock technique is used to soften clock edge between the phase A and phase B. Comparing this new dynamic circuit scheme with the Clock-delayed domino logic and the Skew tolerant domino logic, it has several advantages. First of all, this scheme reduces the timing uncertainty caused by delay variation of delay cells. When the delay cell is designed, its delay time is usually tuned to target delay under the normal condition. Even though fabrication process is controlled under restrict superintendence, the output of real delay circuit will different from the target delay time. If the output of delay circuit is fabricated under worst case conditions, the output of last clock delay stage will be the maximum delay deviation from the normal clock arrival time because the delay variations are accumulated. Since the proposed method uses non-inverting clock and inverting clock as an input of clock distribution circuit, the accumulated total delay variation is reduced to half. In the second place, this method requires similar area penalty compared to Clock-delayed domino logic. It only requires some additional gates to generate the overlapping clock[3]. Fig.5 shows an example of the clock generating circuit. The last point, of course not the least, is that the proposed circuit can simultaneously solve the non-inverting output problem and the clock skew problem.

The proposed clocking scheme need a non-inverting gate at the interface part between phase A and phase B stages to

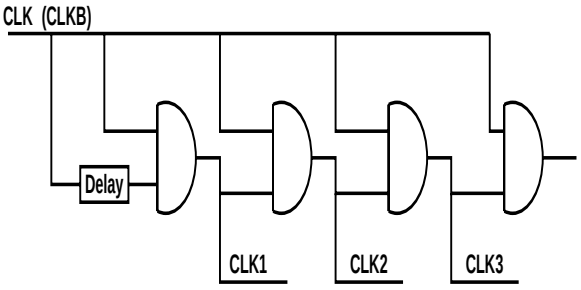

Figure 5. Clock generator circuit

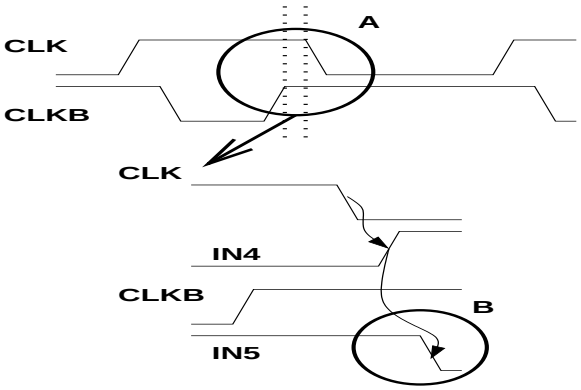

Figure 6. Consideration of interface timing between phase A and phase B

avoid an erroneous discharge. In more specifically, the last gate in phase A and the first gate in phase B simultaneously stay at evaluation period where discharge problem can occur if the non-inverting gate is not used in the last gate in Phase 1. In Fig.6, before CLK goes to precharge period, it is assumed that IN4 was evaluated as low. When CLK goes to precharge period, IN4 goes to high. At this time, Since CLKB is high, the first gate of phase B is in evaluation phase, and its output value is assumed as a high. As a result, IN4 in precharge period can generate erroneous output evaluation of phase B. To prevent this problem, the last gate of phase A should be non-inverting. If the last gate of phase A is inverting logic gate, a buffer shown in Fig.7 can be used to solve this problem. As a memory element, the proposed clocking method uses a latch which shown in Fig. 7. This latch style has several advantages. It can be combined with any type of functional gate logic, and it can share the clock with dynamic logic to minimize the area.

To verify the functionality and performance of proposed clocking strategy, 32 bit CLA adder was designed and simulated using 0.25um CMOS process. In order to verify the proposed clocking method, the domino logic gates of 32 bit CLA adder were divided into two pipeline stages. One

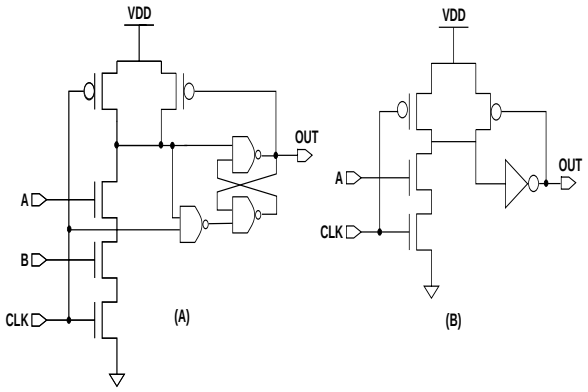

Figure 7. Latch and non-inverting gate in the proposed clocking scheme

pipeline stage is driven by phase A clock, the other pipeline stage is operated by phase B clock. The latches were inserted between logic gates of phase A and B. Transistor width of 2.5um for N-tr and 6.5um for P-tr were used as a basic width. The sizes of transistors were selected for performance comparison only. Using the same transistor ratios as the basic transistors, other primitive cells were designed.

5. The performance and size comparison of each adder

Table 1 shows the HSPICE performance simulation summary for each adder. As shown in Table 1, the adder using the proposed clocking scheme demonstrates the best performance. All of adders are designed to keep the same structure for fair comparison. First, 32 bit CLA adder with static logic was designed, and the adder is used as a reference for performance comparison. Based on this adder architecture, the other dynamic adders were designed using the same microarchitecture, which means that the the gate level schematics of static logic, standard domino logic and skew domino logic are exactly same except clocking part. For our proposed method, several inverting logic gates are used to obtain the minimum area. However, large fan-in is not considered for the implementation using the proposed method. If the large fan-in gate is considered, the adder size of proposed method will be smaller than this result. The number of gates and transistors of 32 bit CLA adders are shown in Table 2. The transistor count of the clock generator is not included. The less number of transistor is required to implement 32 bit CLA using the proposed method, because it implements inverting logic gate without area penalty.

The critical path simulation results of Static logic, Standard domino logic and Skew tolerant domino logic are shown in Fig.8, Fig.9, and Fig.10. And The critical path

Table 1. Delay of adders

Logic family	*Delay*	*Relative performance*
static logic	1.77ns	1
standard domino logic	1.46ns	1.21
skew tolerant domino logic	1.26ns	1.40
proposed method	1.1ns	1.55

Table 2. The number of gates and trs for each adder

Logic family	*No. of gates*	*No. of trs*
static logic	291	1884
standard domino logic	291	2282
skew tolerant domino logic	291	2282
proposed method	343	1911

simulation result of proposed method is shown in Fig.11.

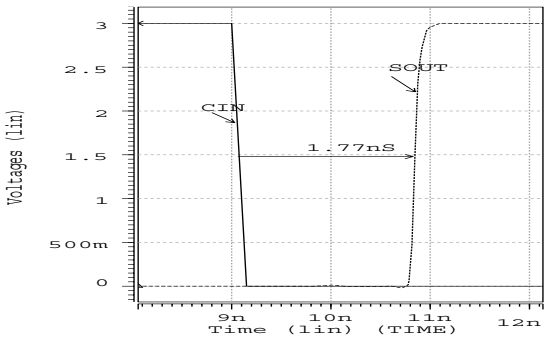

Figure 8. Critical simulation result of Static adder

6. Conclusions

We proposed a new clocking scheme for dynamic circuit and designed 32 bit CLA adder as a test vehicle. The proposed scheme presents a solution to solve the clock skew problem and the logic polarity problem of dynamic circuits. Logic polarity of the dynamic gate and clock skew issues have been looked at as two different issues, and they have addressed those issues as two different ones. However, the clocking scheme we proposed in this paper suggest a clocking scheme that can solve the non-inverting problem and the clock skew problem simultaneously without significant

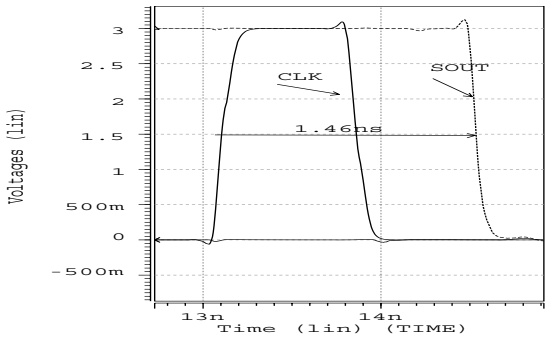

Figure 9. Critical simulation result of Standard domino logic adder

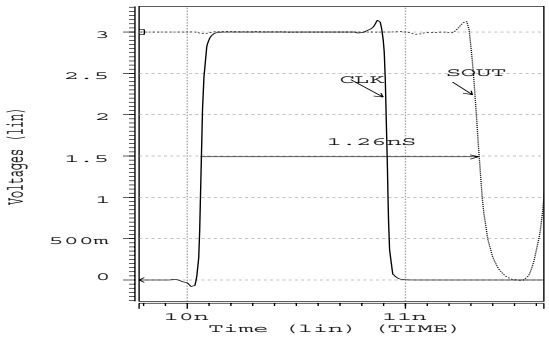

Figure 10. Critical simulation result of Standard domino logic adder

penalties.

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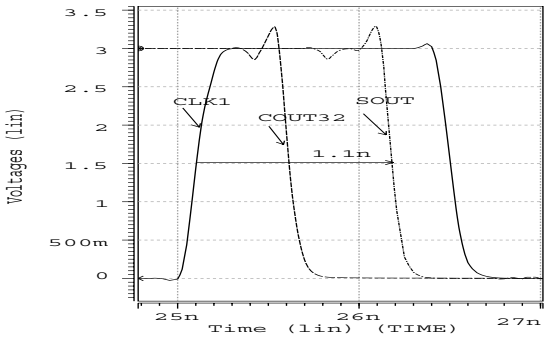

Figure 11. Critical simulation result of Dynamic adder when the proposed clocking method is used.

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