Modeling and Analysis of Power Distribution Networks for Gigabit Applications

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Abstract

As the operating frequency of digital systems increases and voltage swing decreases, it becomes increasingly important to accurately characterize and analyze power distribution networks (PDN). This paper presents the modeling, simulation, and measurement of a PDN in a high-speed FR4 printed circuit board (PCB) designed for chip-to-chip communication at a data rate of 3.2 Gbps and above. The test board consists of two transceiver chips placed on wirebond plastic ball grid array (PBGA) packages. The applied analysis method is a hybrid technique that combines the interactions of the power planes, interconnects, and the nonlinear drivers. The power planes and interconnects are modeled using the transmission matrix method (TMM) and rational interpolation, respectively. Then macro modeling is applied to generate reduced-order models to efficiently analyze the whole system including the nonlinear drivers using conventional circuit simulation tools such as SPICE. The transfer characteristics of the power planes are calculated and the effects of the decoupling capacitors and power supply noise are studied. The simulation results are also correlated with measurement data to verify the validity of the method.

Keywords *– Macro-modeling, power distribution network, reduced-order modeling, and transmission matrix method.*

1. Introduction

In order to meet the high-bandwidth demands and low-power requirements, current digital applications are quickly moving to gigabit data-rate and a sub-volt voltage supply range. For example Rambus' Yellowstone™ signaling technology utilizes a bi-directional 200-mV swing Differential Rambus Signaling Level (DRSL) with a data transfer rate starting at 3.2 Gbps/pair and scalable to 6.4 Gbps/pair [1]-[2]. These higher operating frequencies and low voltage swing place increasing demand on the quality of the power distribution. Therefore, accurate analysis of the PDN is essential to optimize the performance of the overall system.

As the signal switching becomes faster and the supply voltage becomes smaller, the power and ground bounce and switching noise can degrade the quality of the signal. When a large number of logic gates switches, the voltage supply to the circuitry may fluctuate due to the inductive and resistive effects of the power distribution systems. Through the coupling between the power and signal distribution systems, simultaneous switching noise can cause false logic, degrade the signal edge rate, delay skew, and increase signal overshoot or undershoot. For example, I/O circuits can fail due to collapse of or noise on the power and ground I/O rails. Therefore, the understanding of these noise sources in gigahertz applications has been of critical importance to achieve maximum bandwidth and low power.

In order to suppress the power and ground plane fluctuations, the PDN need to be designed to provide a quality power supply at least to more sensitive analog circuits such as a PLL. The PDN must provide a low impedance voltage supply and good return path to the devices. Low-impedance and constant voltage supply can be obtained from DC to few harmonics by using decoupling capacitors. The decoupling capacitors provide an AC ground to the noise. At medium and high frequencies, the impedance peaks can be suppressed using large and small value decoupling capacitors. The low-frequency low impedance is maintained using a regulated voltage supply. If the devices do not see a low-impedance power supply at all frequencies, voltage spikes or droops occur on the power supply terminals of the circuit when edge rates coincide with the high impedance of the power supply. Additionally, if the PDN does not provide low-coupling at all frequencies among devices, the spikes or droops caused by one device affect the neighboring devices. These limit the maximum number of active devices that can be used for reliable operation.

In this paper, the power distribution system of a Yellowstone test board is characterized. The test board, shown in Fig. 1, is a chip-to-chip communication system designed to operate at 3.2 Gbps. The system is modeled using the method described in [3]. The next section briefly describes the modeling and simulation methodologies. Section III and IV describe the test board design and the simulation and measurement results. Finally, Section V presents the conclusions.

2. Modeling and Simulation Methodology

There are two main approaches for the modeling and simulation of PDNs. The first approach is based on the representation of the PDN using equivalent lumped circuit models. The behavior of complicated PDNs has been successfully modeled using this approach. In [4], the power planes are represented by an equivalent single

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0-7695-1881-8/03 $17.00

lumped circuit model using the effective inductance. Although the effective inductance approach is suitable to handle multiple power planes because it is computationally inexpensive, the approach does not reflect the electromagnetic wave propagation effects on the planes. Only a distributed circuit model can accurately model these effects at high frequencies. The second approach is to use traditional electromagnetic field solvers to analyze the whole system. This approach gives the electromagnetic solution at any location on the plane; however, the method is not suitable for simulation of practical designs because of the enormous CPU time it requires. Therefore, the fullwave tools are computationally expensive, and thus, limited to relatively simple structures.

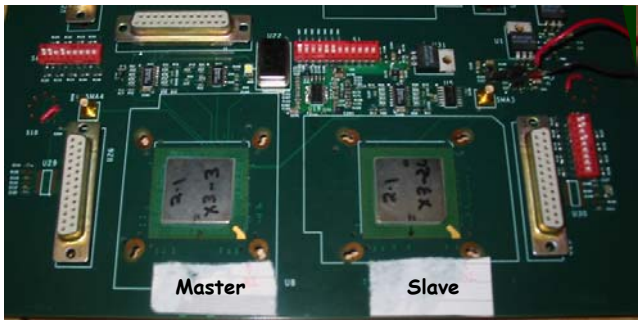

Figure 1: Top view photo of the Yellowstone test board.

Recently, hybrid methods of modeling and simulating PDN have been proposed. The limitations of the equivalent circuit and fullwave EM approaches are reconciled through a divide-and-conquer strategy. The power planes are modeled using electromagnetic solvers and the circuit elements are handled using conventional circuit simulators. The power plane solution is incorporated into the time domain solution through macro-modeling techniques. In the past, EM field simulators such as the finite-element method (FEM), the finite-difference time-domain (FDTD) method, and the transmission matrix (TMM) method have been applied to the power planes and integrated with circuit simulators to analyze power supply noise in packages [5]-[7].

The power planes support wave propagation. More specifically, they behave as cavity resonators supporting radial waves that propagate between the plane pairs. The reflection of these waves at the plane edges causes resonances in the steady state. This behavior can be captured by computing the frequency-domain impedance of the power planes that include wave propagation effects. Therefore, the power planes can be separately modeled and later combined with the rest of the system [8].

Based on this observation, the combined method proposed in [3], preserves the accuracy of field simulators to power plane modeling and at the same time improves the efficiency of the overall analysis of the system consisting of PDN, interconnects, and drivers. This methodology is shown in Fig. 2. First, the frequency-domain impedances of the power plane pairs are calculated using the TMM method. Then the macro-model of the plane is generated at the desired ports. The reduced order models of the interconnects are also generated using rational approximations. Then, the models of the plane and interconnects with the driver models are solved in conventional circuit simulators such as SPICE. Therefore, the modeling method supports both wave propagation in the plane and nonlinear simulation of the driver.

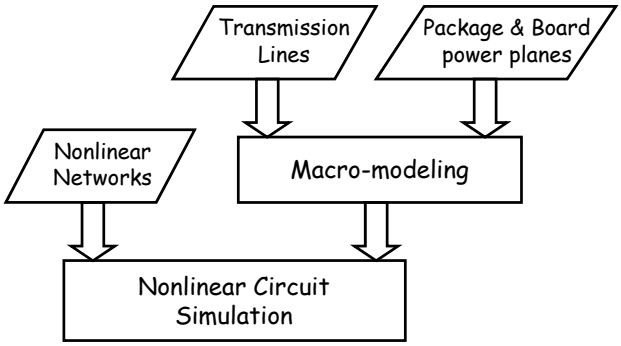

Figure 2: Power distribution modeling and simulation methodology.

To calculate the impedance of the plain pairs using the TMM method, the power and ground planes are divided into $N \times M$ *cells* and each unit cell is represented by RLCG elements. The RLCG elements are generated from the unit cell parameter that is calculated from quasi-static approximations as:

$$C = \varepsilon_o \varepsilon_r \frac{w^2}{d}, \quad L = \mu_o d, \quad R_{dc} = \frac{2}{\sigma_c t}, \quad R_{ac} = \sqrt{\frac{\pi f \mu_o}{\sigma_c}}, \quad G_d = \omega\, C\, tan(\delta) \tag{1}$$

where d is the dielectric separation between the power and ground planes, w is the unit cell lateral dimension, t is the thickness of the conductor, $tan(\delta)$ is the loss tangent of the dielectric, σ_c is the metal conductivity, μ_o is the permeability of free space, ε_o are the permittivity of free space, and ε_r is the permittivity of the dielectric. The parameter R_{dc} and R_{ac} are the DC and AC resistance of the power and ground planes, G_d is the dielectric loss, and L and C are the inductance and capacitance of the planes, respectively.

The details of the MIMO transmission matrix method is discussed in [3]. Since the cell models are circuit elements, the impedance of the power plane can be calculated using the TMM technique. The inverse FFT can be applied to obtain the time-domain response when the source is linear. When nonlinear sources are present, the macro-modeling method can be used to represent the plane in conventional circuit simulators.

The macro-model or reduced-order model of the power plane pairs and interconnects are generated by

representing the frequency-domain characteristic parameters by a passive rational function of the form:

$$Z(s) = \frac{a_0 + a_1 s + \cdots + a_p s^p}{b_0 + b_1 s + \cdots + b_q s^q}, \qquad (2)$$

where a_i's and b_i's are real coefficients solved from least square solution. Equation (2) can then be synthesized with circuit elements or incorporated directly into circuit simulators that support Laplace expressions. It is important to note that the passivity needs to be preserved while generating the macro-model [9].

3. Test Board Design

The Yellowstone test board is shown in Fig. 1. The test board consists of transmitter and receiver chips wirebonded onto PBGA packages. The PBGA packages are directly attached to the board using solder balls or using sockets. The detail of the PBGA package is described in [10]. The board is a 6-layer PCB that is *12.8 in.* by *9.5 in.* in size. The cross section of the board is shown in Fig. 3. There are two power planes and two ground planes. Layer 3 is a *5V* power plane that supplies voltage to the peripherals on the board. It also has two power islands of *1.2 V*, the master and slave sections, to supply voltage to the transmitter and receiver chips on the board respectively as shown in Fig. 4(c). Layer 4 is also a *1.2 V* split power plane that serves the master and slave sections and includes a small island at the center with *3.3 V* to supply voltage to the clock generator chip, as shown in Fig. 4(d). The split is used to monitor the power drawn by each subsystem. The two split planes are connected using a jumper. The ground planes, layers 2 and 5, are continuous planes. The power plane conductor thickness is *1.4 mil.* The top and bottom are signal layers for low and high-speed interconnects, as shown in Fig. 4(a) and Fig. 4(b), respectively. The low speed signals are single ended and their impedance is designed for *50* Ω using trace width of *7 mil* and *18 mil* spacing. The high-speed signal nets are differential and are designed with *6 mil* width and *11.5 mil* spacing. The pair of traces is designed to obtain a *100 Ω* differential impedance. The signal trace thickness on layers 1 and 6 is *0.7 mil.*

The dielectric material of the board is FR4 with a permittivity, ε_r = *4.5*, the conductor is copper with conductivity, σ_c = *5.8e-7 S/m* , and with thickness of *30 um* and dielectric loss tangent, $tan(\delta)$= *0.02* at *1 GHz*. The power planes are excited and measured at the locations shown in Fig. 4(d).

4. Analysis and Results

The modeling and simulation methodology briefly described in Section II have been applied to the test board. The primary objective is to analyze the power distribution system and understand its effect on the performance of the overall system.

Figure 3: The cross section of the board.

First, the frequency-domain impedances are calculated for the power plane pairs. The input impedance and transfer impedance of the power planes across different locations provide a measure of the quality of the PDN. The impedance between the chips on the board is required to be low across the operating frequency spectrum. Therefore, the frequency domain multi-port impedance matrix has been calculated using the TMM method.

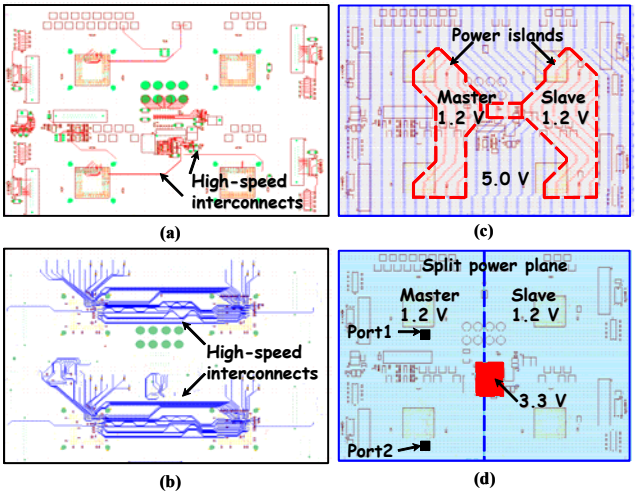

Figure 4: The signal and power plane layers of the test board: (a) layer 1, signal layer for low-speed signals (b) layer 6, signal layer of high-speed signals, (c) layer 3, power layer, and (d) layer 4, power layer.

In addition to the modeling of the power planes, various measurements are also performed on the test board using a vector network analyzer (VNA) [11]. In order to correlate the simulation data with the measurement data, the parasitics associated with the probes and pads are added as series resistors and inductors to the power plane model, as shown in Fig. 5.

Figure 5: Modified equivalent network of the power planes.

Therefore, the impedances of the power plane pairs are modified as

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} + R_1 + j\omega L_1 & Z_{12} \\ Z_{21} & Z_{22} + R_2 + j\omega L_2 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}. \quad (3)$$

The probe and pad parasitics only affect the self impedance, but not the transfer impedance, as described in (3). Therefore, self impedances are very sensitive and require accurate calibration and consequently transfer impedance measurements are more reliable for hardware correlation.

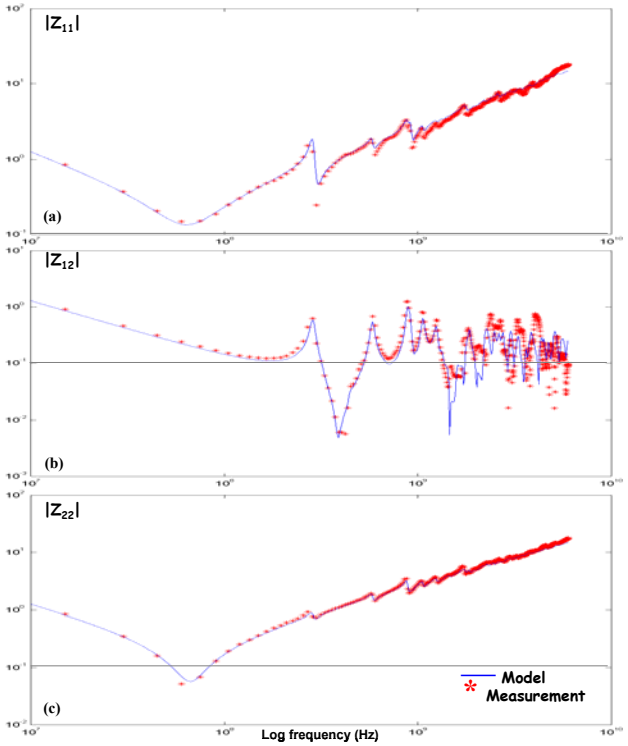

Figure 6: Comparison of modeled and measured impedances of layer 4-layer 5 from 10 MHz to 6GHz: (a) Input impedance at port 1; (b) transfer impedance between ports 1 and 2; (c) input impedance at port 2.

After including the probe and pad parasitics, the simulated and measured input impedances and transfer impedances for ports 1 and port 2 are compared over *10 MHz – 6 GHz*, as shown in Fig. 6. A very good agreement is obtained between the simulated and measured data.

As discussed in Section I, decoupling capacitors can be used to control the peaks of impedance in mid- and high-frequency ranges. A *100-nF* decoupling capacitor with equivalent series inductance (ESL) of *0.55 nH*, and equivalent series resistor (ESR) of *0.02* Ω are placed at different locations on the board.

The simulated and measured impedances with decoupling capacitors are shown in Figs. 7 (a), (b) and (c). The null resonant frequencies and magnitudes of all self and transfer impedances are affected in all the cases. The model of the decoupling capacitor and power plane is shown in Fig. 8. The self-resonant frequency (SRF) is $SRF = 1/2\pi\sqrt{L_{cap}C_{cap}} = 16.57\,MHz$ .The impedance at the SRF gives the ESR of the capacitor. If the coupling between different layers is small, the parallel resonant frequency (PRF) can be approximated as $PRF = 1/2\pi\sqrt{L_{cap}C_{plane}} = 47MHz$, for $C_{cap} >> C_{plane}$. In Fig. 7 a), the addition of a single decoupling capacitor creates the first null at *16.57 MHz* while the first peak occurs at *47 MHz*. With the addition of two capacitors, the first null in Fig. 7 (b) remains the same while the first peak moves to a higher frequency. This is because of the doubling in the capacitance and reduction in the inductance to half its original value. Both results show good correlation with measurements. In Fig. 7 (c), 20 capacitors have been added to the plane along with other components. Once again the results show good agreement with measurements, validating the modeling methodology.

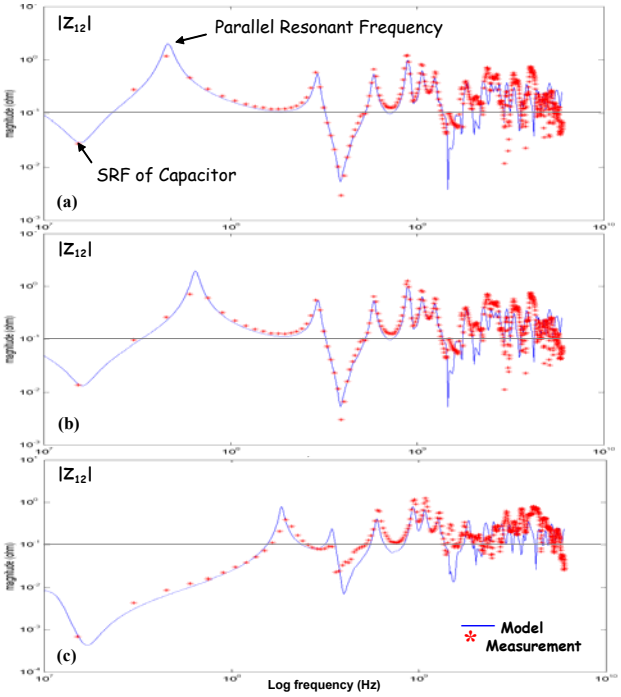

Figure 7: Transfer impedances for (a) one, (b) two, and (c) twenty decoupling capacitors.

In Fig. 7, the transfer impedances show an overall improvement. As more decoupling capacitors are added, the low-frequency impedances and the magnitude of the peak at resonant frequencies are reduced, as shown in Fig. 7.

The effect of the decoupling capacitors at various locations are also studied. To study the effect of the chip on the impedance of the PDN, the transfer impedance of the Yellowstone test board with one decoupling capacitor is measured. As shown in Fig. 9, the transfer impedance,

with and without the chips, does not show a significant change. This is because the chip capacitance has an impedance larger than the impedance of the power planes with decoupling capacitors.

Finally, the transfer impedance of the split plane on layer 3 is simulated at various locations within the split plane and across the master and slave split planes. The input impedances and transfer impedances across various locations within the master and slave plane remain identical, as shown in Figs. 10 (a), (b), and (c). The reason for the higher impedance seen from the voltage regulator module *(Z_{11})* is that a narrow strip is used to supply the charge to the switching circuits on layer 1. The transfer impedance between the master and slave split plane show little coupling at low frequencies. This is because separate islands are used to supply power to the master and slave side. However, at higher frequencies, substantial coupling is seen even though the islands are isolated. This is because the narrow strip from the voltage regulator module is used to maintain the same potential on the two islands using vias. This causes capacitive coupling between the two islands. When the two islands resonate, they couple energy through the coupling capacitance. This behavior can be explained by means of a simple equivalent circuit shown in Fig. 11. In the figure, the *55 nH* of inductance is the spreading inductance from the coupling capacitor to the master and slave chips. Each chip has 12 capacitors in parallel, as shown in the figure.

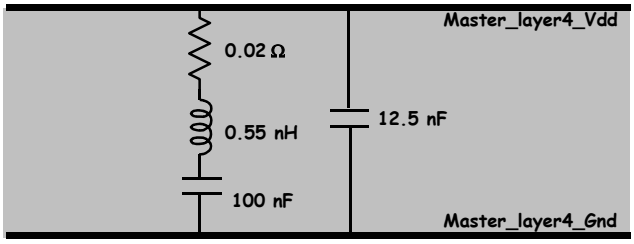

Figure 8: Model of plane pair with decoupling capacitor.

In order to study the power supply noise, a time-domain simulation is also performed using the macro-model of the power planes. The combined circuit model of the power plane, interconnect, and the driver is shown in Fig. 12. A bit pattern with rise and fall time of *50 ps* and voltage swing of *300 mV* is used. When three differential drivers are switched, a power supply noise of *10 mV* is observed, as shown in Fig. 13. This represented a bit pattern 0000111100001111…. It is important to note that a perfect differential circuit cannot produce power supply noise due to the balance in the current drawn by the two transmission lines. However, any imbalance in the differential circuit can generate power supply noise. In Fig. 12, *10 ps* skew is intentionally introduced in the circuit to generate the power supply noise.

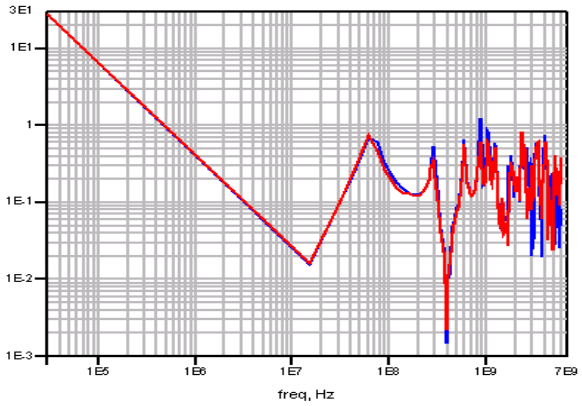

Figure 9: Transfer impedances of the Yellowstone board with two decoupling capacitors, with and without the chips.

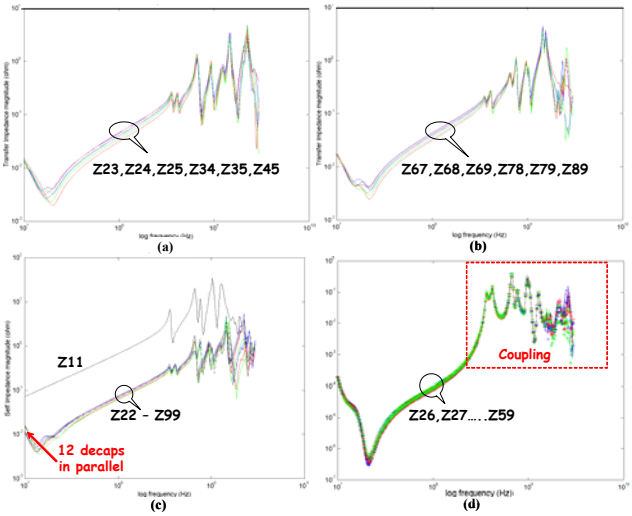

Figure 10: Impedances of the split plane; (a) transfer impedance within the master, (b) transfer impedance within the slave, (c) input impedance, and (d) transfer impedance between master and slave power planes.

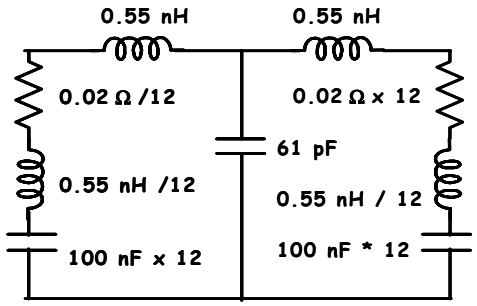

Figure 11: Equivalent circuit for coupling between the master and slave islands.

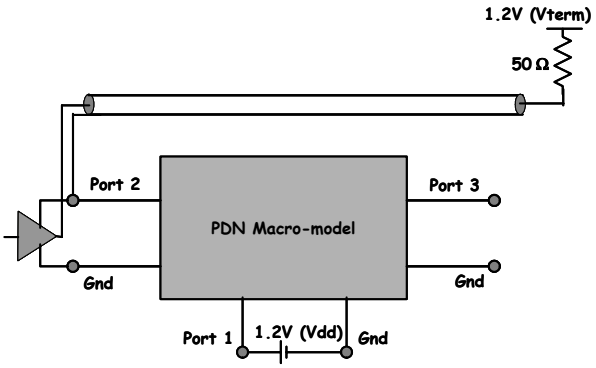

Figure 12: Combined model Yellowstone channel for power supply noise analysis.

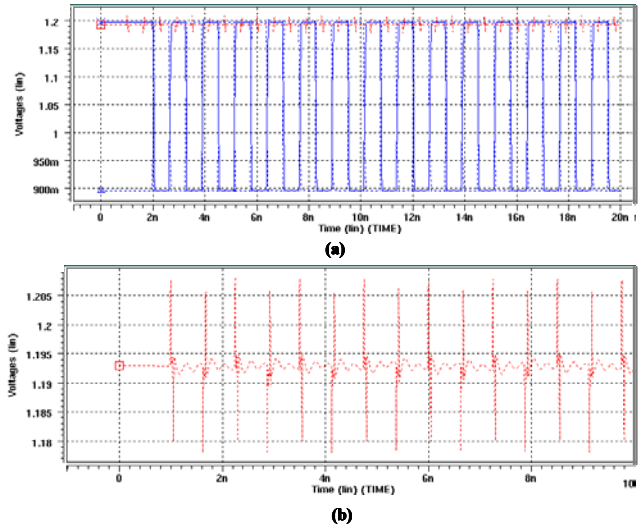

Figure 13: Power supply noise: (a) data waveform, (b) power supply noise.

5. Conclusions

In this paper, we have presented the modeling, simulation, and measurement of the power distribution system in a test board that operates at 3.2 Gbps and above. The methodology applied to study the system is a hybrid method that combines the TMM and macro-modeling in a conventional circuit simulation environment. The method accurately and efficiently analyzes the PDN of the test board. The effect of decoupling capacitors and the behavior of the split power planes are also analyzed. Measurements are also performed on the complete test board with and without the chips. The results from the modeling and simulation match with measurement data very well.

Acknowledgement

The authors would like to thank the following engineers from Rambus; Rob Dhat for the designing the package and the test board, Newton Cheng, and Hao Shi for performing the measurements.

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