Advanced Module Packaging Method

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Abstract

An intermediate solution between conventional printed circuit board technology and wafer level packaging, WLP, is to fabricate interconnection circuits and flip chip assembly structures on large glass substrates using LCD manufacturing equipment. Trace widths of 5 microns and a trace pitch of 10 microns are achievable on flexible substrates as large as 1800 x 1500 mm. Back planes for displays and keyboards can also utilize thin film transistors, TFTs, as developed for LCDs and enhanced for flexible assemblies (200ºC processing). A flexible circuit is built on a glass carrier with an intermediate release layer. The carrier is discarded after all processing is complete, including interconnection circuits, IC chip assembly, test and rework. The assembly method uses gold stud bumps on IC chips, and corresponding wells filled with solder on the motherboard. 100-micron pad pitch is achievable for IC chips, module cables, and test connections. Avoidance of epoxy under layers contributes to a robust capability for reworking defective IC chips. The methods are applicable to a wide range of products, from cell phones to blade servers.

1. Introduction

The author was working on advanced structures for non-impact printing and discovered that sub 5–micron features are achievable on polyimide substrates if there is an underlying glass carrier. It is postulated that the mechanical support and dimensional stability transfer from the rigid glass substrate to the flexible circuit assembly on top, thereby enabling fine features and dense flip chip assemblies. However, using release layers that are currently under development, the circuit assembly can ultimately be separated from the carrier, to take advantage of compliant packaging technology. The author has researched and patented the process [1] and the application to computing devices with roll up components [2]. Copies of these patent applications are available on request.

2. Building on glass

Figure 1 shows a layout of several different types of circuits on a glass panel measuring 1250 x 1100mm, representing 5th generation LCD manufacturing technology.

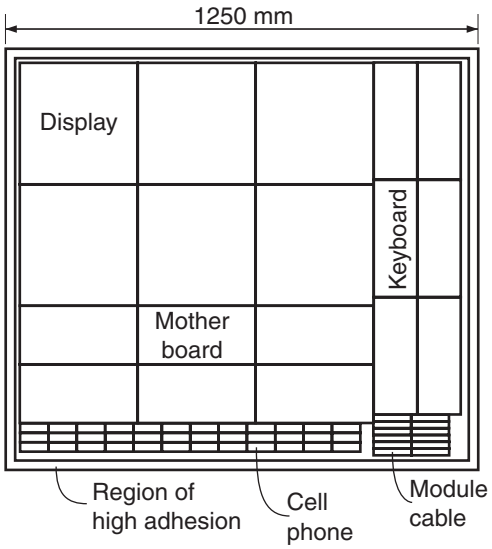

Figure 1, Glass layout for mobile computer

A powerful blade server component can also be manufactured as a single large flexible assembly, incorporating more than 100 processing units, as shown in Figure 2.

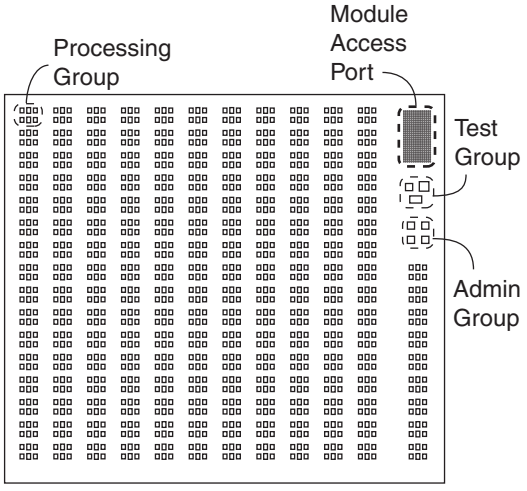

Figure 2, Glass layout for blade server

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2.1. Comparative glass manufacturing costs

Industry executives have estimated the cost per square inch of glass processing for a 7-layer TFT process at less than $0.25 for 7th generation substrates and a fully loaded fab. This compares favorably with an unfinished cost of $0.43/in^2 for an 8-layer Cu-based PCB using much larger geometries, not including any active circuits (like TFTs), and not capable of direct attachment of IC chips.

3. Interconnection Circuits

Figure 3 shows a cross-section of an 8 layer interconnection circuit with trace width, w = 5 microns, spacing, s = 5 microns, and thickness, t = 1 micron. Photo BCB (benzocyclobutene) is the preferred interlayer dielectric, and 2-level contacts are shown.

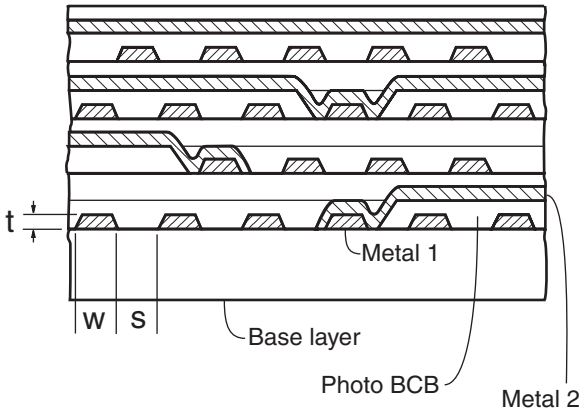

Figure 3, Eight Layer interconnection circuit

4. Flip Chip Bonding Structures

Figure 4 illustrates gold stud bumps, as produced by a Kulicke & Soffa 8098 bonder, using gold wire with 18-micron diameter.

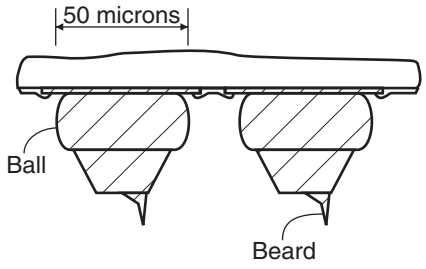

Figure 4, Gold stud bumps

Preferably, stud bumps such as shown in Figure 4 are provided on all of the IC chips to be assembled. The motherboard is prepared for receiving the stud-bumped devices by building wells filled with solder, as shown in Figure 5. Because the glass carrier is so large, and because this process step is performed before dicing the carrier into individual circuits, several million wells are typically formed with one pass of the squeegee, resulting in a cost/well of less than 0.02 cents.

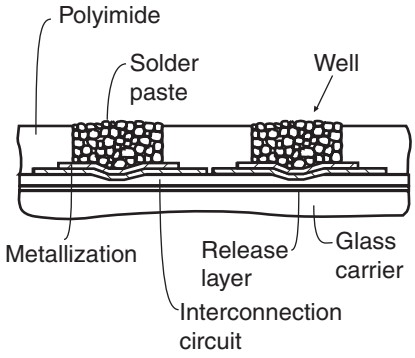

Figure 5, Wells filled with solder

The IC chips are aligned with the motherboard (still on the glass carrier), and the stud bumps are inserted into the wells. After heating to melt the solder paste, the result is shown in Figure 6.

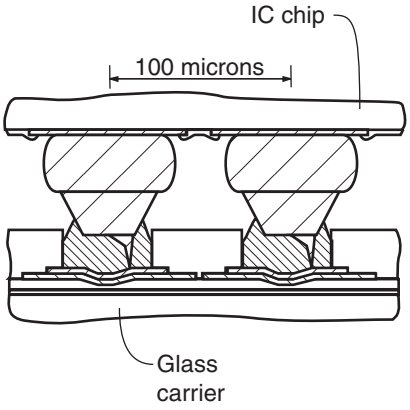

Figure 6, Flip Chip bonds

4.1. Cost per flip chip bond

Kulicke & Soffa has provided cost data for 8-inch wafers having 200,000 stud bumps at 0.03 cents per stud bump. This leads to a total cost per flip chip bond of less than 0.05 cents.

4.2. Rework of Defective Chips

If a part is defective, it is removed by applying heat to the glass carrier, and hot inert gas to the defective chip. The wells and the surrounding area are cleaned and touched up as necessary. Then a new part is installed and tested. Because the glass carrier provides mechanical support and dimensional stability, and because the substrate materials can easily handle the solder melting temperature, the rework process can be repeated as often as necessary, even with tight pad spacing.

4.3. Tester-On-Board (TOB)

It is proposed that modern test technology is capable of Tester-On-Board (TOB), wherein special-purpose test chips are mounted directly alongside the system components and mimic all the capabilities of external testers. Sophisticated pin electronics are generally required to provide drivers and receivers between the device under test (DUT) and an external tester. Eliminating this complexity is highly desirable; the system can then be tested at full speed and with improved noise margins. If digital, analog and RF functions are required then multiple test chips will be necessary. However, adding these test chips to the system using the SysFlex approach is not as expensive as in the past because the production volume of the test chips will be high, leading to low unit costs, and the cost of packaging and assembly will be minimal. Thus, a tester is included with every module produced. However, more efficient production, shorter time to market, and improved usability of fielded products may redeem its cost. Imagine devices that track critical system health indicators, and take action before faults occur. The cost of testing is currently around 4% of manufacturing cost. If 4% or fewer system chips are test chips, lower test costs may be achieved.

The test program is preferably a version of the user program, wherein all of the system components and capabilities are thoroughly exercised. Normally this is programmed in a high-level language. The test environment is the actual system, rather than a simulation provided by test vectors; this can lead to more accurate and meaningful tests at lower cost.

5. Testing the interconnection circuit

A module access port is provided on the motherboard for additional testing flexibility, as shown in Figure 7. The pad pitch is again 100 microns or less, providing access to a large number of circuit nodes. For example, a medium complexity motherboard may have 4,000 nodes, and these connections would occupy just 0.4 cm^2 at the 100-micron pitch. The module access port is also used for validating the special purpose test chips, and optionally for testing each component as it is assembled, for debug purposes.

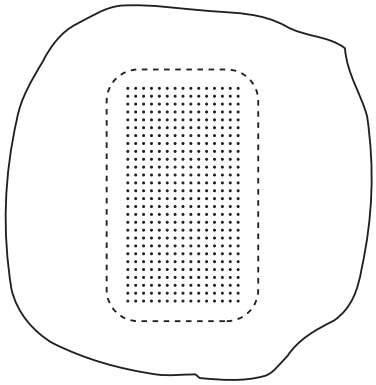

Figure 7, Module access port

Figure 8 shows a circuit assembly being tested using a test fixture manufactured by the same process as the motherboard.

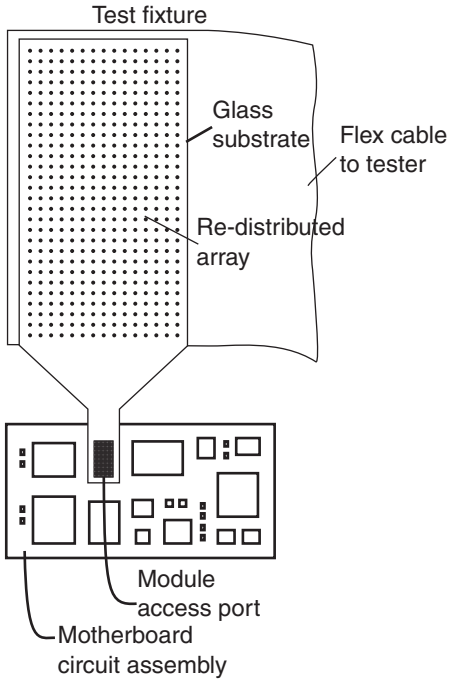

Figure 8, Test fixture

6. Module hermeticity

Traeger [3] has documented the water permeabilities of silicones, epoxies, fluorocarbons, glasses and metals. In terms of providing a barrier to water, his data shows that a

1-micron thick layer of metal is approximately equivalent to a 1mm thick layer of glass, and also equivalent to a 100cm thick layer of epoxy. Accordingly, if an electronics module can be fully enclosed in a layer of continuous metal at least one micron thick, the hermetic properties should be quite good. However, it is necessary in any useful electronic system to communicate data and/or commands with other systems, and this requires something like a module access port for signals and power. The module access port is preferably built using a semi-hermetic structure surrounding each module access pad. Coating schemes are available using sputtering or evaporative systems that provide continuous metal at the top, bottom, and edges of an electronic module. An electronic circuit with these "module packaging layers" is shown in Figure 9.

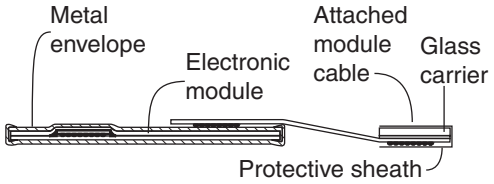

Figure 9, Hermetic module

This module has an attached module cable because the assembly of the cable needs to occur before the glass carrier is removed, and the carrier must be removed before the bottom layer metal is applied. These constraints are necessary to preserve the dimensional stability provided by the carrier through all of the precision assembly steps.

7. Electromagnetic screen

The same metal envelope that provides protection against water also provides an effective electrical screen around the module for reducing electro-magnetic interference, EMI, and particularly electro-magnetic radiation, EMR, produced by the module. The metal envelope also reduces electro-magnetic susceptibility, EMS, by reducing the effect of external electrical noise on circuits within the module.

8. High-density edge connector

At the same time as the wells are created for the flip chip bonding sites, elongated wells can be created for a high-density edge connection. This is illustrated in Figure 10, where the pitch of the edge connector traces can be 200 microns or less, again assuming that the presence of the glass carrier is maintained until the connection is made.

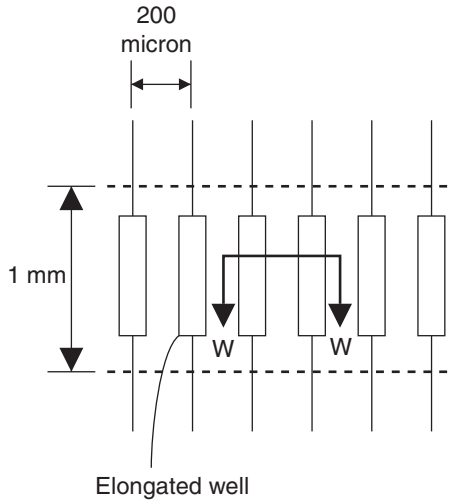

Figure 10, Edge connection scheme

Figure 11 shows solder paste filling the elongated wells
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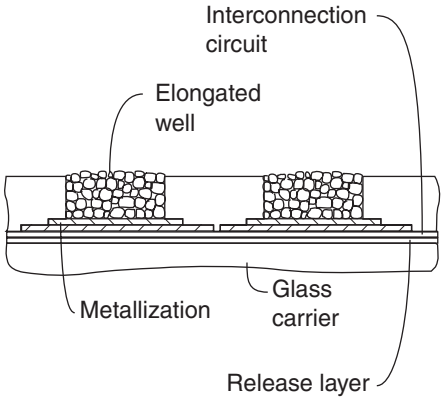

Figure 11, Elongated wells in cross section

After aligning the circuits in face-to-face relation, the region is heated and the solder melted to create the permanent high-density connection shown in Figure 12, which is a view through section WW of Figure 10.

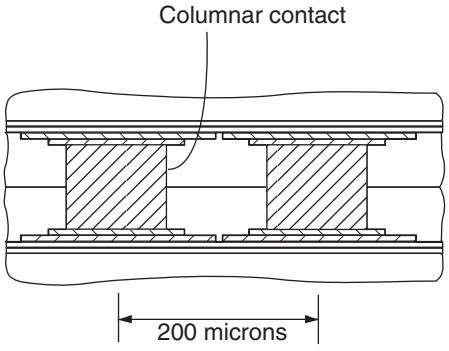

Figure 12, Permanent edge connection

9. Process flow charts

Figure 13 summarizes the process steps to create a tested circuit assembly, starting with a bare glass substrate.

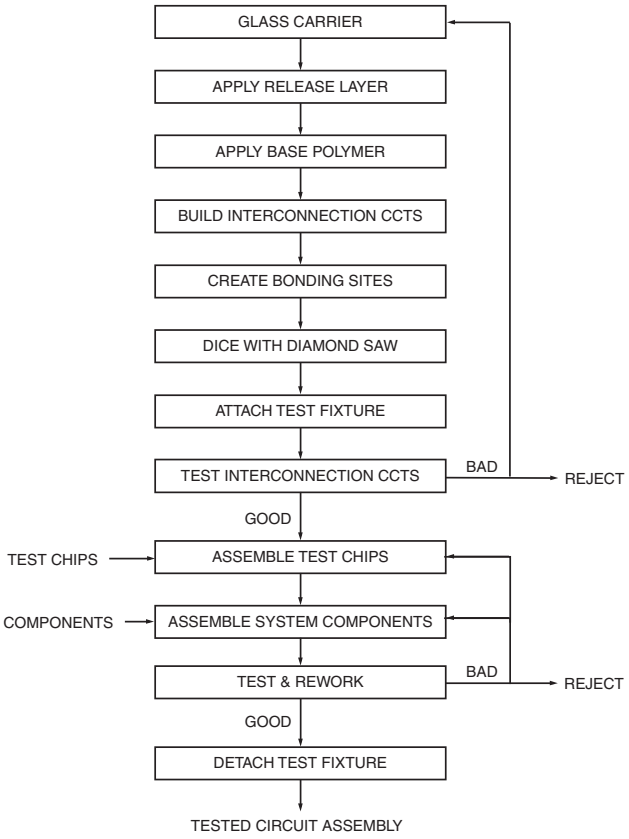

Figure 13, First process flow chart

Figure 14 summarizes the further steps required to convert a tested circuit assembly into an electronic circuit module.

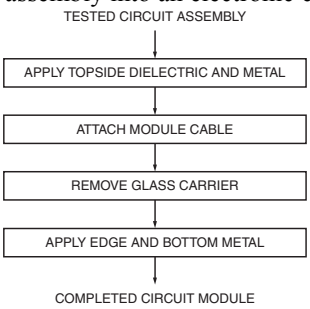

Figure 14, Second process flow chart

10. Thermal design

Figure 15 shows a cross-sectional view of a blade server component such as described in Figure 2, combined with a fluid-filled heat sink. The thermal impedance, θ_{JC}, from junction to coolant can be very low. By eliminating packaging structures and providing such a low impedance thermal path, the IC chips can run at increased power without exceeding their maximum junction temperature.

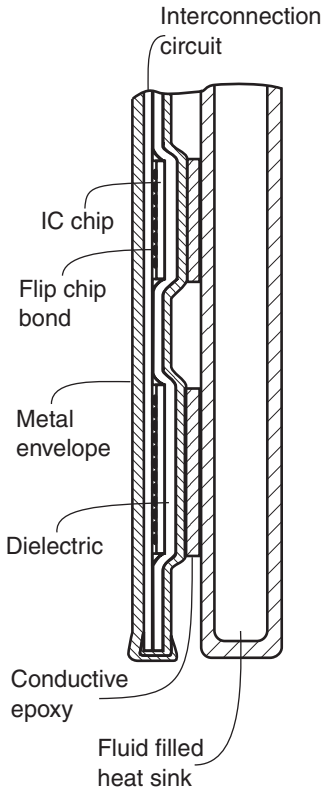

Figure 15, Water-cooled blade server/supercomputer

It may be possible to modularize the plumbing and the electrical connections to make a high-performance replaceable unit. One can also imagine a super-computer comprised of large panels, each with several hundred tightly coupled processing groups, and the panels closely spaced using cooling methods similar to those described in Figure 15. By this means, the greatest amount of silicon can be assembled in the smallest possible volume. This provides short signal paths for maximum performance, the ability to rework the assembly until all defective parts have been replaced, and effective cooling to prevent a meltdown.

11. Roll Up Components

A shape memory material such as Nitinol may be used to stiffen the flexible circuits for applications such as displays, keyboards, and sensors. The stiffening sheet is laminated with the flexible circuit after the glass carrier is removed. Nitinol is an alloy of nickel and titanium, and can be produced in cold-rolled sheets that have shape memory and are super-elastic at room temperature. A suitable thickness is around 50-100 microns. Newly developed polymers also have shape memory properties. Figure 16 shows a mobile computer that can be built with the techniques discussed herein. With a 12x9-inch display and full size keyboard, it can weigh less than one pound.

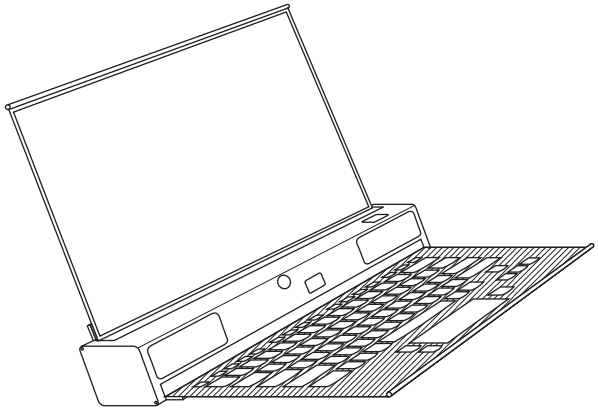

Figure 16, Mobile computer with roll up components

The display can be built using a transparent flexible substrate material such as polyethylene terepthalate (PET) or polyether sulfone (PES). These substrates can tolerate 200ºC processing of the TFT back plane circuits that may be based on low-temperature polysilicon, or alternatively on polymer switching devices that are currently under development. Clear substrates are required for bottom-emitting Organic Light Emitting Diode (OLED) displays. Tiny spots of organic material for each color can be deposited at each pixel location using modified ink jet printers, as have been developed by Litrex in Pleasanton, California.

A straw-like cylinder is provided at the edge of each roll up component. The user can roll his or her fingers over the cylinder to roll up the device, and click it into place inside the enclosure. The rhombus shape of the enclosure facilitates this process. After the keyboard has been rolled up and stored, the device is rotated through 60 degrees so that the display is lying flat on the work surface, and can be similarly rolled up.

Capacitive sensing technology may be employed for all of the touch sensors. The keyboard assembly may include separate TFT arrays for the key array, a touch pad, and a fingerprint sensor. When the display and keyboard are rolled up, the mobile computer is transformed into a compact package, as shown in Figure 17. The edge length of the rhombus can be 2 inches for a model with a 12x9-inch display and a full size keyboard, and a simple fixed-focus camera can also be provided within the 1 pound weight budget.

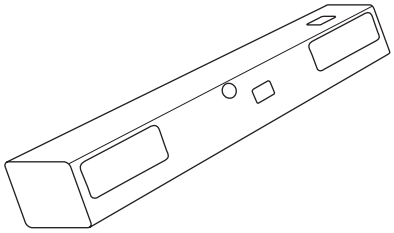

Figure 17, Mobile computer in its stored state

12. Acknowledgments

Prior work on non-impact printing structures provided the basis and illuminated the possibilities for fine-featured flexible circuits. This work was performed at The Salmon Group, LLC, Los Altos, California, and was funded primarily by David M. Salmon. I'd also like to thank Dann Gustavson for his review and insightful comments on testing.

13. References

[1] Peter C. Salmon, "Electronic System Modules and Method of Fabrication", *U.S. Patent Application*, 9/7/02, pp. 1-47.
[2] Peter C. Salmon, "Computing Device with Roll Up Components", *U.S. Patent Application*, 9/7/02, pp. 1-47.
[3] R. K. Traeger, "Hermeticity of Polymeric Lid Sealants", *Proc. 25th Electronics Components Conf.,* 1976, p. 361.