Benchmarks for Interconnect Parasitic Resistance and Capacitance

(Invited)

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Abstract

Interconnect parasitics are dominating circuit performance, signal integrity and reliability in IC design. Copper/low-k process effects are becoming increasingly important to accurately model interconnect parasitics. Even if the interconnect process profile is accurately represented, approximations in parasitic extraction could cause large errors. Typically, researchers and designers have been using pre-defined set of structures to validate the accuracy of interconnect models and parasitic extraction tools. Unlike industry benchmarks on circuits such as MCNC benchmarks, no benchmarks exist for interconnect parasitics. This paper discusses the issues in accurate interconnect modeling for 130nm and below copper/ultra low-k technologies. A set of benchmark structures that could be used to validate accuracy and compare parasitic extraction tools is proposed. Silicon results from 130nm technology are presented to illustrate the usefulness of these benchmarks. Results of application of these benchmarks to compare parasitic extraction tools are presented to demonstrate systematic validation of resistance and capacitance extraction.

1. Introduction

Accurate modeling of interconnect parasitics is listed as one of the difficult challenges in ITRS Modeling and Simulation section [1]. Accurate modeling of Deep Sub Micron (DSM) processes, efficient parasitic extraction/model order reduction are needed to ensure predictable performance, signal integrity and reliability of IC designs. It is quite common in the industry to use some set of simple structures and real design examples to validate the accuracy of parasitics and how they impact circuit performance/signal integrity. Unlike industry benchmarks on circuits such as MCNC benchmarks, no benchmarks exist for interconnect parasitics. Availability of benchmark structures that encompass DSM processes and broad range of design scenarios would help designers, tool developers and academia in easily comparing different tools and methods. This paper proposes a benchmark for parasitic resistance (R) and capacitance (C). This benchmark proposal can be extended to include inductance (L) and electrical analysis such as delay, noise, electromigration, and voltage drop.

This paper is organized as follows. A few key aspects of interconnect modeling in DSM processes are covered in section 2. Section 3 covers a summary of key aspects in parasitic resistance and capacitance extraction. Section 4 includes benchmark proposal followed by results on 130nm copper technology in section 5. A summary of the benchmark proposal is discussed in section 6.

2. Accurate Interconnect Modeling

In this section, four key aspects of DSM process are discussed: Non-linear resistance in copper, Selective Process Bias (SPB), dummy (fill) metal and process variations. All these have significant impact on accurate modeling of parasitic RC elements.

Metal sheet resistance (Rsheet) is not a constant parameter ([4], [5]). As shown in Fig.1, sheet resistance varies as a non-linear function of line width in 130nm copper technology. Two phenomena cause significant systematic changes in sheet resistance as a function of line width for copper technologies. The first one is due to scattering of electrons off of the edges of the conductor. The second includes systematic changes in copper cross-sectional area as a function of line width that are induced by the damascene process flow. An example of such an effect is CMP (Chemical Mechanical Polishing) induced copper dishing that would increase resistance. Slotting and dummy metal is often used to address dishing effects.

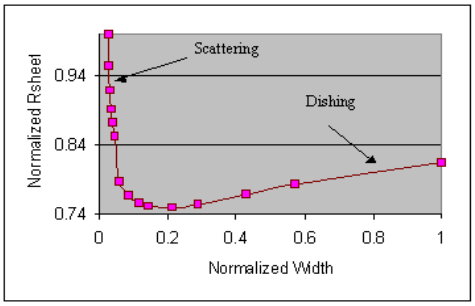

Fig.1 Non-linear relation between Rsheet and line width

In DSM copper technologies, as route dimensions are becoming increasingly smaller, "what you draw is not what you get". This effect is referred to as Selective Process Bias (SPB) in this paper (different terms used in the industry to describe this effect). As shown in Fig.2, effective line width (and hence effective spacing) varies as a function of drawn width and spacing. It should be noted that isolated lines could have significant change in width. Change in width can be negative and positive as well, depending on the spacing of a given line to adjacent line(s). Fig. 3 shows the combined effect of SPB and non-linear resistance for narrow line widths. It can be easily seen that simplistic modeling of resistance can result in significant errors.

Dummy (or fill) metal is introduced in the interconnect

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process flow to enable uniform thickness control in CMP process. Dummy metal needs to be treated as floating metal unless it is intentionally connected to constant potential. Another issue is that multiple instances of a design block could get different dummy metal based on location, leading to a systematic change in capacitance on multiple instances. Process variations induced due to changes in local and global densities is another key aspect to be accounted in accurate parasitic modeling.

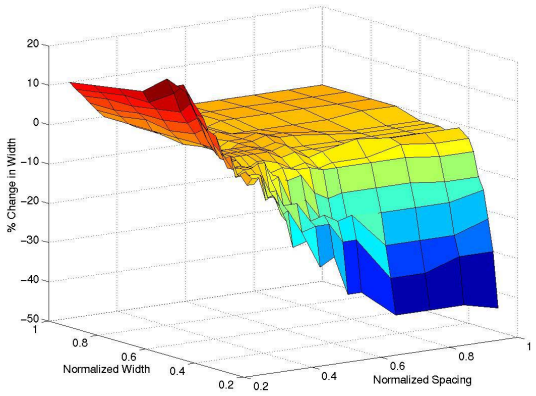

Fig.2 Change in Effective line width due to SPB

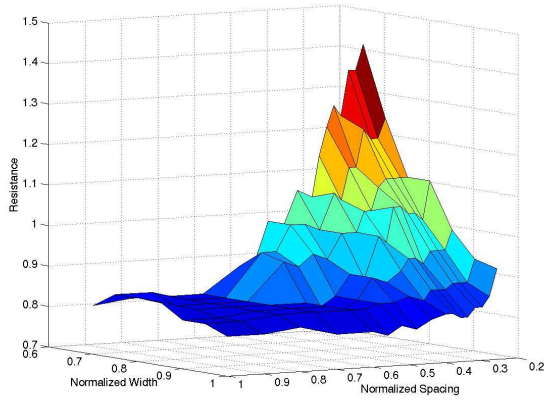

Fig.3 Change in Effective resistance due to SPB

3. Parasitic RC Extraction

Resistance extraction is much simpler than capacitance extraction. Most of the tools use square-counting method combined with some fracturing algorithm for resistance extraction. Net-An™ uses field solver technique to extract resistance.

Several capacitance extraction techniques exist ([2], [3]) ranging from simple analytical expressions [6], to field solver techniques [13] and statistical techniques [12]. As shown in Fig.4, these techniques provide varying speed v/s accuracy trade-offs. Full 3-D solver tools such as Raphael™ are used for detailed TCAD extractions on small structures. Fast full-3D methods such as Net-An™ enable use of field solver techniques on large designs. Pseudo-3D methods use some form of pattern matching and pre-computed capacitance look-up tables. Most of chip-level parasitic extraction tools fall into this category. Area/perimeter method, 2-D or 2.5D equation based methods are quite common in physical design tools for quick estimation of parasitic capacitance. Whereas all these techniques are deterministic, statistical random-walk technique used in QuickCap™ allows variable accuracy v/s runtime trade-off. Also, QuickCap™ doesn't suffer from errors due to approximations in deterministic methods.

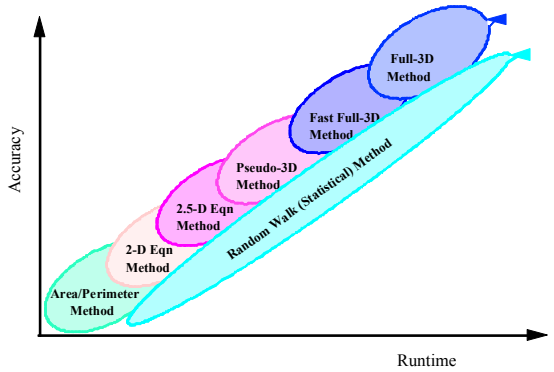

Fig.4 Comparison of Capacitance Extraction Methods

Silicon validation of parasitics is critical to close the loop between process and parasitic extraction. CBCM (Charge Based Capacitance Measurement) technique [11] is often used to measure capacitance besides traditional passive methods. Resistance measurement is typically done using I-V method. Silicon measurements are extremely helpful in modeling process variations and systematic effects ([12], [13], [14]).

4. Benchmark Proposal

The resistance and capacitance benchmark proposal in this paper covers key process issues discussed in section 2 and key careabouts in analog/digital designs.

No	Structure Type	Purpose
1	Routing pitch lines	Simple checks/Process monitoring
2	Lines for several width/space	SPB and non-linear resistance
3	Wide lines with slots	Accurate R in presence of slots
4	Custom routes	Accurate R for bends/junctions
5	Variable overlap on contacts	Overlap-based contact resistance
6	Variable overlap on vias	Overlap-based via resistance

Table –1 Summary of benchmarks for Resistance

A summary of key structures for resistance benchmarks is captured in Table-1:

1. *Routing pitch lines*: These are lines with common routing pitch for a given technology and are helpful in process monitoring and simple checks on the accuracy of resistance.
2. *Lines for several width/space*: These are extensive set of structures that cover the commonly used width/space combinations for a given technology. These structures help in validating SPB/non-linear resistance modeling.
3. *Wide lines with slots*: These structures help in validating the accuracy of parasitic resistance in the presence of slots.
4. *Custom routes*: These are routes that consist of combinations of bends, slots and junctions. Fracturing techniques used in resistance computation play an important role to achieve good accuracy.

5/6. Variable overlap on contacts/vias: These structures help in

accurate modeling of contact/via resistance due to misalignment and width reduction.

No	Structure Type	Purpose
1	Process-sensitive structures	Simple checks/Process monitoring
2	Lines w/ several width/space	Accurate C in presence of SPB
3	Custom routes	Accurate C for custom routes
4	SRAM bit-cell	Overlap-based contact resistance
5	Standard-cell parasitics	Transistor-level parasitics
6	Sparse routes	Dummy metal effect
7	Real routes from designs	Combination of several effects

Table –2 Summary of benchmarks for Capacitance

A summary of key structures for capacitance benchmarks is captured in Table-2:

1. *Process-sensitive structures*: These are simple 2-D structures that are sensitive to process parameters such as metal thickness/width/spacing and ILD (Inter Level Dielectric) thickness. Fig.5 shows the vertical cross-section of two structures, left structure is sensitive to metal thickness/width/space and right wide structure sensitive to ILD.

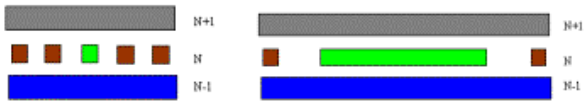

Fig.5 Structures routing pitch and ILD structures

2. *Lines w/ several width/space*: These 2-D/3-D structures exercise the same width/space combinations as resistance and help in analyzing SPB effect on capacitance.
3. *Custom routes*: These are structures typically found in Datapath and/or custom designs. Some examples of these structures are shown in Fig.6 to Fig. 9. Fig.6 shows a route in MET3 coincident with routes in MET2/4. Fig.7 shows a structure where route in MET3 has routes in MET2/4 coincident on edges. Fig. 8 shows a routing structure where route in MET3 has signals in MET2/4 diagonally opposite. Fig.9 shows a structure where route in MET3 has partial overlap from signals in MET2/4. Several other structures found in custom routes would be included in this category.

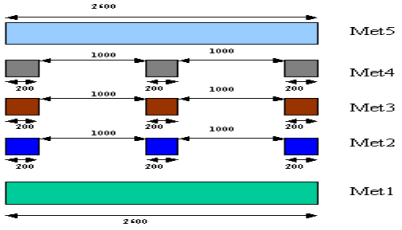

Fig.6 Structure with coincident signals

4. *SRAM bit-cell*: These include bit-line and word-line structures. A key aspect of accurate modeling in this case is modeling via/contact capacitances.
5. *Standard-cell parasitics*: These include examples of standard cells, where modeling of transistor-level parasitics is key to accuracy.
6. *Sparse routes*: These structures help assess accuracy in the presence of both inter and intra-level dummy metal.
7. *Real routes from designs*: These structures are selected from real designs that help evaluate the combined effect of structures discussed earlier.

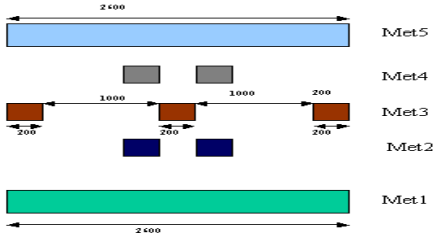

Fig.7 Structure with coincident edges

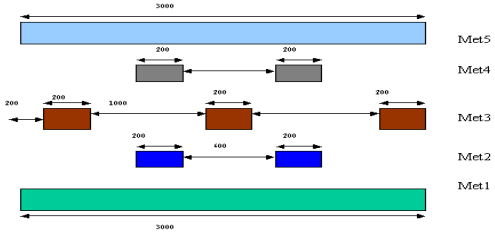

Fig.8 Structure for diagonal capacitance

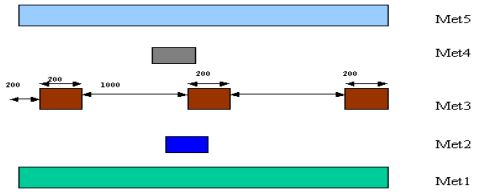

Fig.9 Structure width partially overlapped signals

These benchmarks can be represented in standard LEF/DEF and GDSII format. EDA vendors working with design houses/foundries could use real technology profiles and academia could use IRTS [1] to obtain technology parameters. In reporting of the results, statistical attributes of distribution of errors (mean, median, sigma and Cpk) should be reported.

Whereas it is feasible to place most of these benchmark structures in silicon to obtain correlation to silicon, a practical approach would be to qualify a reference extraction tool against silicon on as many structures as possible and use that reference extraction tool for further validation. Silicon validation should cover the bounds of the interconnect process parameters and SPB/non-linear resistance models to qualify a reference extraction tool.

Impact on circuit delay is also often used to evaluate the errors induced due to parasitic RC. All the above benchmarks could be used in the context of a ring oscillator and/or critical path to determine the impact of circuit delay. Silicon validation of circuit delay can be easily obtained using a combination of transistor dominated and interconnect dominated ring oscillators.

5. Results

In this section, results on a subset of the benchmarks proposed in section 4 are presented. These include results from silicon measurements of 130nm copper technology and comparison of commercial parasitic extraction tools against reference parasitic extraction tool. Resistance measurements were obtained by using I-V method. Capacitance measurements

were obtained by an enhanced CBCM technique. Fig.10 to Fig.14 show histograms of silicon measurement data from 60 lots for more than 12,000 sites. In Fig.10, X-axis corresponds to resistance scaled to minimum and maximum process specifications (-100 and +100 correspond to minimum and maximum resistance specification respectively). Similarly, Fig.11 to Fig. 13 have capacitance scaled to minimum and maximum process specifications.

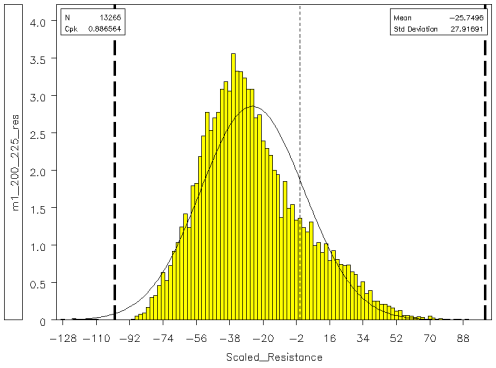

Fig.10 Resistance Si results on MET1 routing pitch

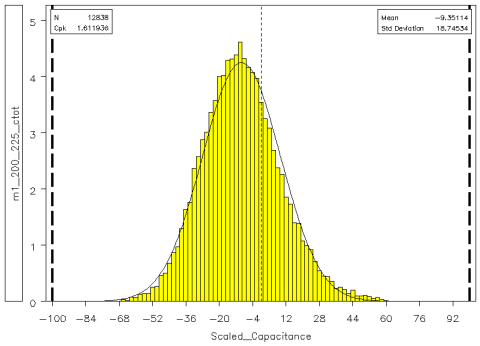

Fig.11 C-total Si results on 2-D MET1 structure

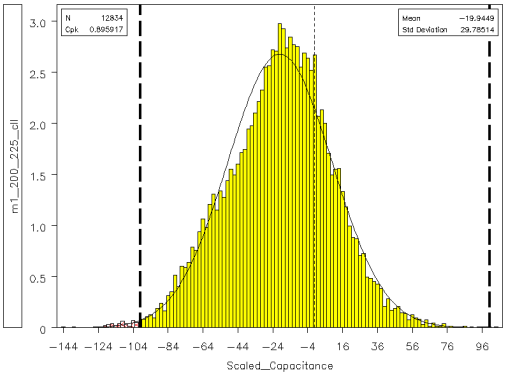

Fig.12 C-l2l Si results on 2-D MET1 structure

Fig. 10 shows distribution of measured resistance for routing pitch dimensions. Fig. 11 shows distribution of measured total capacitance on 2-D MET1 structure that is sensitive to metal thickness/width/space (left structure in Fig. 5). Fig. 12 shows line-to-line (C-l2l) for the same structure. Fig.13 shows total capacitance for wide structure (right structure in Fig. 5) that is sensitive to ILD variations. This silicon data provides good confidence in interconnect models and reference extraction tool used in determining upper and lower specification limits.

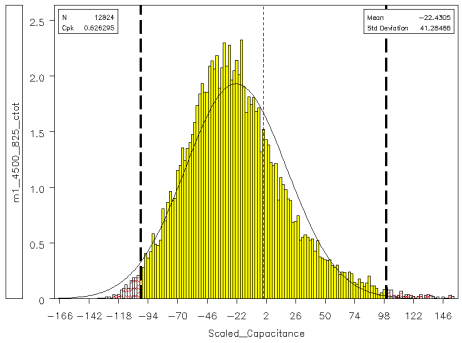

Fig.13 C-total Si results on 2-D MET1 ILD structure

Fig. 14 shows the silicon results for MET1 dominated interconnect ring oscillator that exhibits consistent behavior with R and C observations.

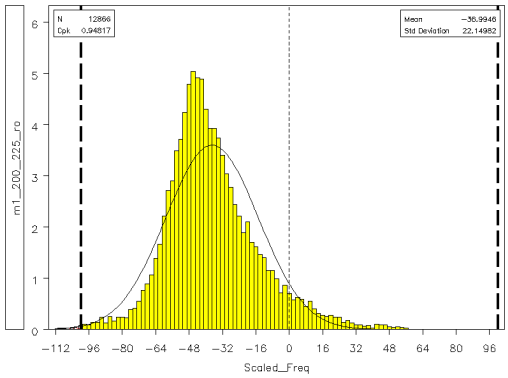

Fig.14 Si results on MET1 dominated Ring Oscillator

A summary of comparison of total capacitance on 78 structures against reference extraction tool is shown in Fig. 15. In this figure, silicon results are plotted with USL (Upper Spec Limit) corresponding to +100 and LSL (Lower Spec Limit) corresponding to –100. Mean/+3sigma/-3sigma is shown for each structure. It can be seen that reference extraction tool bounds silicon results.

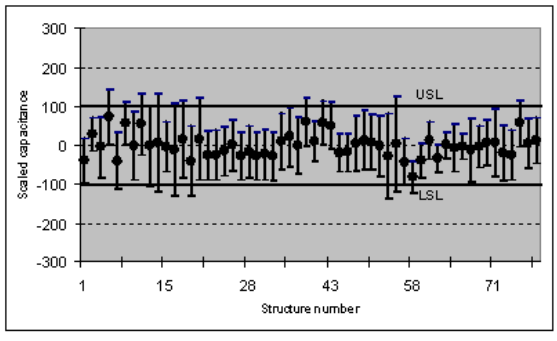

Fig.15 Si results for reference extractor

When commercial parasitic extraction tools were used on custom routes and compared against silicon results, limitations

of the tools became more apparent. Four different post-layout extraction tools (A, B, C and D) were used on custom routes (row 3 in Table 2). A_{min}, B_{min}, C_{min} and D_{min} correspond to minimum capacitance process corner for tools A, B, D and D respectively. A_{max}, B_{max}, C_{max} and D_{max} correspond to maximum capacitance process corner for tools A, B, D and D respectively. In Fig.16, though silicon results from 510 data points are well bounded by all tools, it can be seen that tools B and C fall short of reference tool A. For diagonal capacitance structure, tool B totally misses silicon data as shown in Fig. 17. Tool C narrowly covers lower bound. In Fig. 18, it can be seen that tools B and D miss most of silicon data for structure with coincident edges. Tool C misses good amount of data on lower side.

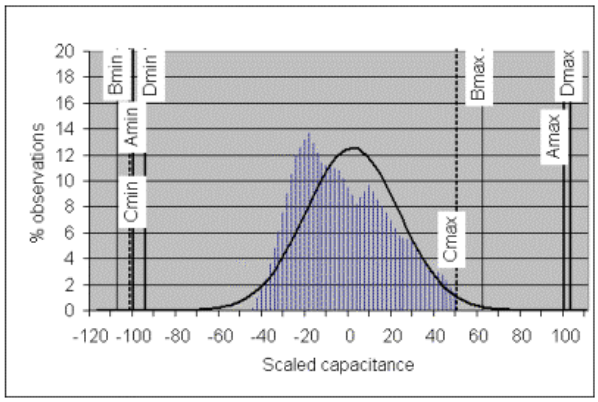

Fig.16 Si results on isolated route in MET3

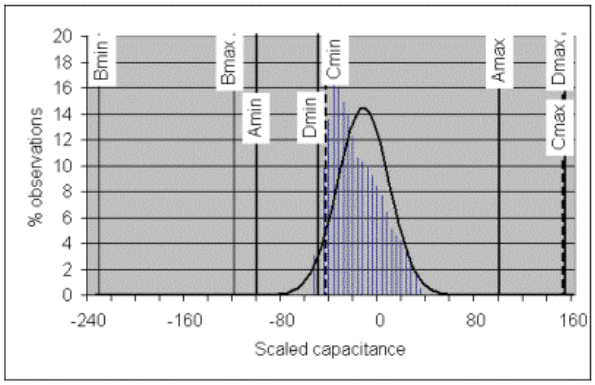

Fig.17 Si results for diagonal capacitance structure

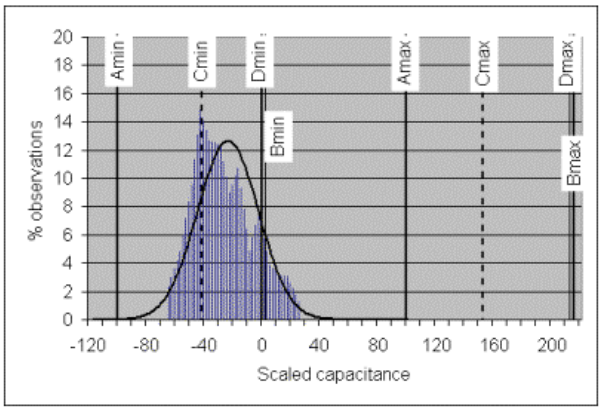

Fig.18 Si results for coincident edges structure

Fig. 19 shows silicon results for total capacitance on a clock route that was "cookie cut" from a real design. It can be seen that tool B completely misses silicon data and tool D is more pessimistic on the upper bound. Fig. 20 shows a structure that has several bends in MET2 and MET3. In this case, tool C is optimistic and misses silicon data, whereas tool B is pessimistic and misses the data.

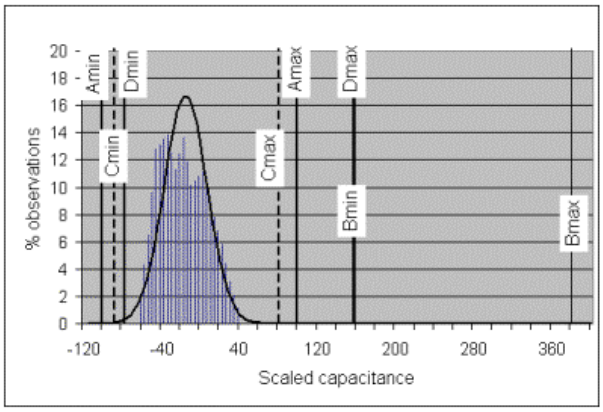

Fig.19 Si results for clock route

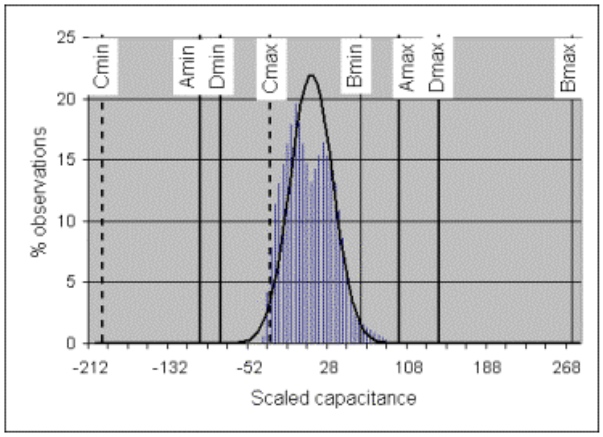

Fig.20 Si results for structure with bends in MET2 and MET3

The value of these benchmarks can be easily seen as a systematic method to compare EDA tools and identify areas of improvements. Table-3 shows a summary of Cpk values of silicon distribution. Cpk = min {(USL- μ/3σ), (μ – LSL/3σ)}, where μ and σ are mean and sigma of distribution. As Cpk is dependent on LSL and USL values, a distribution not centered on mean would have a lower value. A Cpk value greater than one is an indicator of good distribution. It can be clearly seen that tool-A, that happens to be reference extraction tool has best Cpk values and bounds silicon data very well.

Structures	Tool-A	Tool-B	Tool-C	Tool-D
2-D	1.07	0.67	0.82	0.86
3-D/Custom	1.24	-0.56	0.41	0.53

Table 3 Summary of average Cpk values for different extractors

Fig. 21 shows a structure that is helpful in quickly assessing the impact of floating metal. This structure is identical to ILD structure shown in Fig.5, except that top plate is floated. Silicon results on capacitance are shown in Fig. 22. It can be

clearly seen that only if the top plate is modeled as floating, silicon data can be bounded. This data can be related to the impact of floating dummy metal.

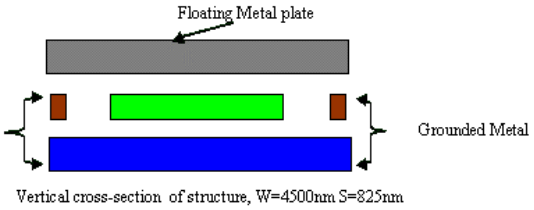

Fig.21 Structure to assess impact of floating metal

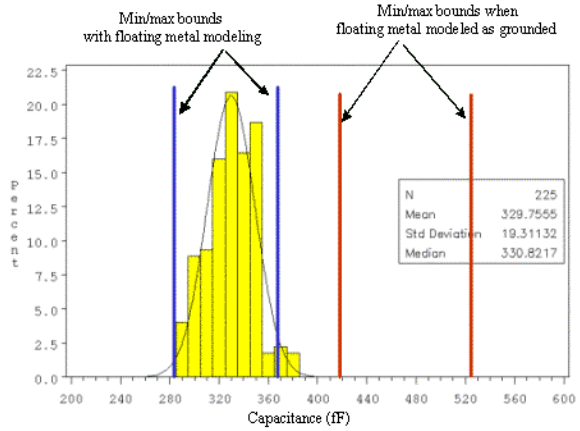

Fig.22 Si results for structure with floating metal

Fig.23 shows distribution of %difference in capacitances in running tool-B and tool-D in two modes on 1082 nets chosen from a high performance DSP design. Tool-A is used as reference tool in this case. It can be seen that Tool-D (Mode1) has a good distribution relative to Tool-B or Tool-D (Mode2), but has the mean off-centered. For +/-10% bounds, Cpk of Tool-D (Mode1) can be improved from 0.71 to 1.48 by shifting the mean to zero. Tool-B and Tool-D (Mode2) are centered on zero and have Cpk of 0.57 and 0.62 respectively.

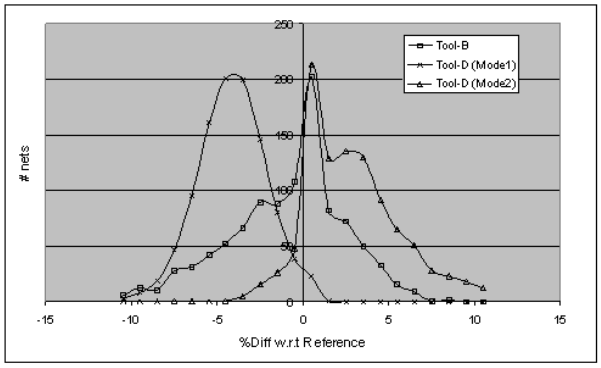

Fig.23 Comparison of tools against reference tool

6. Summary

A benchmark suite has been proposed for interconnect parasitic resistance and capacitance. These benchmarks cover both the realities of DSM processes and key design careabouts in analog/digital designs. These benchmarks can be easily implemented in silicon to ensure a thorough validation of interconnect models and reference extraction tools. All these structures could be represented in industry standard LEF/DEF and GDSII format.

Similar to MCNC benchmarks, these interconnect benchmarks can provide a mechanism to aid research in academia and industry. Commercial parasitic extraction tools can be compared against these standard structures and validated against silicon as well. Accuracy of parasitics can be validated for approaches in [8] and [9]. EDA vendors could use real technology data from design houses/foundries and IRTS [1] interconnect process parameters can be used by academia. In addition to accuracy of R and C, impact on circuit delay can be measured using ring oscillators and/or critical paths.

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