LYS: A Solution for System on Chip (SoC) Production Cost and Time to Volume Reduction

Jean-Pierre HELIOT
Director, Library Yield Improvement Group (LYIG)
Central R&D
STMicroelectronics
jean-pierre.heliot@st.com

Florent Parmentier
Library Yield Improvement Group
Central R&D
STMicroelectronics
florent.parmentier@st.com

Marie-Pierre Baron
Library Yield Improvement Group
Central R&D
STMicroelectronics
marie-pierre.baron@st.com

Abstract

With the introduction of new generations of Systems on Chip (SoC) on 0.18 µm and 0.12µm technologies, the production cost and time to volume become more and more critical, on top of best in class level of quality and reliability. The SoC approach – widely based on the usage of cell libraries or reusable IP blocks – brings extreme complexity. Accurate knowledge and level of validation on silicon of each block of library/IP used within new chip becomes mandatory in order to secure first silicon success.

In this context, knowledge sharing between users of the same IP in different SoC plays a key role in cost optimisation & time to volume reduction.

This paper describes the information system solution developed on 0.18µm technology, named LYS (Library Yield System). LYS allows keeping track of the version of library cells or reusable IP blocks used within each SoC of a given technology. Each SoC project is analysed at different steps of its life cycle starting from product specification up to silicon qualification. Block by block silicon results applied to SoC, and early warning system linking the different projects together, allow to optimise and update in real time the content of each projects, and to perform the needed improvements.

This methodology allows, before mask order, any new project to be updated with appropriate library or IP blocks revision in order to get rid of known silicon issues detected on previous projects.

This solution is now fully implemented and in use on 0.35µm, 0.25µm, 0.18µm, 0.12µm, and 90nm technologies.

As far as we know, there is no equivalent solution available & running in microelectronics companies.

1. Introduction

The complexity of new System on Chip (SoC) is not only requiring the most advanced 0.18µm or 0.12µm technology platform with wide process options, best in class design flow adapted for deep sub-micron (physical & electrical effect), library variety... but also strong knowledge sharing information system, linking library/IP and SoC together, starting from project specification, up to silicon validation.

For that purpose, an information system/risk analysis tool oriented has been developed, with the main target to ensure first silicon success & to improve both high volume product ramping-up and profitability.

This information system is regrouping by technology platform the following information:

- Technical data regarding libraries: features, versioning, level of maturity, process defectivity, comments & eventual technical limitation (warning, usage restriction)...
- System on Chip description: surface, library usage with versioning & associated level of qualification, yield prediction (global & block by block oriented).
- Silicon results, libraries & IP blocks oriented, collected and synthesised coming from qualification test vehicles or previous Systems on Chip.
- Yield results by category of libraries, initially based on models and updated thanks to real silicon data from the manufacturing volume.
- Library versioning references, comments & limitation that could bring interest to potential end user.
- Early WARNING information management, SoC oriented with communication to project manager of any event with potential risk for his/her project & proposed alternative solution.

This information system is able to improve:
- time to volume (thanks to product/library/IP knowledge sharing)
- cost (thanks to early warning system)
- reliability (thanks to central data storage)
- resources (thanks to statistics on libraries & IP usage)

Pertinent information is gathered all along the library flow: from design of qualification test vehicles, and all along product flow: from design of prototype to high volume production manufacturing.

This information permits to do product yield prediction, early warning communication and to collect statistics on library usage.

2. Library, IP and trace ability

Traditional flow for libraries or IP's goes through:
- layout of a qualification testchip
- diffusion of lots of the reticule containing the testchip
- wide electrical characterisation (temperature, voltage, process, frequency)

Library is subject to enhancement all along the flow, thus expressed through versioning. Clear knowledge of improvements of each version of a library element is crucial.

Each layout of library elements is identified thanks to a formalized set of information (called TAG). The TAG is a complete set of labels which allows to quickly and accurately identify the library element (information are: cell name, date of generation, technology, design kit used for generation…- see figure 1) TAG is attached to each layout of each library elements allowing to have for each System on Chip a comprehensive and accurate content.

Key milestones have been defined in the Library Yield System (LYS) all along the library flow:
- **design review** (quality assurance and full simulation results in line with specifications, appropriate certificate is then issued and consultable by any potential user)
- **silicon validation** (functionality proven on silicon with full characterization and performances compliant with target specification, appropriate certificate is then issued and consultable by any potential user)
- **silicon qualification** (library components reliability and functionality in full process window is assessed, appropriate certificate is then issued and consultable by any potential user).

Library Yield System (LYS) is filled in with pertinent information concerning the libraries such as: versions, improvements description & maturity levels (see figure 2).
3. Product Maturity/Qualification

Traditional flow for product goes through:
- Design
- Prototyping
- Pre-production
- Mass production

The key milestones for Library Yield System (LYS) all along the product flow are the following ones:

- **Maturity Checkpoint (MCP):** At the earliest stage of the product elaboration, the project is described in term of content in the Library Yield System (LYS) (Libraries, IP blocks). This is done via an intranet interface allowing for the project manager to be aware, in real time, of the level of maturity of each library element he/she is willing to use within his/her project. Depending on the level of risk the project manager is ready to handle, several alternatives in the choice of the design content are offered to him/her. Automatic extraction of the content of the product, associated with link to the library data from LYS permit to instantaneously show the maturity of all components of the product, comments, yield model & warnings. An analysis of the content of the product is provided; a picture of the product robustness is given.

- **Pad Ring Review (PRR):** With the introduction of very deep sub-micron technologies, pad ring (I/O ring) review with appropriate expert is absolutely mandatory. This review is organized and managed through the Library Yield System. This review is held couple of weeks before the database submission for mask ordering. The completion of this review with safe conclusion is a mandatory element authorizing the mask ordering.

- **Maturity Checkpoint 2 (MCP2):** similar to Maturity Checkpoint. A preliminary GDSII is needed. A tag extraction by a scan tool replaces the description entered by the designer of the product.

- **PG Review (PGR):** last check before the mask order. The final GDSII file is analysed based on TAG extraction and information contained in the Library Yield System. Mask ordering is authorized as soon as comprehensive check of the embedded libraries has been done.

- **Engineering Data:** Done as soon as first silicon is available. Electrical measurements (yields, functional tests, Operating Life Test, …) are made on products with a block-by-block approach. Embedded libraries are filled into the Library Yield System (LYS). Defectivity by block of library is extracted, benchmark on yield is done, anomalies are highlighted allowing to focus on the most critical one, and to clear all the issues before the production ramp-up. Real yield obtained is compared to estimated yield (detailed in next chapter).

- **Test For Manufacturing (TFM):** A methodology has been developed for that purpose. This step is a major key allowing to split the origin of the potential yield losses between the following categories: process marginalities on one given parameter, process defectivity, test program robustness, library design, top level design issues...

- **Product Ramping-Up Review (PRUR):** Done before the decision to launch any product in volume. Review of the content of the chip, latest information is gathered and updated on the libraries based on silicon available. Silicon results of the product are updated, decision to update library and to perform design fix prior to go in mass-production is taken during this review.

For each milestone, a report is sent to the SoC manager by the Library Yield Improvement Group (LYIG) in charge to manage the information system.

Some recommendations or mandatory modifications are highlighted. (See figure 3):
- library versions and redundancy needs (MCP and PGR)
- product floorplan (PRR and PGR),
- testability logic and test program (MCP,PGR,PMR).

![Figure 3: Reports sent to customers](image)

4. Yield Prediction

A yield prediction is established and provided to the user via the maturity checkpoint report.

During the technology development phase, yield prediction is based on models. It is then refined based on real silicon results extracted from manufacturing data.

Yield strongly depends on different parameters:
- process (number of masks, defectivity)
- chip design (area, library content, density, complexity...)

Defectivity is the main detractor for yield for a mature process.

Library testchip yield measurements allow defining “equivalent defectivities” values for each family of libraries (memories, digital part...)

The chip equivalent defectivity directly depends on library equivalent defectivity, weighted by areas.

Chip yield is then calculated using Murphy-Seeds law:

\[
Yield = \frac{1}{2} \left[ \exp\left(-\sqrt{D_{eq} \times S \times N}\right) + \left(1 - \exp\left(-\frac{D_{eq} \times S \times N}{D_{eq} \times S \times N}\right)\right)^2 \right]
\]

With \(D_{eq}\): Equivalent Defectivity (number of defaults/cm²/level, \(S\): area (cm²), \(N\): number of level.

5. Early Warning / Cost Reduction Time to Market Optimisation

Strict anticipation and early verification are key factors for production cost reduction and time to volume reduction.

Once an improvement has been identified for library element embedded in a product, the Library Yield System (LYS) allows to list all the products containing this library element and to go with, the product designers. A mailing is then made (see figure 4) and an action list is continuously followed to make sure all impacted designs are fixed.

![Figure 4: Early warning illustration](image)

Earlier the chip is described, more efficient the early warning mechanism is. The following figure (see figure 5) is a good illustration of the redesign impact on time to volume indicator.

Consider the following example: a Product A is in silicon debug phase: a potential improvement is detected in a library. A fix is identified. An extraction from LYS gives the list of products that use this library \(\rightarrow\) an Early Warning is sent. Suppose that 10 of these products are still in design phase, they can be immediately fixed.

The minimum duration from design to silicon is about a month. In 0.18\(\mu m\), several products were warned during design phase and improvements were applied without redesign impact on time and cost. As a consequence, for 0.18 \(\mu m\) technology, several months and a lot of money (mask-set, wafers...) were saved avoiding to reach silicon before the discovery of the improvement.

The PG Review is a perfect complement to the early warning mechanism: one of the main targets of the PG review (PGR) is to make sure all known library elements of a chip have been updated using the latest improved library elements.

![Figure 5: Redesign impact on Time to Volume](image)

6. Statistics

Different kind of information can be traced through the Library Yield System (LYS) as a function of time:

- Library improvement and maturity i.e. following of the product risk assessment.
- Visualisation of the technology platform, via the product status: Overview of all the projects in design, prototype and mass production quantities.
- Yield and defectivity evolution.
- Library usage and area repartition (see figure 6).

Such studies bring to a good knowledge of the overall platform, and a higher anticipation, key for prevention and for a better resource management.

![Figure 6: Statistics on area repartitions](image)
7. Data Collection Process

LYS is directly available through intranet.
The first connection to LYS automatically gives a guest profile to the user.
Guest profile gives access to the library catalog and associated improvement description.
Then, on request, and based on his/her role in the company, user’s rights can be extended according to the following profiles:
- **Library designer**: enters and updates the library description (version, maturity level, & improvement) at the key milestones of the library flow (refer to chapter 2).
- **Chip designer**: enters the chip content at the earliest stage in the design phase (ideally when specification is ready) and updates it regularly.
- **Product & test engineer**: provides engineering data for testchips or products.

Additionally, other profiles permit to access to LYS information in read mode (**viewer**), to send the reports (**support** – refer to chapter 3), and to manage the LYS database (**administrator**).
Note: access rights are restricted to the user’s organization in the company.

8. Conclusions

In the semiconductor industry, System On Chip (SOC) comes to extreme complexity & first silicon success requires best in class knowledge & level of validation on silicon of each block of library/IP’s used within new Chip. This information becomes mandatory in order to secure first silicon success & improve time to volume.

In this environment the LYS (Library Yield System) establishing a knowledge sharing between content of different Systems on Chip, as far as libraries and IP blocks are concerned, play a key role in production cost optimisation & time to volume reduction. This methodology allows, before mask ordering, any new project to be updated with appropriate library or IP block revision in order to get rid of known silicon issues detected on former projects. This solution is now fully implemented and in use as a company standard on 0.35µm, 0.25µm, 0.18µm, 0.12µm, and 90nm technologies, .18 µm, .12 µm, and 90 nm technologies.