Comparative Assessment of Adaptive Body-Bias SOI Pass-Transistor Logic

Geun Rae Cho Tom Chen*
Department of Electrical and Computer Engineering
Colorado State University
Fort Collins, CO 80523
E-mail:{geunc,chen}@engr.colostate.edu

Abstract

We present a silicon-on-insulator (SOI) pass-transistor logic (PTL) gate with an active body bias control circuit and compare the proposed PTL gate with other types of PTL gates with different body bias circuits in two different $0.13\mu m$ SOI CMOS technologies. The experimental results show that the proposed SOI PTL gate using the body bias controlled technique is superior in terms of performance and power consumption than other DTMOS PTL gates.

1 Introduction

SOI dynamic threshold voltage MOSFET (DTMOS)[1] has been shown to be very effective to realize high-performance and low-power systems using extremely low supply voltages. Since the gate and body of a DTMOS transistor is connected together, the controllability of the gate over the cannel can be improved for SOI devices and the device performance can be further improved by the virtue of reduced device threshold voltage. However, the major drawback of conventional DTMOS is that it suffers from a significant amount of current when the supply voltage is higher than diode turn-on voltage which is approximately $0.7V$. One way that can alleviate the drawback is to use auxiliary transistors so that the body voltage of the device is clamped on the voltage below the diode turn-on voltage, and a great deal of effort has been made for static SOI CMOS circuits[1, 2, 3, 4].

With power being more and more a limiting factor in high density and high-performance VLSI designs, PTL circuits have received a great deal of attention as an alternative high-speed and low-power circuit style. And, the applications of DTMOS technique to PTL have also been proposed in [5, 6, 7]. However, since DTMOS PTL with body biasing circuit is an emerging circuit style, not enough work has been carried out to further examine its effectiveness particularly in deep submicron technologies. The basic SOI PTL structure in [5, 6, 7] uses nMOS-only pass transistor trees to reduce cell size. The full rail-to-rail swing of the output signal is restored by an extra level restoring logic at the output of a SOI PTL gate. The existence of level-restoring logic at the output of PTL gates not only slows down the PTL gates due to potential drive-fights, but also increases their power consumption.

In this paper we present a new SOI PTL gate where an active body control circuit is used to allow increase in supply voltages, and we compare the proposed SOI PTL gate with other SOI DTMOS PTL types. The experimental results using two different $0.13\mu m$ SOI technologies show that the proposed SOI PTL gate with one auxiliary transistor for each nMOS and pMOS transistor shows a significant performance improvement and power reduction over the other SOI DTMOS PTL gates.

The remaining part of this paper consists of four sections. In Section 2 basic body bias control technique for pass-transistor will be reviewed. The detailed analysis for three PTL gates using body bias control circuit will be given in Section 3. Section 4 shows the experimental results. Concluding remarks are given in Section 5.

2 Body Bias Control Techniques for Pass-Transistor

The nMOS pass-transistor circuit with active body bias circuit shown in Figure 1(a)[6] uses two auxiliary transistors, N_{a1} and N_{a2}, to clamp main transistor body voltage. However, this DTMOS configuration requires a significant amount of extra silicon area due to two auxiliary transistors. In addition, since the body potential of the main transistor is divided between two auxiliary transistors, it may not rise high enough to speed up the signal transfer from source to drain. The asymmetrical dynamic threshold pass-transistor (ADTPT)[7] scheme shown in Figure 1(b) can achieve faster signal transfer from source to drain because the main transistor body potential can be increased to further than that of the main transistor body in Figure 1(a). The main drawback of these two DTMOS schemes

*This research was partially supported by HP

0-7695-1881-8/03 $17.00 © 2003 IEEE

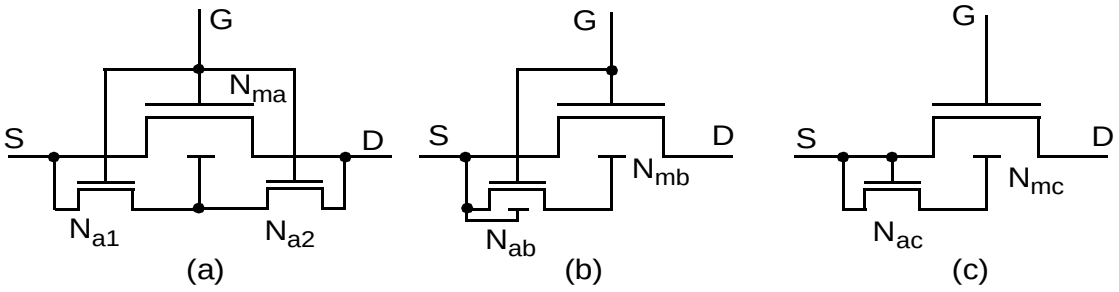

Figure 1: Different body bias control circuits for DTMOS

using auxiliary transistor(s) to allow increase in supply voltages is that the capacitance at gate terminal is increased because the gate of auxiliary transistor is connected to the gate of the main transistor. The DTMOS pass-transistor in Figure 1(a) sees more gate capacitance than that in Figure 1(b). Therefore, the circuit in Figure 1(b) is expected to be faster than Figure 1(a).

Figure 1(c) shows one of the body bias control circuits proposed in [4] for SOI DTMOS static gates. As shown in the figure, the gate of auxiliary transistor N_{ac} is connected to the source of the main transistor N_{mc}, and the source of N_{ac} is also connected to the source of N_{mc}. Therefore, the capacitance seen at the gate of main transistor N_{mc} is reduced compared to both DTMOS pass-transistor techniques in [6, 7]. The main advantage of this body biasing technique can explained as follows.

When V_G and V_S are both high, the auxiliary transistor N_{ac} is off. Since N_{ac} is off by the fact that the voltage difference gate and drain connected to main body is less than V_t, the capacitive coupling between the body and the drain of the auxiliary transistor N_{ac} is not shielded by a channel. When V_S goes to low, the capacitive coupling between the main transistor N_{mc} body and the gate/source of N_{ac} quickly discharges the body charge, and the body voltage dropped to the voltage above zero level because of capacitive coupling. However, the DTMOS schemes in Figures 1 (a) and (b) pulls the body voltage down to zero because the auxiliary transistors, N_{a1} and N_{ab}, are turned on during the discharge process. When V_S in Figure 1(c) goes to high, the initial body potential is increased by the capacitive coupling. When the gate voltage is increased above the V_t of N_{ac}, N_{ac} is on and the body charging process is accelerated. This body charging process is also faster than those of in Figures 1 (a) and (b).

Furthermore, the performance of pass-transistor in [7] is determined only for the delay from source to drain when the input signal at source switches from low to high. However, in a PTL circuit, a signal path can be from source to drain when the gate is in high-state or from gate to drain when the source is low or high. Assuming that the source voltage V_S is high and the gate signal (V_G) changes from low to high, Figure 1(c) can take the full advantage of dynamic threshold voltage. When

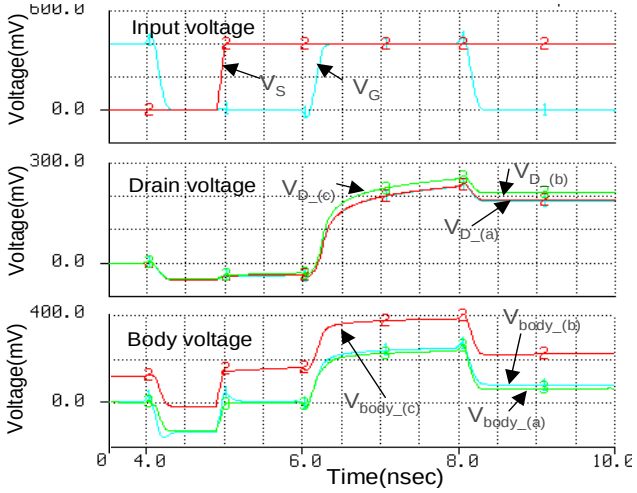

Figure 2: The body voltage of main transistors in Figure 1

the source voltage V_S is high and the gate voltage V_G is low, the body of the main transistor N_{mc} in Figure 1(c) stays a level higher than the main body of Figures 1 (a) and (b) as shown in Figure 2. This is because the capacitive coupling through N_{ac} charges the main body of Figure 1(c) while the main body of Figures 1 (a) and (b) stays low because the auxiliary transistors are off. As V_G goes to high, the body voltage of the N_{mc} is further increased. As shown in Figure 2, the body voltage of Figure 1(c), $V_{body\_(c)}$, is higher than the body voltage of the main transistors in Figures 1 (a) and (b). Therefore, the DTMOS pass-transistor using active body biasing technique in Figure 1(c) is faster than the methods in [6] and [7]. When the gate voltage V_G is high and the source voltage V_S changes from low to high, Figure 1 (c) sees slightly higher capacitance than Figures 1 (a) and (b) because of the auxiliary transistor N_{ac}. However, the auxiliary transistor N_{ac} is small and the delay from the source to drain also mainly depends on the body potential of the main transistor. Since Figure 1 (c) maintains higher body potential than that of Figures 1 (a) and (b) because of capacitive coupling through N_{ac}, the delay from the source to drain of Figure 1 (c) is also smaller than that of Figures 1

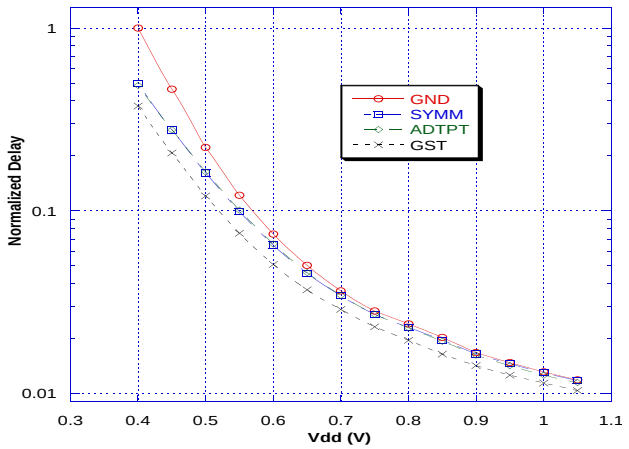

Figure 3: Normalized average delay of pass-transistors with different body control scheme.

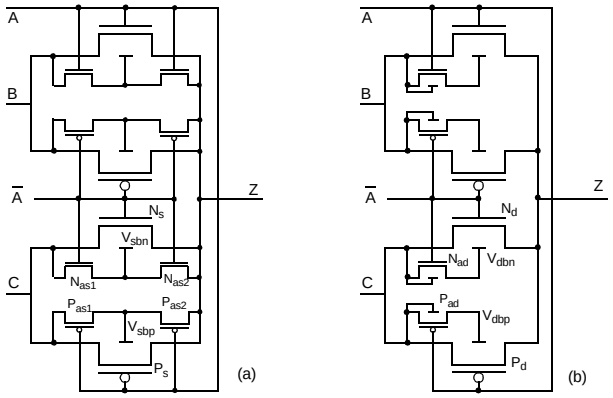

Figure 4: DTMOS PTL using symmetrical and ADTPT structure. (a)Symmetrical structure. (b)ADTPT structure

(a) and (b). Figure 3 shows the average delay of the circuits in Figure 1. In Figure 3, SYMM, ADTPT, GST, GND represent the normalized average delay of Figure 1(a), Figure 1(b), Figure 1(c), and body-grounded pass transistor, respectively.

3 Dynamic Threshold PTL Gates

Dynamic threshold transistor structure shown in Figure 1(c) in [4] was intended and experimented in context of static CMOS circuits only. Its suitability and performance characteristics for PTL logic has not been fully understood. The effect of threshold voltage drop can have significant impact on performance in DTMOS because DTMOS is usually operated at lower voltage for low-power applications. The previous methods of SOI PTL[6, 7, 8] using only nMOS for the signal path of non-control inputs suffers from the threshold voltage drop and requires a level restoring logic at the output of pass-transidtor

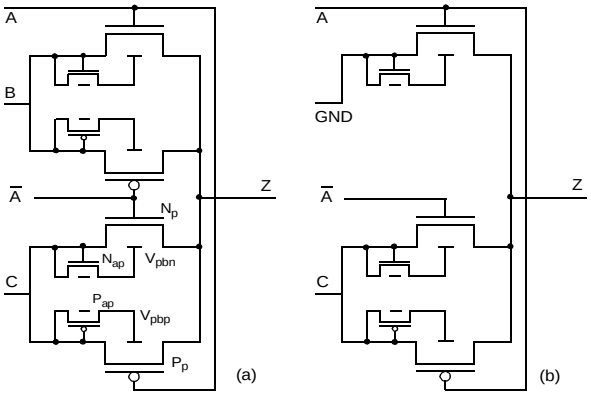

Figure 5: (a)DTPTL+ structure. (b)A variation of DTPTL+ when signal B is connected to ground

resulting in significant increase in power and delay. Therefore, the SOI PTL types with nMOS or pMOS only circuits for the non-control signal path will not be considered in this paper. Instead, a SOI PTL type which uses both nMOS and pMOS transistors will be considered. Figure 4 (a) and (b) shows the SOI DTMOS PTL implementations, that performs the XOR function, using symmetrical and ADTPT techniques, respectively. As shown in Figure 4, the body of each nMOS (pMOS) main transistor in symmetrical DTMOS PTL is connected to the source/drain of two auxiliary nMOS (pMOS) transistors while the body of each nMOS (pMOS) main transistor of ADTPT is connected to the drain (source) of only one nMOS (pMOS) auxiliary transistor.

Let's examine the switching characteristics of these circuit structures in PTL logic. When V_A is low and V_C is high, the pMOS main transistors, P_s and P_d, of symmetrical and ADTPT are on while nMOS main transistors (N_s and N_d) are off. The body voltage of P_s and P_d is high. As V_C changes from high to low, the initial discharge path from output Z to input C is formed by the main transistors P_s and P_d for symmetrical and ADTPT structure, respectively. Since both V_{sbp} and V_{dbp} are high, the discharging speed through pMOS for both circuits is almost same. At the same time, the body voltage of nMOS main transistors, V_{sbn} and V_{dbn}, are pulled down by the capacitive coupling of the main transistors (N_s and N_d) which are in off-state. When input V_C goes down below device threshold voltage V_t, the discharging path is changed from pMOS main transistor to nMOS main transistor. From this time, the discharging speed of the body voltage of N_d is quicker than that of N_s. This is because the body of N_d is pulled down by the auxiliary transistor N_{ad} which is in on-state while the body voltage of N_s is pulled down slowly by the effect of the auxiliary transistor N_{as2}. Since the decreasing speed of V_{sbn} is slower than that of V_{dbn}, the symmetrical structure is faster than ADTPT structure as shown in Figure 6.

Figure 5(a) shows another DTMOS PTL structure referred

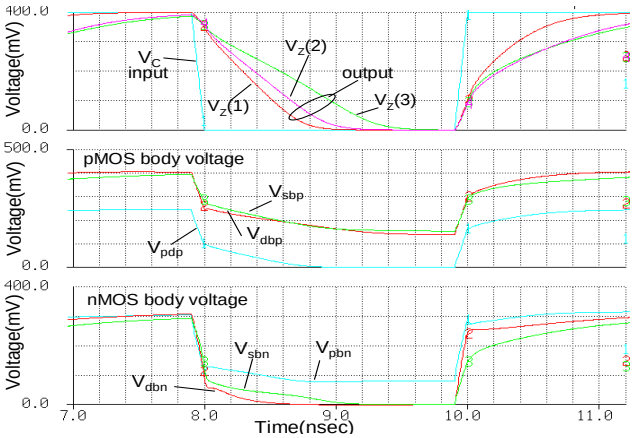

Figure 6: The body voltages of the pMOS and nMOS main transistors. $V_z(1)$, $V_z(2)$, and $V_z(3)$ represent the output voltage of DTPTL+, Symmetrical, and ADTPT PTL gates, respectively.

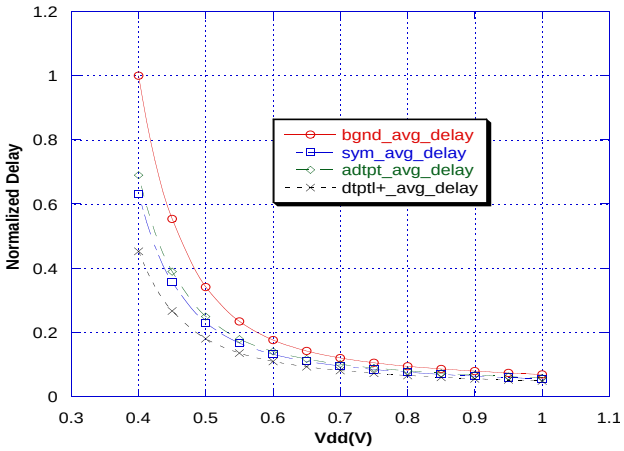

Figure 7: Normalized average delay vs. supply voltage (Process A).

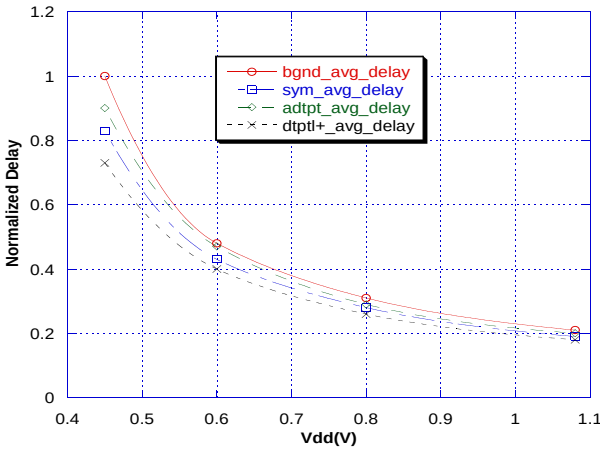

Figure 8: Normalized average delay vs. supply voltage (Process B).

to as DTPTL+. For the DTPTL+ case, when V_A is low and V_C is high, the body voltage of pMOS main transistor, P_p, is much lower than that of symmetrical and ADTPT because a small amount of charge is injected to the body of P_p by off-state auxiliary transistor P_{ap} during the body charging process. During discharging when V_C goes down, the auxiliary transistor P_{ap} is on and the body of P_p quickly discharges to zero as shown in Figure 6. On the other hand, the body of nMOS main transistor N_p is not pulled down to ground level because N_{ap} is in off-state during the discharge. The voltage discharging speed through nMOS main transistor is also faster than symmetrical and ADTPT structure. Therefore, DTPTL+ is faster than the other two DTMOS PTL structure.

When the PTL structures described above used in SOC applications, the load capacitance of driving gate can be reduced by removing some of the main and auxiliary transistors as shown in Figure 5(b).

4 Experimental Results

The SOI DTMOS PTL gates described in Section 3 were implemented in two different $0.13\mu m$ SOI CMOS technologies (process A and process B). The main difference between process A and process B is that the channel doping density of process B is lower than that of process A. Therefore, the threshold voltage of process B is slightly lower than that of process A, and the transistors in process B is leakier than those in process A. As such, the body effect in process B will not be as pronounced as that in process A. Most of existing research on DTMOS used partially depleted SOI (PDSOI) process models with a great deal amount of body effect. Process A resembles the PDSOI characteristics of most of the PDSOI processes on what most of the DTMOS experiments were based. Process B, however, is the result of tuning process parameters for better performance and power consumption of standard CMOS circuits. The goal of investigating DTMOS performance and power consumption on two different PDSOI processes is to better understand the impact of PDSOI parameters on DTMOS.

Since the signal pathes for the gates can be from non-control inputs to output as well as from control-input to output, all possible signal pathes were chosen to compare delay and power consumption. The simulation results of the DTMOS PTL were also compared to body-grounded CMOS style PTL gate. The simulation was done by a SPICE simulator which uses BSIM3SOI model.

Figures 7 and 8 show the normalized average delay of the gate using the proposed method is lower than that of the symmetrical and ADTPT structures because the threshold voltage

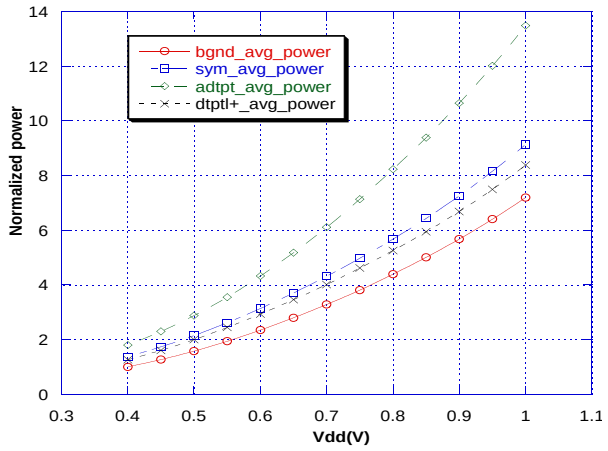

Figure 9: Normalized average power vs. supply voltage (Process A).

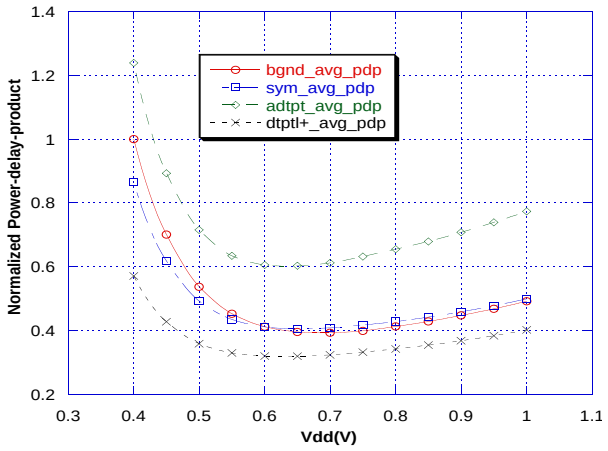

Figure 11: Normalized average power-delay-product vs. supply voltage (Process A).

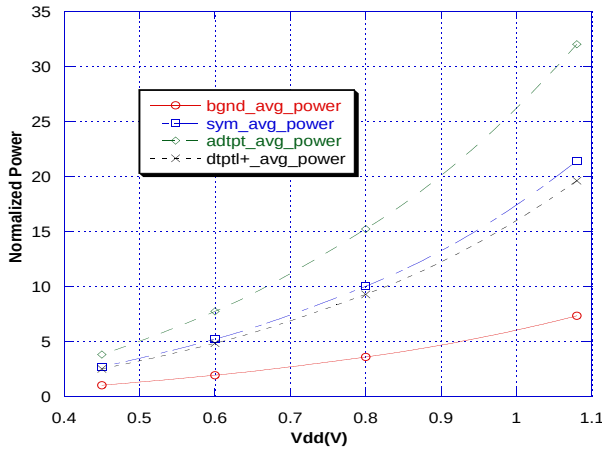

Figure 10: Normalized average power vs. supply voltage (Process B).

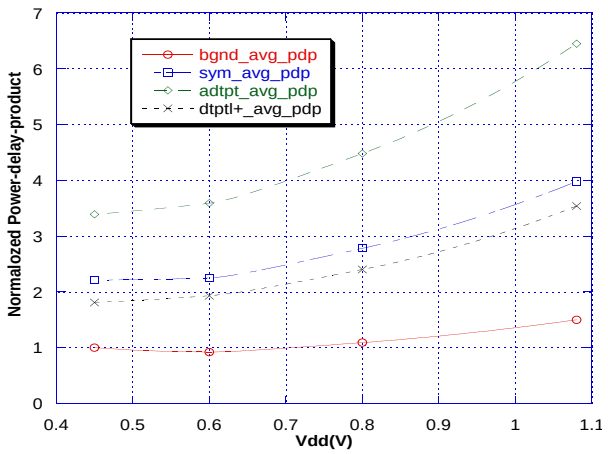

Figure 12: Normalized average power-delay-product vs. supply voltage (Process B).

of main transistor in the proposed gate is lower than that of symmetrical and ADTPT structure. In Figures 7 and 8, bgnd, sym, adtpt, and dtptl+ represent body-grounded, symmetrical, ADTPT, and DTPTL+ PTL gates, respectively. The delay of body-grounded PTL gate is higher than the PTL gate with body bias control circuit. The performance gain of DTPTL+ can be seen for both processes over the whole voltage range. Therefore, the DTPTL+ structure is desirable for high-performance SOC design using PTL logic.

The normalized average power consumption, normalized power-delay-product, and normalized energy-delay-product are shown in Figures 9 and 10, Figures 11 and 12, and Figures 13 and 14, respectively. The average power consumption of DTPTL+ is lower than that of symmetrical and ADTPT structures, and the power consumption of ADTPT structure is higher than that of symmetrical DTMOS PTL structure. The power-delay-product and energy-delay-product of DTPTL+ circuits are also better than that of symmetrical and ADTPT structure. Therefore, DTPTL+ is preferable for lower power applications using PTL logic.

When the average power consumption of the circuits implemented in process B is compared to that in process A, the former has a high average power consumption than the latter. This is consistent with the characteristics of process A and B as discussed earlier. As shown in Figures 11 and 12, the average power-delay-products for circuits in process A increase significantly when supply voltage is less than 0.5V, and this trend is very similar to the power-delay-product curves reported in [6][1], while the average power-delay-products for circuits in process B decrease monotonically as the supply voltage decreases. This results indicates that with leakier transistors in SOI, the advantage in performance and power consumption

[1] In [6], body-grounded and symmetrical SOI PTL structures were reported.

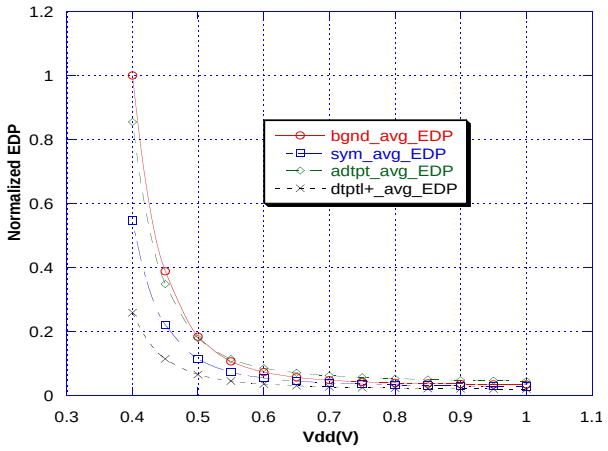

Figure 13: Normalized average energy-delay-product vs. supply voltage (Process A).

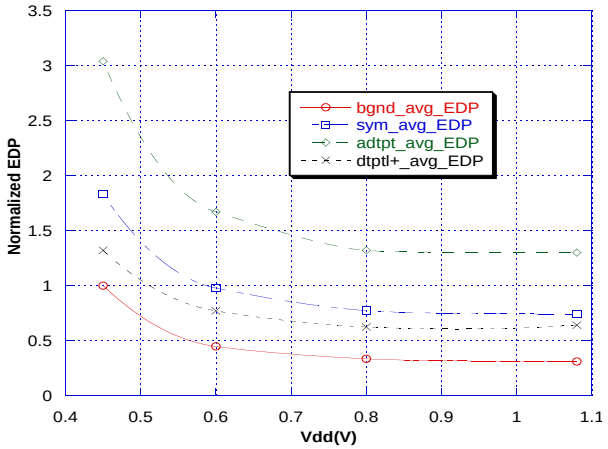

Figure 14: Normalized average energy-delay-product vs. supply voltage (Process B).

due to the floating body effect diminishes. However, among different DTMOS structures, the proposed DTPTL+ structure performs consistently better than others in both power consumption and performance.

5 Conclusions

We presented an SOI PTL structure with adaptive body-bias and compared with different DTMOS PTL structures. All the SOI PTL gates were implemented in two different $0.13\mu m$ SOI CMOS technologies. The experimental results show that the DTPTL+ structure with adaptive body-bias by one auxiliary transistor can achieve better performance than other SOI PTL gate structures. However, DTMOS PTL structures consume more power than body-grounded PTL structure in the same technology because of the forward-biased diode current of the DTMOS structures. Such a power consumption disadvantage is further exacerbated if the floating body effect is reduced by making the transistor leakier. However, DTMOS, and the DTPTL+ structure in particular, maintain a significant performance advantage over non-DTMOS structures. The tradeoffs between performance and power depends on details of process parameters.

References

[1] F. Assaderaghi, D. Sinitsky, S. A. Parke, J. Boker, P. K. Ko, and C. Hu, "A Dynamic threshold voltage MOSFET (DTMOS) for ultra-low voltage operation," in *IEDM Tech. Dig.*, pp. 809–812, 1994.

[2] F. Assaderaghi, D. Sinitsky, S. A. Parke, J. Boker, P. K. Ko, and C. Hu, "Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage VLSI," *IEEE Trans. on Electron Devices*, vol. 44, pp. 414–422, Mar. 1997.

[3] I.-Y. Chung, Y. J. Park, and H. S. Min, "A New SOI Inverter Using Dynamic Threshold for Low-Power Applications," *IEEE Electron Device Letters*, vol. 18, pp. 248–250, June 1997.

[4] M. A. Casu, G. Masera, G. Piccinini, M. R. Roch, and M. Zamboni, "Comparative Analysis of PD-SOI Active Body-Biasing Circuits," in *2000 IEEE International SOI Conference*, pp. 94–95, 2000.

[5] T. Fuse, Y. Oowaki, T. Yamada, and et al, "A 0.5V 200MHz 1-Stage 32b ALU using a Body Bias Controlled SOI Pass-Gate Logic," in *1997 IEEE International Solid-State Circuit Conference*, (Lew Orleans, Louisiana), 1999.

[6] N. Lindert, T. Sugii, S. Tang, and C. Hu, "Dyanmic Threshold Pass-Transistor Logic for Improved Delay at Lower Power Supply Voltages," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 85–89, Jan. 1999.

[7] B.-T. Wang and J. B. Kuo, "A Novel Low-Voltage Silicon-On-Insulator (SOI) CMOS Complementary Pass-Transistor Logic (CPL) Circuit using Asymetrical Dynamic Threshold Pass-Transistor (ADTPT) Technique," in *Proc. 43rd Midwest Symp. on Circuit and Systems*, (Lansing, MI), pp. 694–697, 2000.

[8] R. Puri and C.-T. Chuang, "Hysterisis Effect in Pass-Transistor-Based, Partially Depleted SOI CMOS Circuits," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 625–631, April 2000.